THE SUITABILITY OF ACTIVE INDUCTORS FOR A WIDE RANGE OF CMOS IMPLEMENTATIONS

by

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ABSTRACT

THE SUITABILITY OF ACTIVE INDUCTORS FOR A WIDE RANGE OF CMOS IMPLEMENTATIONS

Integrated circuits (ICs) form the heart of today's technology thanks to their prominent features such as minimal size, reduced cost, high reliability, and low power consumption. Then, inductors have found a wide range of uses in modern IC implementations. These application areas can be exemplified by impedance matching, bandwidth enhancement, gain boosting, frequency selection, phase shifters, and LC oscillators. The frequently preferred method for the required inductances is using CMOS spiral inductors. However, spiral inductors have significant shortcomings that limit their use in CMOS realization. For example, spiral inductors consume a large chip area, and it is impossible to tune their inductance values. Moreover, these inductors have low quality factors (Q) and low self-resonant frequencies. Due to the drawbacks of spiral inductors, researchers have been looking for alternatives. One of these approaches is active inductors (AIs), which use active circuit components to synthesize required inductance. Numerous AI topologies have been presented in the literature. Each architecture may be selected depending on the inductance needs of the application. Thus, AIs have a broad variety of applications in CMOS implementations due to their diversity of topologies. This thesis demonstrates that employing AIs is feasible for a range of CMOS implementations. Its feasibility is proven by designing an AI-based wide-tunable LC voltage-controlled oscillator (LC-VCO), a lattice-based allpass filter, and an autonomous chaotic oscillator.

ÖZET

AKTİF İNDÜKTÖRLERİN GENİŞ YELPAZEDE CMOS UYGULAMALARI İÇİN UYGUNLUĞU

Entegre devreler (IC'ler), minimum boyut, düşük maliyet, yüksek güvenilirlik ve düşük güç tüketimi gibi öne çıkan özellikleri sayesinde günümüz teknolojisinin kalbini oluşturmaktadır. İndüktörler de modern entegre devre (IC) uygulamalarında geniş kullanım alanına sahip bileşenlerlerden biridir. Bu uygulama alanları empedans eşleştirme, bant genişliği geliştirme, kazanç artırma, frekans seçimi, faz kaydırıcılar ve LC osilatörler olarak örneklendirilebilir. CMOS uygulamalarında ihtiyaç duyulan endüktanslar için sıklıkla tercih edilen yöntem spiral indüktörlerin kullanılmasıdır. Ancak, spiral indüktörler CMOS uygulamalarındaki kullanımlarını sınırlayan önemli eksikliklere sahiptir. Örneğin, spiral indüktörler büyük silikon alanı tüketir ve endüktans değerlerinin kontrolü mümkün değildir. Ayrıca, bu indüktörler düşük kalite faktörlerine (Q) ve rezonans frekansına sahiptir. Bu dezavantajlardan dolayı, araştırmacılar CMOS endüktans gerçeklenmesi için farklı alternatifler üzerine çalışmaktadır. Yaklaşımlardan biri, gerekli endüktansı sentezlemek için aktif devre bileşenlerini kullanan aktif indüktör (AI) yapılarıdır. Literatürde çok sayıda AI topolojisi sunulmuştur. Kullanıldığı uygulamanın endüktans ihtiyaçlarına bağlı olarak farklı AI mimarileri tercih edilebilir. Bu nedenle, AI'lar, sahip oldukları topoloji çeşitliliği sayesinde çeşitli CMOS uygulamalarında yer bulur. Bu tezde, frekansı ayarlanabilir LC voltaj kontrollü osilatör (LC-VCO), lattice tabanlı tam geçirgen filtre ve otonom kaotik osilatör tasarlanarak AI devrelerinin CMOS uygulamaları için uygulanabilirliği kanıtlanmıştır.

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A	Angular coefficient
C_p	Equivalent parallel capacitance of inductors
C_{ox}	Oxide capacitance of MOS transistors
$E_n(s)$	Allpass filter denominator
f_t	Transition frequency of MOS transistors
g_m	Transconductance of MOS transistors
H(s)	Transfer function
L	Length of MOS transistors
L_{act}	Equivalent inductance of AI
P_{dc}	DC power consumption
R_p	Equivalent parallel resistance of inductors
R_s	Equivalent series resistance of inductors
V_{sat}	Saturation voltage of MOS transistors
V_{th}	Threshold voltage of MOS transistors
W	Width of MOS transistors
Q	Quality Factor
μ_n	Electron mobility
τ_0	Constant term of the delay function
$\tau_g(\Omega)$	Group delay function
$\phi(\Omega)$	Phase function
Ω	Normalized frequency

LIST OF ACRONYMS/ABBREVIATIONS

AI	Active Inductor
APF	Allpass Filter
ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal-Oxide Semiconductor
DTR	Delay Tuning Range
FAI	Floating Active Inductor
FOM	Figure of Merit
GAI	Grounded Active Inductor
IC	Integrated Circuit
ICMR	Input Common-Mode Range
KCL	Kirchoff Current Law
LC-VCO	LC Voltage-Controlled Oscillator
MOS	Metal-Oxide Semiconductor
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MSB	Most significant bit
NAI	Negative Active Inductor
NMOS	N-type Metal-Oxide Semiconductor
OTA	Operational Transconductance Amplifier
PAI	Positive Active Inductor
PDK	Process Design Kit
PLL	Phase-locked Loop
PMOS	P-type Metal-Oxide Semiconductor
PTR	Percentage Tuning Range
PVT	Process, Voltage, Temperature
RNG	Random Number Generators
THD	Total Harmonic Distortion
TSMC	Taiwan Semiconductor Manufacturing Company
VCO	Voltage-Controlled Oscillator

VDTA	Voltage Differencing Transconductance Amplifier

1. INTRODUCTION

With each passing day, technology increases its prevalence and importance in human life. The widespread use of integrated circuits is one of the fundamental reasons for this increase. As the use of integrated circuits expands, new production technologies continue to be developed in this area. Undoubtedly, the ability to manufacture on-chip inductors is an essential milestone in this technological evolution. Before on-chip inductors were available, off-chip passive inductors were used in communication circuits with limited bandwidth and high cost. With the discovery of IC-compatible inductors in the early 1990s [1], the usage of inductors has increased considerably. Impedance matching circuits, bandwidth enhancement methods, gain boosting techniques, frequency selection systems, RF phase shifters, and LC oscillators can be given as examples of the application areas of on-chip inductors [2–6].

Inductors, which are so popular and widely utilized, have their own set of drawbacks. The main disadvantages of CMOS spiral inductors are that they have a non-tunable structure, consume large silicon areas, have low self-resonant frequencies, and have low quality factors [2, 7]. These unfavorable characteristics highlighted above have led researchers to work on finding different alternatives to the CMOS spiral inductors. As a result of these circumstances, active inductors (AIs) have a significant presence in the literature [8–35]. AIs attracted attention due to their small chip area requirement, large and tunable inductance, self-resonant frequency, and quality factor.

Gyrator-C-based topologies are frequently preferred for AI synthesis. They consist of two back-to-back transconductance stages and a capacitor. In the literature, the transconductance stages of gyrator-C networks are implemented in various ways [9, 12–14]. While [9] employs single transistors to implement the transconductance stages, [12] chooses Voltage Differencing Transconductance Amplifiers (VDTAs) for the same purpose. Differential pairs are used as transconductance stages in [13] whereas Operational Transconductance Amplifiers (OTA) are preferred in [14]. For instance,

single transistor structures enable the design of AI circuits with fewer components, while VDTA-based transconductance stages improve the input common-mode range (ICMR) of the AI. Thus, various AI architectures may be feasible for different application areas, which makes AIs suitable in a very large number of application areas. To illustrate the CMOS implementation diversity of AIs, this thesis designs a wide-tunable LC-VCO circuit for circuits that need a large frequency range, such as phase-locked loop (PLL), a lattice network-based allpass filter structure for 5G applications, and a chaotic oscillator for hardware security applications.

Chapter 2 provides the background information needed to better understand the rest of the thesis. Chapter 3 includes the proposed novel positive and negative AI circuits to be used in CMOS implementations. In Chapter 4, a wide-tunable LC-VCO circuit is designed using proposed novel AI circuits based on the MOSFET-C approach of gyrator-C networks. Chapter 5 describes the design of tunable lattice network-based allpass filter for 5G applications. Chapter 6 discuses the AI-based chaotic oscillator architecture for random number generators (RNGs) in hardware security applications. Finally, the thesis is concluded in Chapter 7.

2. BACKGROUND

This chapter discusses some critical topics related to this thesis in order to make the subsequent chapters more understandable. Section 2.1 introduces CMOS spiral inductors and summarizes their shortcomings. Section 2.2 discusses pros and cons of AI structures in comparison to their spiral counterparts. Then, in Section 2.3, the fundamentals of gyrator-C-based inductors synthesis with grounded and floating configuration are presented. Then, the criteria for evaluating the performance of AIs are discussed in Section 2.4. Finally, the chapter is concluded in Section 2.5.

2.1. CMOS Spiral Inductors

It is one of the critical issues of modern CMOS technologies to realize on-chip inductors, also known as spiral inductors. In today's CMOS technologies, both stacked and planar spiral inductors can be produced. Semiconductor foundries provide comprehensive characterization and accurate component models of these inductors. Thus, designers have the opportunity to carry out their designs by using and simulating these models comfortably. Although multiple metal layers are available in modern CMOS technologies, only the top metal is used to build a planar spiral inductor. Otherwise, parasitic capacitance between the spiral inductor and the substrate can be increased, which is undesirable. Thus, planar spiral inductors have low inductance values; but their parasitic capacitances are also low. On the other hand, the inductance value can be significantly increased by stacking the other metals. However, undesirable parasitic capacitances will be higher for stacked spiral inductors since bottom metal layers are used. CMOS spiral inductors are known for their high linearity and low noise levels. Spiral inductors have a variety of limitations that impact their performance and applications. These drawbacks arising from their physical geometries and the CMOS technologies they are implemented can be listed as follows:

- They have non-tunable inductance values: Once the number of spiral turns is determined, the inductance value of a CMOS spiral inductor is fixed. It is not possible to tune its inductance with a simple control mechanism. There are two possibilities to increase its inductance: increasing the number of spiral turns, which consumes a huge amount of chip area; or having several metal layers stacked, which causes more parasitic capacitance.
- They consume a large silicon area: The silicon area required for routing the spiral of the inductors is high due to the low inductance of spiral inductors. Since the inductance is directly proportional to the spiral turns, a reasonable inductance can only be obtained with a few turns. Moreover, most CMOS technologies do not allow you to put another device under the spiral inductors. Hence, the spiral inductor consumes a significant portion of the silicon alone.
- They have low self-resonant frequencies: The shunt capacitance between the spiral inductor and the substrate forms an LC tank with the series inductance of the spiral inductor. Since the large metal area of the inductor causes large parasitic capacitances, the self-resonant frequency of the LC tank becomes low. The typical self-resonant frequency of spiral inductors is in the low GHz range.
- They have relatively low quality factors: CMOS spiral inductors have an ohmic loss at high frequencies, limiting their quality factors (Q). The skin-effect-induced resistance of the spiral and the resistance produced by eddy currents in the substrate are two factors that contribute to the ohmic loss of spiral inductors.

2.2. General Characteristics of AIs

Circuits that do not contain an inductor but have inductive characteristics are called AIs. These networks have inductive behavior in a specific frequency band under specified DC biasing conditions and signal-swing limitations. The benefits of AIs are listed below:

- They have large and tunable inductance values: The inductance value of an AI is inversely proportional to the transconductance values of the transistors in it.

Thus, this situation makes it possible to obtain large inductance values using small transistors. Also, the inductance value of the circuit can be tuned by adjusting the bias currents of the transistors. In addition to this coarse tuning, fine-tuning can also be done by changing the capacitor values in the circuit.

- A small chip area is enough for them: Generally, MOS transistors are used in AI circuits. Further, the transconductance values of these transistors are inversely proportional to the inductance of the circuit. Thus, the silicon area of the transistors is incomparably smaller than the spiral inductors.
- They have large and tunable self-resonant frequencies: AIs having a high self-resonant frequency are commonly preferred in general applications. For instance, when an AI is used in a low-pass filter, the filter will operate at frequencies below its self-resonant frequency. Thus, an AI having a high self-resonant frequency will have an extensive frequency range for proper operation. Especially for simple structures of CMOS AIs, the self-resonant frequency approaches the transit frequencies (f_t) of the MOS transistors.
- They have large and tunable quality factors: The ohmic loss of CMOS AIs defines the quality factors, determined mainly by the finite output resistance of the transistors in the circuit. In the literature, cascodes, regulated cascodes, and negative resistor compensation techniques are applied to enhance the quality factors of AIs by increasing the equivalent output resistances of the transistors.

Besides the advantages mentioned above, there are also difficulties with AIs. These drawbacks will be discussed below:

- They have limited dynamic range: The inductive characteristics of AIs are based on the DC biasing conditions of the transistors. Thus, the voltage swing on AI ports can directly affect the circuit operation, limiting the dynamic range. Some studies focus on the dynamic range problem in the literature. For instance, the Class AB configuration is proposed to expand the dynamic range [15].
- They are noisy circuits: Since AI circuits consist of MOS transistors, they have noisy characteristics, unlike noiseless spiral inductors. In particular, as the com-

plexity of the circuit increases, the noise it contains also increases. In the literature, some techniques are applied to minimize the noise of AIs. For example, in [16], noise has been tried to be reduced by increasing the quality factor of the AI used in an LC oscillator.

- They are sensitive to process variations: Process variations change many parameters of MOS transistors, especially the threshold value. Thus, the inductance value and quality factor of AIs are directly affected as many parameters change, particularly transconductances and output resistances of the transistors [18]. The effects of these variations are tried to be reduced by using tunability of inductance and quality factor of AIs.
- They can be affected by supply voltage fluctuations: Although the characteristics of spiral inductors are not dependent on the supply voltage, unfortunately, the same is not valid for AIs since DC biasing conditions are directly affected by supply voltage fluctuation. Some of the fluctuation effects can be reduced by using less sensitive topologies and preferring replica-biasing methods [19].

2.3. Fundamentals of Gyrator-C-Based AIs

Gyrator-C-based AIs can be examined under two main categories: single-ended and differential. These groups can also be called grounded and floating, respectively. In this section, the working principles of grounded active inductors (GAIs) and floating active inductors (FAIs) are investigated. In order to understand their working principles more easily, the behavior of lossless AI circuits will be discussed in Sections 2.3.1 and 2.3.3. Then the effect of parasitic resistances and capacitances will be shown in Sections 2.3.2 and 2.3.4.

2.3.1. Lossless Gyrator-C-Based GAIs

Systems with two back-to-back transconductance stages and a capacitor connected to one of the ports are called gyrator-C networks. As shown in Figure 2.1, one of the transconductance stages is positive while the other one is negative. When the

input and output impedances of the transconductance stages are ignored, it is called lossless gyrator-C networks. Even though the lossless gyrator-C network does not exist in practice due to parasitic capacitances and finite conductances of MOS transistors, it is examined to understand the working principle of the gyrator-C based AIs.

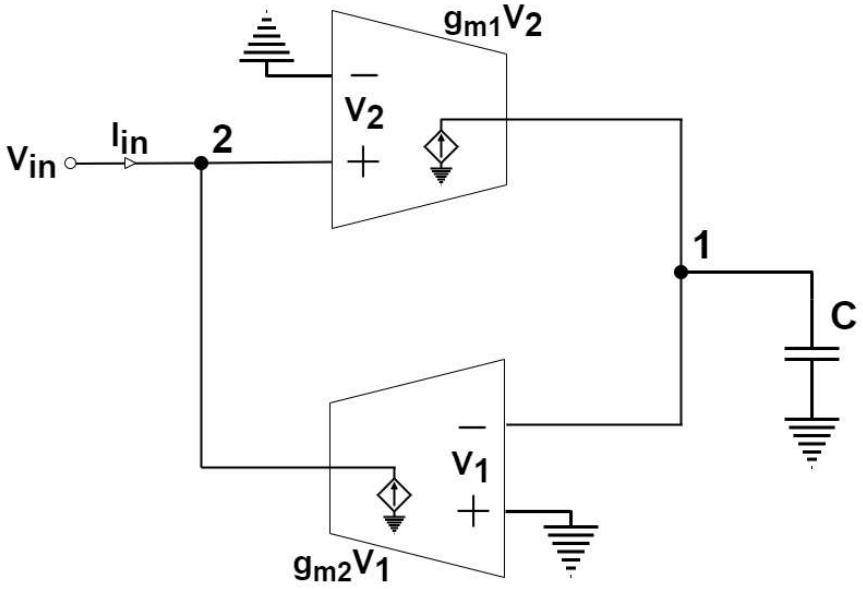


Figure 2.1. The scheme of lossless gyrator-C-based GAI.

The admittance seen looking at port 2 of the gyrator-C network can be expressed by

$$Y_{in} = \frac{1}{Z_{in}} = \frac{I_{in}}{V_2} = \frac{1}{s(\frac{C}{g_{m1}g_{m2}})}, \tag{2.1}$$

which evidences that gyrator-C network has an inductive behaviour with the inductance of

$$L = \frac{C}{g_{m1}g_{m2}}. \tag{2.2}$$

As seen in Equation (2.2), the inductance value of gyrator-C based AIs is proportional to the load capacitance and inversely proportional to the transconductances of the

MOS transistors. By adjusting these parameters, tunable inductive behavior can be obtained as an important property of AIs.

As shown in Figure 2.1, negative and positive transconductance stages are needed to implement the gyrator-C network. A common source amplifier can be used for a negative transconductance stage, while common-gate, common-drain, and differential-pair amplifiers can be used for positive transconductance stages.

2.3.2. Lossy Gyrator-C-Based GAIs

Although lossless inductance was examined in the previous section, AIs encountered in practice are lossy due to the parasitic resistance and capacitance of transistors. The block diagram of lossy gyrator-C GAI is pictured in Figure 2.2.

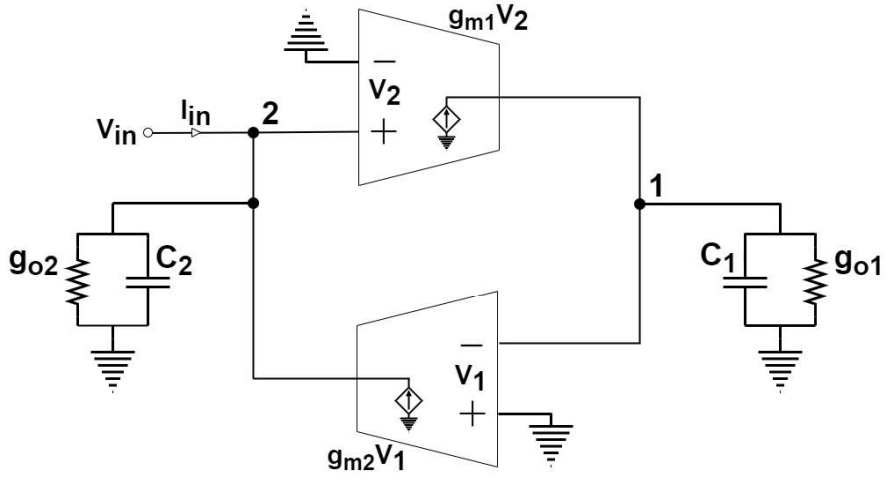


Figure 2.2. The scheme of lossy gyrator-C-based GAI.

The admittance seen looking at port 2 of the lossy gyrator-C network can be expressed by

$$Y_{in} = \frac{1}{Z_{in}} = \frac{I_{in}}{V_2} = sC_2 + g_{o2} + \frac{1}{s(\frac{C_1}{g_{m1}g_{m2}}) + \frac{g_{o1}}{g_{m1}g_{m2}}}, \tag{2.3}$$

while the RLC network equivalent of the lossy gyrator-C GAI is shown in Figure 2.3. The parameters of the RLC system defined by Equation (2.3) can be represented by

$$\begin{aligned} R_p &= \frac{1}{g_{o2}}, \\ R_s &= \frac{g_{o1}}{g_{m1}g_{m2}}, \\ C_p &= C_2, \\ L_{act} &= \frac{C_1}{g_{m1}g_{m2}}. \end{aligned} \tag{2.4}$$

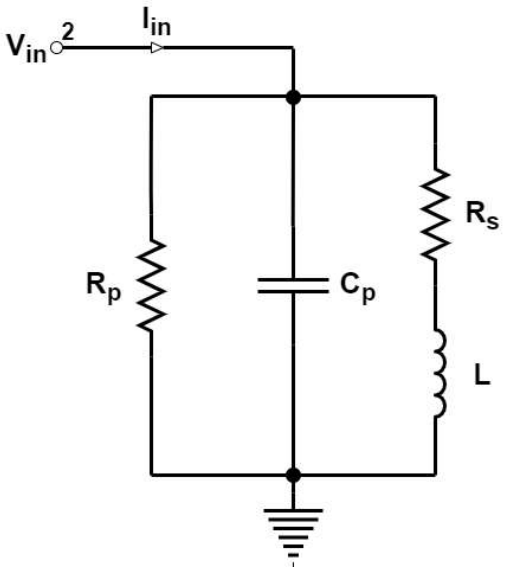


Figure 2.3. The equilavent RLC network of the lossy gyrator-C-based GAI.

As seen in Equation (2.4), ohmic loss of the AI can be reduced by maximizing R_p and minimizing R_s to obtain high-quality inductive behavior. For this purpose, in the literature, Q-enhancement techniques are applied to the inductors [17]. Q-enhacement techniques are used in the designs presented in Chapter 5 and Chapter 6.

2.3.3. Lossless Gyrator-C-Based FAIs

Gyrator-C networks are called gyrator-C FAIs when both terminals are not connected to the ground or power supply. Floating inductors are obtained by making

the transconductance stages of the grounded inductors differential as demonstrated in Figure 2.4.

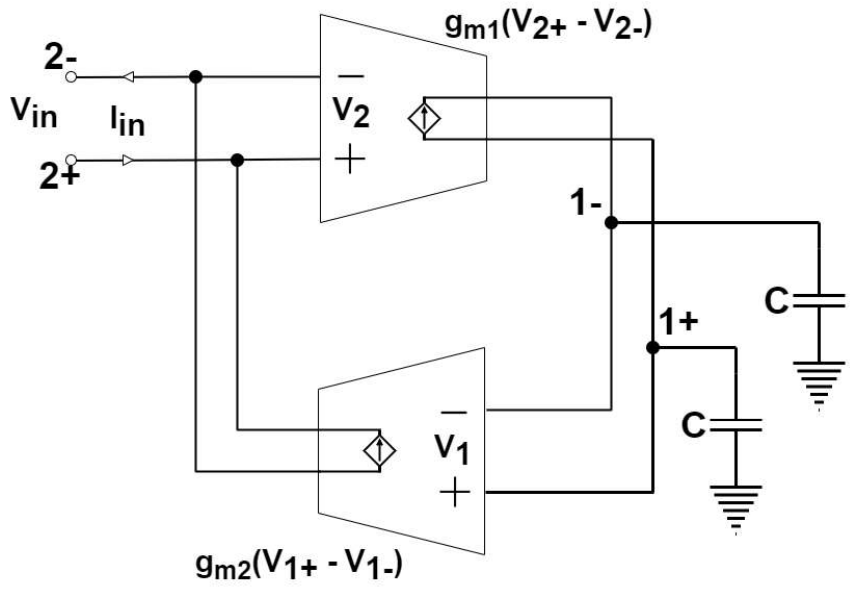


Figure 2.4. The scheme of lossless gyrator-C-based FAI.

The admittance seen looking at port 2 of the lossless gyrator-C network is slightly different than the grounded counterpart as

$$Y_{in} = \frac{1}{Z_{in}} = \frac{I_{in}}{V_{in2}^{+} - V_{in2}^{-}} = \frac{1}{s(\frac{2C}{g_{m1}g_{m2}})}, \tag{2.5}$$

which shows that gyrator-C network has a floating inductance expressed by

$$L = \frac{2C}{g_{m1}g_{m2}}. \tag{2.6}$$

The few advantages of FAIs over grounded ones can be listed as follows:

- The voltage swing of floating inductors is twice that of the grounded counterparts thanks to their differential configuration.
- DC voltage offset between two ports of the AIs are eliminated.

- Differentiating the structure of the AI circuit reduces harmonic distortions.
- They are more suitable for use with noisy digital circuits since their differential structures lessen the impact of common-mode noise.

2.3.4. Lossy Gyrator-C-Based FAIs

The system diagram of lossy gyrator-C FAI is depicted in Figure 2.5.

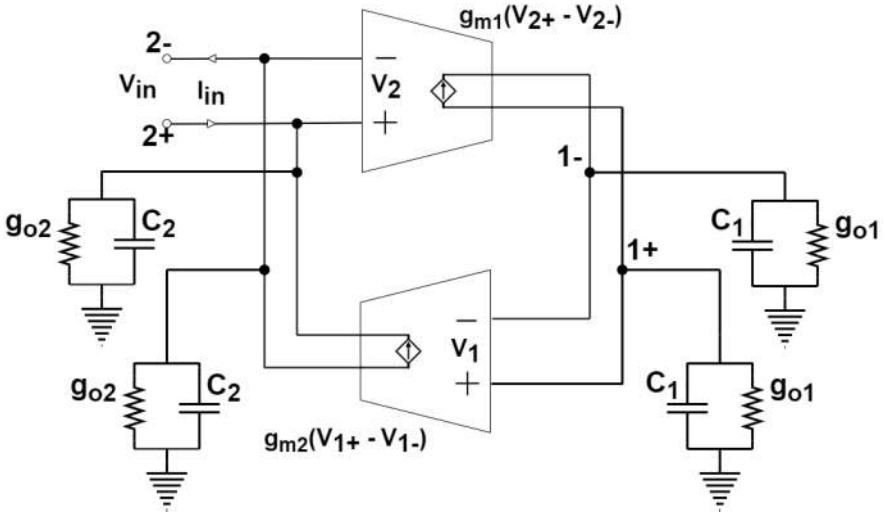


Figure 2.5. The scheme of lossy gyrator-C-based FAI.

These circuits are similar in behavior to the lossy grounded inductors. The admittance equation becomes:

$$Y_{in} = \frac{1}{Z_{in}} = \frac{I_{in}}{V_{in2}^{+} - V_{in2}^{-}} = s\frac{C_2}{2} + \frac{g_{o2}}{2} + \frac{1}{s(\frac{C_1}{2g_{m1}g_{m2}}) + (\frac{g_{o1}}{2g_{m1}g_{m2}})}. \tag{2.7}$$

The parameters of the equivalent RLC circuit of the lossy grounded inductor, depicted in Figure 2.6, can be represented by

$$\begin{aligned} R_p &= \frac{2}{g_{o2}}, \\ R_s &= \frac{g_{o1}/2}{g_{m1}g_{m2}}, \\ C_p &= \frac{C_2}{2}, \\ L_{eq} &= \frac{C_1/2}{g_{m1}g_{m2}}. \end{aligned} \tag{2.8}$$

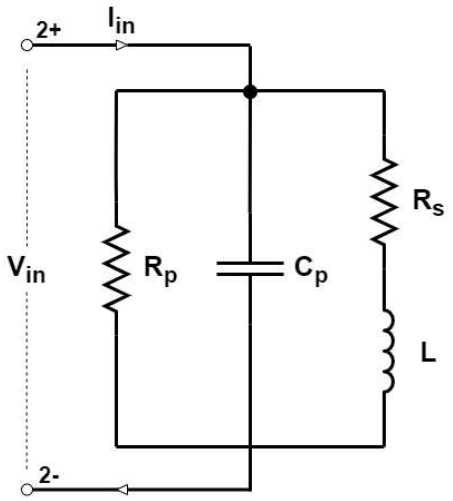


Figure 2.6. The equivalent RLC network of the lossy gyrator-C-based FAI.

Unlike Equation (2.4), the number 2 is added to the RLC parameters in Equation (2.8) due to the differential structure of the floating inductor. Since this circuit also has a differential structure, it has the advantages mentioned in Section 2.3.3.

2.4. Performance Parameters of AIs

The most significant figure-of-merits that offer quantitative measurements of AIs performance are examined in this section.

- Inductance Tunability: AIs are useful circuits for systems where large inductance tuning range is required, such as filters, phase-locked loops, and voltage-controlled oscillators. According to Equation (2.2), it is possible to control the inductance of a gyrator-C AI by varying the transconductances of the MOS transistor and the load capacitance. The former method can be used as coarse tuning method since the transconductances of the transistors have large tuning range. The latter one can be used for as the fine tuning mechanism of the inductance since varactors have a small tuning range. Tuning range of the load capacitor can be increased by using digital control, but it can complicate the system as the chip will need a digital interface.
- Quality Factor: The quality factor (Q), independent of voltage and current in CMOS spiral inductors, depends on the voltage and current swing in AIs. For linear inductors, including AIs, Q value can be calculated as

$$Q = \frac{Im[Z]}{Re[Z]}. \tag{2.9}$$

  As seen in [10], for conventional gyrator-C based active inductors, there are two main ways of increasing Q: increasing g_{o1} or increasing transconductance values g_{m1} and g_{m2}. The transconductance values can be directly adjusted by controlling the bias currents of the circuit, but this method is not usually preferred since it changes the inductance value of the circuit at the same time. On the other hand, different techniques have been proposed to increase g_{o1}. This value can be increased by choosing transistors with large lengths, or cascode devices are can be added to the circuit. Moreover, in some studies, negative resistance circuits are also added to increase the effective g_{o1}.
- Frequency Range: The inductive characteristic of a lossy gyrator-C AI is limited to a certain frequency range. To understand the frequency response of the AI, the RLC equivalent equation can be studied as

$$Z = (\frac{R_s}{C_p L}) \frac{s\frac{L}{R_s} + 1}{s^2 + s(\frac{1}{R_p C_p} + \frac{R_s}{L}) + \frac{R_p + R_s}{R_p C_p L}}, \tag{2.10}$$

$$\omega_p \approx \sqrt{\frac{1}{LC_p}} = w_o. \tag{2.11}$$

Z also has a zero at frequency

$$\omega_z = \frac{R_s}{L} = \frac{g_{o1}}{C_1}. \tag{2.12}$$

As seen in Equation (2.11) and Equation (2.12), upper bound of the inductive frequency range of the AI is determined by the self-resonant frequency ω_o while its lower bound is limited by ω_z. To optimize the frequency range of an AI for a desired inductance value, both R_s and C_p should be reduced.

- Power consumption: In gyrator-C AIs, dc power is consumed to obtain transconductance from the MOS transistors while CMOS spiral inductors do not consume any static power. Because the transconductance and inductance values are inversely proportional, high inductance values can be achieved with low dc currents. Thus, dc power consumption is not a big issue for AIs.
- Noise: As different from CMOS spiral inductors, AIs show high noise behavior since they contain MOS transistors. In [10], detailed noise analysis of gyrator-C networks are included. For the sake of simplicity, detailed information is not included in this thesis. In [36], PMOS transistors are preferred for cascode structure to reduce the noise. Moreover, they can eliminate the nonlinear body effect since they can be produced in separate n-wells.
- Linearity and signal sensitivity: The large voltage swing on the AI can change the small signal characteristics of the MOS transistors in the gyrator-C network. It can even cause the transistors to go out of saturation when the swing is large enough. This situation causes the AI to exhibit nonlinear behavior so that its critical parameters such as inductance value and quality factor change according to the voltage swing on it. This problem is one of the important reasons that prevent the AI from being used widely.
- PVT variation sensitivity: Process, supply voltage and temperature variation can directly affects the dc biasing of the MOS transistors in AIs. Hence, the figure-

of-merits of the AI, especially the inductance value and the quality factor, have deteriorated. Constant g_m biasing techniques can be applied to minimize the supply sensitivity of the circuit. On the other hand, corner analysis and Monte Carlo analysis can be made for process and temperature variation analysis. According to these simulations, design parameters can be tuned to achieve minimal variation in the circuit operation. Moreover, tunable parameters can also be effective to reduce the effect of these variations.

2.5. Chapter Summary

After a discussion of the benefits and drawbacks of spiral inductors and AIs, fundamental concepts of gyrator-C-based AI circuits has been presented. It was demonstrated that gyrator-C networks may be used to make both grounded and floating AIs. Then, performance parameters of AIs have been investigated to understand what to expect from a well designed circuit.

3. PROPOSED ACTIVE INDUCTOR CIRCUITS

In this chapter, novel positive and negative gyrator-C-based AI circuits are presented. Then, some of the proposed circuits are biased so that their transistors operate at the saturation region. Properly biased circuits can be utilized in various CMOS implementations. To demonstrate that they are suitable circuits in IC applications, the proposed circuit in Section 3.1.1 is used for the LC-VCO design presented in Chapter 4.

3.1. Proposed Core Circuits

Novel positive and negative gyrator-C-based AI circuits are introduced in this section. Core circuit schematics of the proposed AIs are demonstrated, and their small signal equations are briefly explained.

3.1.1. Positive Active Inductor - 1 (PAI-1)

Figure 3.1 represents the first proposed positive active inductor circuit, PAI-1. The double arrows mean the transistors can be both NMOS or PMOS. Kirchoff current law (KCL) equations of the small signal representation of the circuit PAI-1 are shown as

$$\begin{aligned} -I_1 - g_{m3}(V_3 - V_1) + g_{m2}(V_2 - V_4) &= 0, \\ -I_2 - g_{m3}(V_3 - V_1) + sC(V_2 - V_3) &= 0, \\ g_{m1}(V_1 - V_4) + sC(V_3 - V_2) &= 0, \\ -g_{m1}(V_1 - V_4) - g_{m2}(V_2 - V_4) &= 0. \end{aligned} \tag{3.1}$$

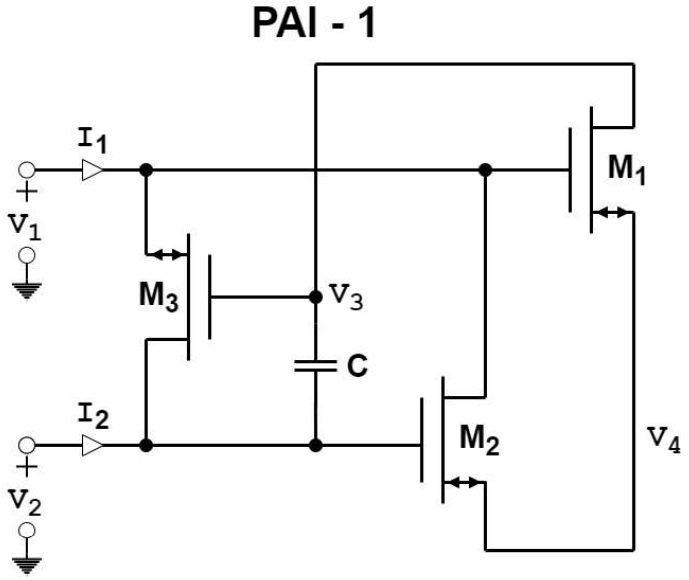


Figure 3.1. The core schematic of the proposed PAI-1 circuit.

When the KCL equations in Equation (3.1) are solved, the equivalent inductance of the proposed circuit PAI-1 can be calculated as

$$L = \frac{C}{(g_{m3})^2}, \quad \text{if} \quad g_{m3} = \frac{g_{m1}g_{m2}}{(g_{m1} + g_{m2})}. \tag{3.2}$$

As seen in Equation (3.2), g_m values of each transistor should be adjusted together to not disturb the inductive behavior. Further, the inductance can also be varied by changing the capacitor C.

3.1.2. Positive Active Inductor - 2 (PAI-2)

The core circuit of the proposed active inductor PAI-2 is depicted in Figure 3.2, which includes four transistors and one capacitor.

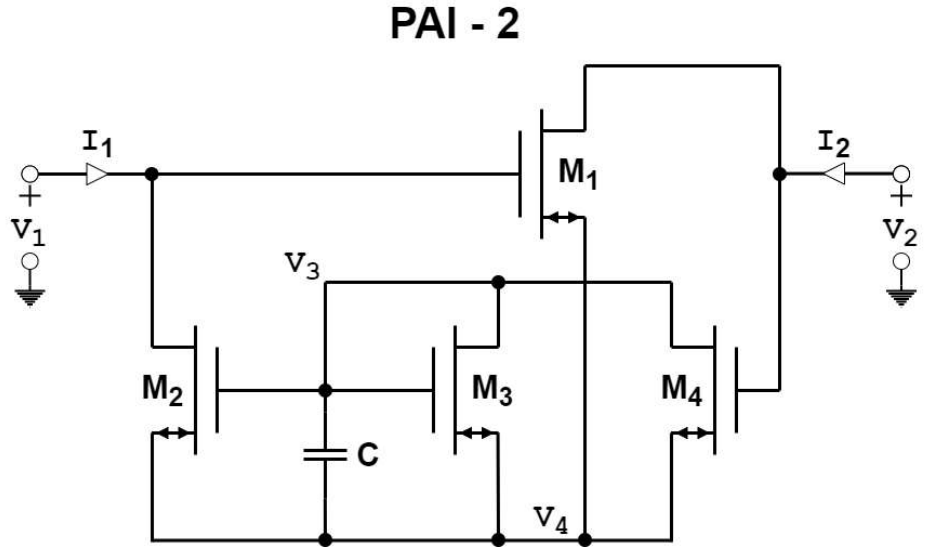


Figure 3.2. The core schematic of the proposed PAI-2 circuit.

KCL small signal equations of PAI-2 circuit can be expressed as

$$\begin{aligned}
&-I_1 + g_{m2}(V_3 - V_4) = 0,\\
&-I_2 + g_{m1}(V_1 - V_4) = 0,\\
&\quad g_{m3}(V_3 - V_4) + g_{m4}(V_2 - V_4) + sC(V_3 - V_4) = 0,\\
&-g_{m1}(V_1 - V_4) - g_{m2}(V_3 - V_4) - g_{m3}(V_3 - V_4) - g_{m4}(V_2 - V_4) + sC(V_4 - V_3) = 0.
\end{aligned} \tag{3.3}$$

According to the individual equations in Equation (3.3), the inductance value of the proposed circuit PAI-2 can be represented by

$$L = \frac{C}{g_{m2}g_{m4}}, \quad \text{if} \quad g_{m1}g_{m3} = g_{m2}g_{m4}. \tag{3.4}$$

The inductance of circuit PAI-2 can be tuned by adjusting both g_{m2} and g_{m4} values of the transistors. In order not to disturb the inductive behavior, g_{m1} and g_{m3} values should be increased at the same time.

3.1.3. Negative Active Inductor - 1 (NAI-1)

Figure 3.3 represents the first proposed negative active inductor circuit, NAI-1. KCL small signal equations of NAI-1 circuit can be stated as

$$\begin{aligned} &-I_1 + g_{m1}(V_3 - V_4) = 0, \\ &-I_2 - g_{m2}(V_1 - V_2) + g_{m3}(V_1 - V_4) = 0, \\ &\quad g_{m2}(V_1 - V_2) + sC(V_3 - V_4) = 0, \\ &-g_{m1}(V_3 - V_4) - g_{m3}(V_1 - V_4) + sC(V_4 - V_3) = 0. \end{aligned} \tag{3.5}$$

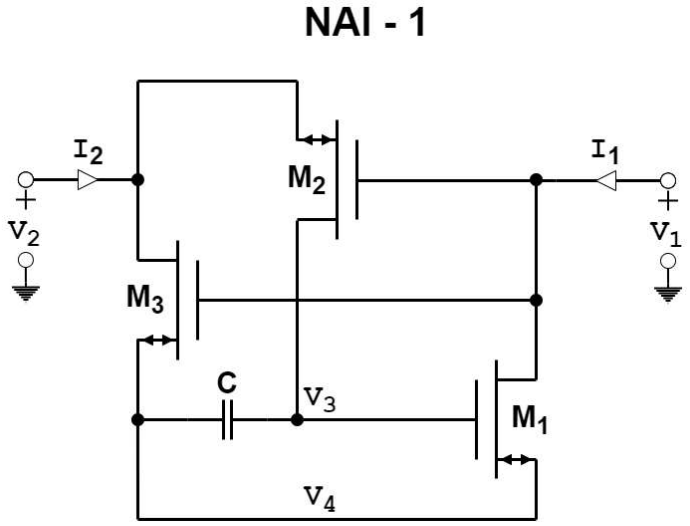


Figure 3.3. The core schematic of the proposed NAI-1 circuit.

When the KCL equations in Equation (3.5) are solved, the equivalent negative inductance of the proposed circuit NAI-1 can be represented by

$$L = -\frac{C}{g_{m1}g_{m2}}. \tag{3.6}$$

Transconductance values g_{m1}, g_{m2} and the capacitor C can control the inductance value of the circuit NAI-1. All three parameters can be used for tuning since there is no if condition for the inductive behavior of the proposed circuit.

3.1.4. Negative Active Inductor - 2 (NAI-2)

Figure 3.4 shows the schematic of the proposed negative active inductor circuit, NAI-2. KCL small signal equations of the proposed NAI-2 circuit can be described as

$$\begin{aligned} &-I_1 - g_{m1}(V_3 - V_1) = 0, \\ &-I_2 + g_{m3}(V_3 - V_4) = 0, \\ &\quad g_{m1}(V_3 - V_1) + g_{m2}(V_2 - V_4) + sC(V_3 - V_4) = 0, \\ &-g_{m3}(V_3 - V_4) - g_{m2}(V_2 - V_4) + sC(V_4 - V_3) = 0. \end{aligned} \tag{3.7}$$

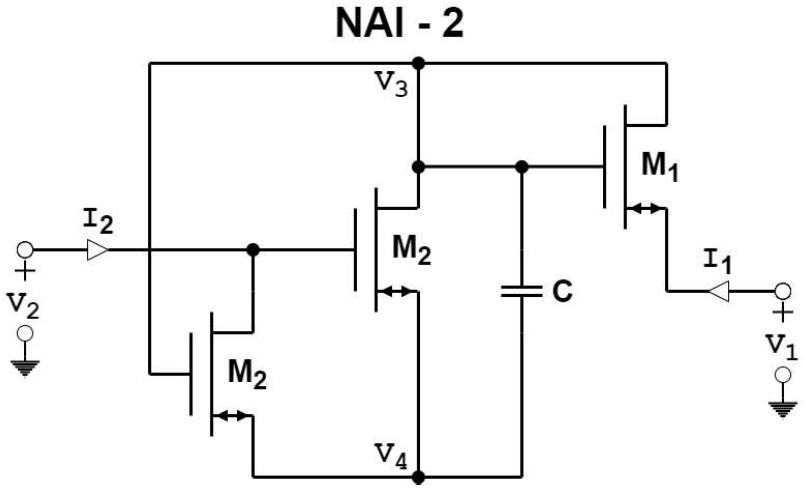


Figure 3.4. The core schematic of the proposed NAI-2 circuit.

According to the equations in Equation (3.7), the negative inductance of the circuit NAI-2 can be expressed by

$$L = -\frac{C}{g_{m2}g_{m3}}, \quad \text{if} \quad g_{m1} = \frac{g_{m2}g_{m3}}{g_{m2} + g_{m3}}. \tag{3.8}$$

As seen in Equation (3.8), the negative inductance value of the circuit NAI-2 can be tuned by changing the capacitor C and the transconductances of the MOS transistors M_2 and M_3 if g_{m1} meets the requirement of the given condition.

3.1.5. Negative Active Inductor - 3 (NAI-3)

Figure 3.5 represents a novel negative active inductor circuit, NAI-3. KCL equations of the small signal equivalent of the circuit NAI-3 can be written as

$$\begin{aligned} &-I_1 + g_{m2}(V_3 - V_2) = 0, \\ &-I_2 - g_{m2}(V_3 - V_2) - g_{m3}(V_1 - V_2) + sC(V_2 - V_3) = 0, \\ &\quad g_{m1}(V_1 - V_4) + sC(V_3 - V_2) = 0, \\ &-g_{m1}(V_1 - V_4) + g_{m3}(V_1 - V_2) = 0. \end{aligned} \tag{3.9}$$

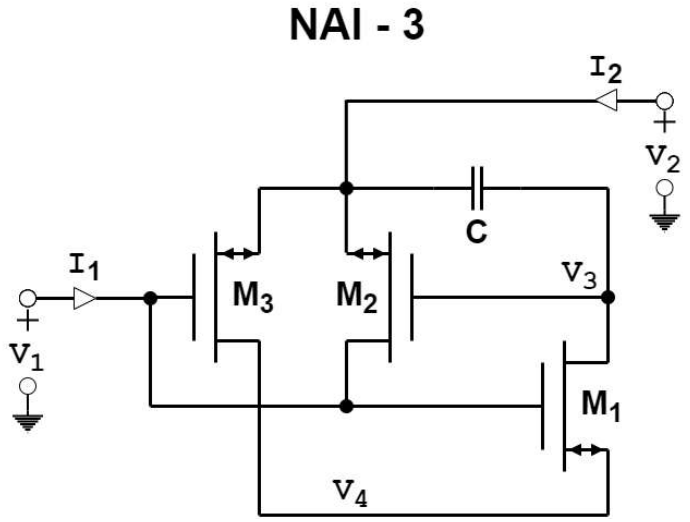


Figure 3.5. The core schematic of the proposed NAI-3 circuit.

From the Equation (3.9), the negative inductance value of the circuit NAI-3 can be derived as

$$L = -\frac{C}{g_{m2}g_{m3}}. \tag{3.10}$$

As seen in Equation (3.9), the circuit NAI-3 has an inductive behaviour depending on the capacitor C and the transconductances of the MOS transistors M2 and M3. Since there is no conditional statement of its inductive behaviour, it is possible to tune the inductance directly without affecting the inductive characteristics of the circuit.

3.1.6. Negative Active Inductor - 4 (NAI-4)

Figure 3.6 shows a proposed novel negative active inductance circuit, NAI-4. KCL small signal equations of NAI-4 circuit can be described as

$$\begin{aligned} &-I_1 + g_{m2}(V_3 - V_2) = 0, \\ &-I_2 + g_{m2}(V_3 - V_2) + g_{m3}(V_2 - V_4) + sC(V_2 - V_3) = 0, \\ &\quad g_{m1}(V_1 - V_4) + sC(V_3 - V_2) = 0, \\ &-g_{m1}(V_1 - V_4) - g_{m3}(V_2 - V_4) = 0. \end{aligned} \tag{3.11}$$

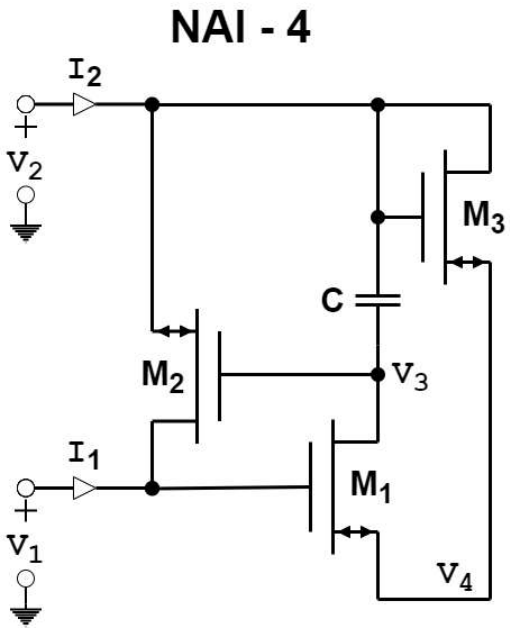


Figure 3.6. The core schematic of the proposed NAI-4 circuit.

According to the equations in Equation (3.11), the inductance of the proposed circuit NAI-4 can be expressed by

$$L = -\frac{C(g_{m1} + g_{m3})}{g_{m1}g_{m2}g_{m3}}. \tag{3.12}$$

which shows that the inductance of the circuit NAI-4 can be tuned by adjusting the g_{m1}, g_{m2} and g_{m3} values.

3.1.7. Negative Active Inductor - 5 (NAI-5)

Figure 3.7 represents the negative active inductance circuit, NAI-5. KCL small signal equations of NAI-5 circuit can be stated as

$$\begin{aligned} &-I_1 + g_{m1}(V_3 - V_4) = 0, \\ &-I_2 - g_{m2}(V_1 - V_2) - g_{m3}(V_3 - V_2) + sC(V_2 - V_3) = 0, \\ &\quad g_{m2}(V_1 - V_2) + sC(V_3 - V_2) = 0, \\ &-g_{m1}(V_3 - V_4) + g_{m3}(V_3 - V_2) = 0. \end{aligned} \tag{3.13}$$

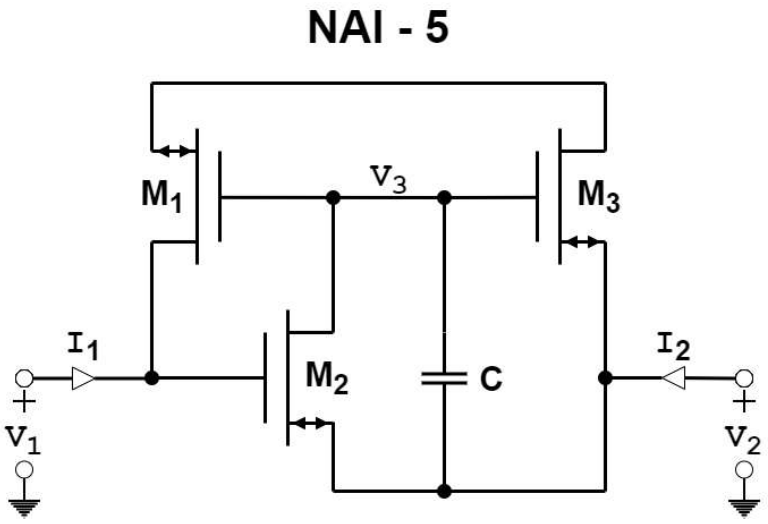


Figure 3.7. The core schematic of the proposed NAI-5 circuit.

When the small signal KCL equations in Equation (3.13) are solved, the equivalent inductance of the circuit NAI-5 can be calculated as

$$L = -\frac{C}{g_{m2}g_{m3}}. \tag{3.14}$$

which demonstrates that the inductance value NAI-5 circuit can be linearly controlled by adjusting the g_{m2} and g_{m3} values. Moreover, inductance tuning does not affect the inductive characteristics of the circuit since there is no conditional statement in Equation (3.14).

3.2. Biased Circuit Configurations

This chapter presents biased versions of several of the core circuits proposed in Section 3.1.

3.2.1. Biased Version of PAI-1

Figure 3.8 depicts the biased configuration of the core circuit PAI-1 presented in Section 3.1.1. For DC shifting purpose, diode connected NMOS transistors M_4 and M_5 added to the circuit in Figure 3.1. Then, bias currents $I_{b1\text{-}4}$ are added to provide required tail currents. For this circuit, M_1 and M_2 transistors are selected NMOS type while M_3 is chosen as PMOS type. The complementary version of this configuration can also be biased correctly according to the requirements of the system to be used.

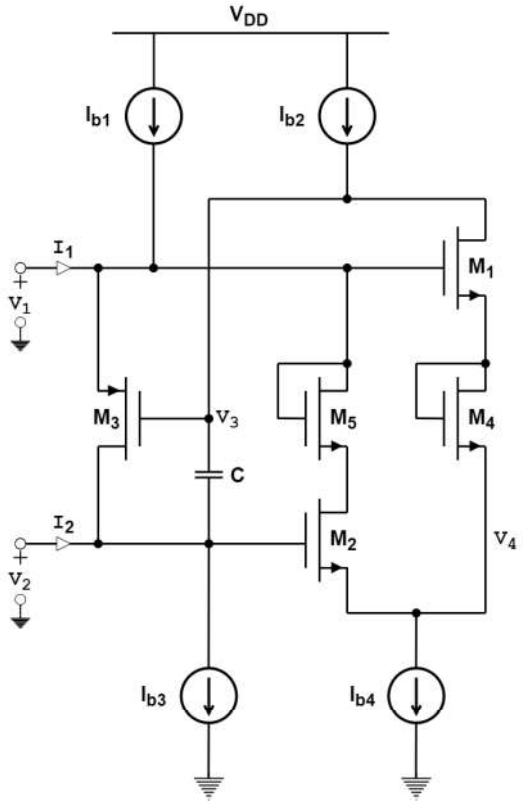


Figure 3.8. The schematic of the biased version of PAI-1 circuit.

Although the circuit given in Figure 3.8 has floating characteristics, there is a DC offset between its two terminals. To eliminate the DC offset and improve the THD behavior of the circuit, this structure can be joined together with its duplicated version to create fully differential topology. This technique is used in the LC-VCO design presented in Chapter 4.

3.2.2. Biased Version of NAI-5

Figure 3.9 demonstrates the biased version of the NAI-5 core circuit given in Figure 3.7. All transistors are chosen as NMOS type in this configuration, but different transistor types can be selected if needed. For example, the case where all transistors are PMOS can also be properly biased. Moreover, bias currents $I_{b1\text{-}3}$ are added to provide required tail currents.

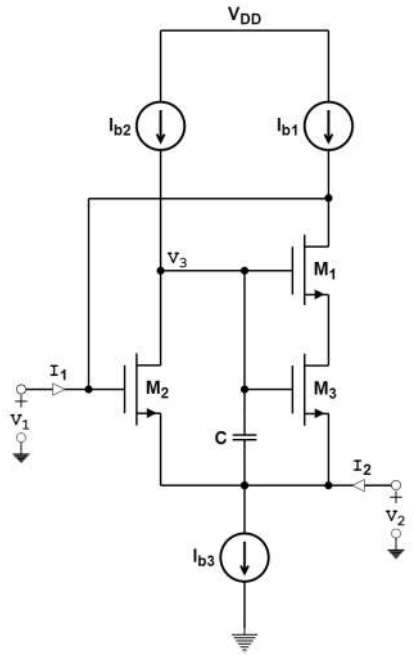


Figure 3.9. The schematic of the biased version of NAI-5 circuit.

Figure 3.10 illustrates the fully differential form of the biased NAI-5 circuit shown in Figure 3.9, which is obtained by connecting two NAI-5 circuits from their v_2 nodes.

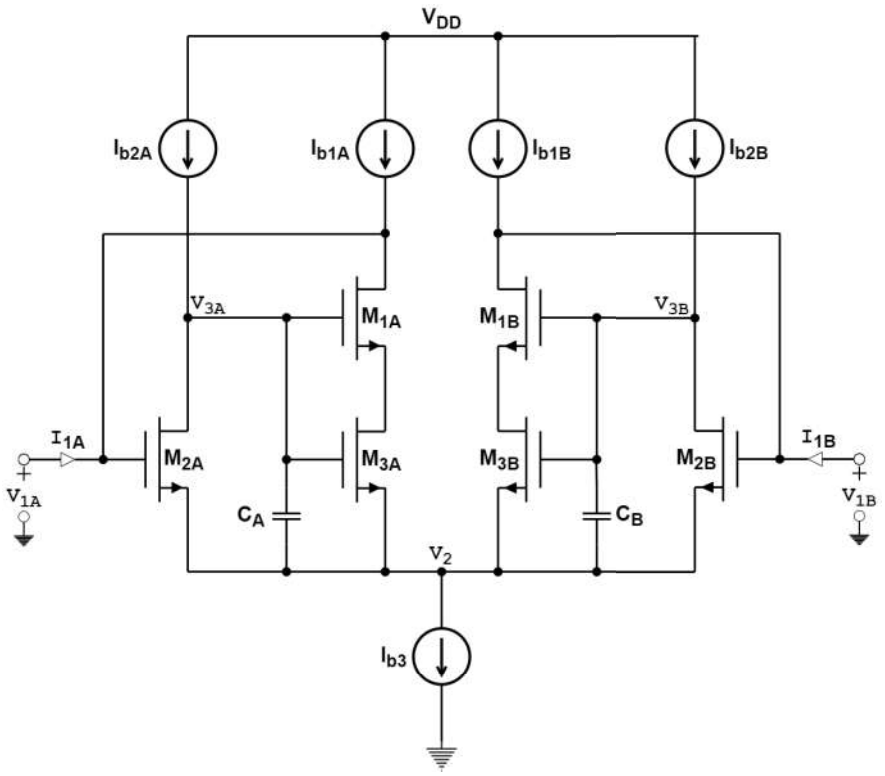


Figure 3.10. The schematic of the fully differential NAI-5 circuit.

For the fully differential version, the equivalent inductance equation given (3.14) is revised as follows

$$L = -\frac{2C}{g_{m2}g_{m3}}. \tag{3.15}$$

3.3. Chapter Summary

This chapter has proposed gyrator-C-based PAI and NAI circuits, as well as biased configurations of several of them. Moreover, small signal equations and corresponding inductance values of the suggested circuit have been included, along with summary comments concerning the circuit equations. As seen in Chapter 4, the proposed AI architectures in this chapter are compatible with CMOS implementations.

4. WIDE-TUNABLE LC-VCO DESIGN WITH A NOVEL ACTIVE INDUCTOR

4.1. Chapter Introduction

Voltage-controlled oscillators (VCOs) are critical components of modern communication and signal processing systems. They are crucial for Phase-Locked Loop (PLL) circuits used for synchronization and frequency demodulation. PLLs are generally fully integrated structures that try to lock onto an off-chip reference clock. LC-VCOs are often preferred in such systems due to low phase noise performance [37]. However, CMOS implementations of LC-VCOs require spiral inductors, which consume a significant amount of silicon area. Additionally, these structures lack a wide tuning range. These limitations of spiral inductors-based VCO architectures have prompted researchers to look for alternatives. In this direction, apart from the ring oscillator-based architectures mentioned in [38, 39], LC-VCO architectures employing AIs rather than spiral inductors are described as in [20–22].

AIs outperform spiral inductors in terms of tunable factors such as inductance value and quality factor (Q). Additionally, they occupy considerably less silicon area than spiral inductors, making them significantly more cost-effective. On the other hand, they cannot meet spiral inductors' phase noise performance and consume static current [10]. The literature involves a number of AI structures based on a variety of different principles [23–27]. Among these topologies, MOS-only gyrator-C-based topologies have risen to prominence due to their low number of transistors and ability to achieve high frequencies [28, 29].

In this chapter, a low-supply LC-VCO based on a novel gyrator-C FAI is designed. It has a wide frequency range due to the tuning mechanism that takes advantage of the FAI's tunability. It is unsuitable for RF applications due to its poor phase noise performance compared to spiral inductors. It is, however, a circuit capable of locating

itself in areas where phase noise is not a significant factor. For instance, its low supply operation and wide tuning range make it an excellent choice for PLLs in digital circuits commonly designed today.

The remainder of this chapter will proceed in the following manner: Section 4.2 introduces the proposed FAI. The frequency response and bias conditions of the circuit are examined, and the design parameters are taken into account while determining the inductor parameters. Section 4.3 discusses the design process for a wide-tuning-range LC-VCO based on the suggested FAI. Section 4.4 presents the Cadence Design Suite post-layout simulation results for the designed oscillator. Additionally, the mechanism that enables wide-tuning is described, as are the oscillator's benefits and drawbacks. Finally, the study was concluded, and future work is discussed in Section 4.5.

4.2. Proposed FAI Circuit

The main principle in generating an AI is to obtain a circuit that satisfies the following two-port short circuit admittance matrix equation:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{1}{sL_{\text{act}}} \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \tag{4.1}$$

where L_{act} is the equivalent inductance value of the AI. In this chapter, we will focus on gyrator-C based architecture, which constitutes a significant part of the proposed AIs in the literature [9, 15, 21, 28, 29]. Among the gyrator-C-based applications, the MOSFET-C approach was preferred considering high-frequency performance and the number of transistors required to implement it.

The core circuit of the proposed AI, computed using the design automation method [30, 31], is illustrated in Figure 4.1. The proposed circuit has floating inductance behavior, which is a valuable feature that expands the circuit's application area. The bidirectional arrows indicate that the transistors in the core circuit may be

either PMOS or NMOS as both transistor types have an identical small-signal equivalent model. Considering this information, it may seem possible to create 2^n different circuits; however, some are not applicable due to bias constraints. As a result, one or more circuits can be designed with the same small-signal characteristics of the core circuit and can be properly biased.

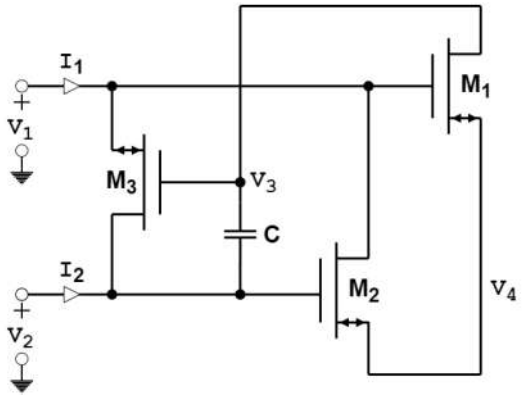


Figure 4.1. The core circuit of the proposed AI.

Replacing MOS transistors with their small-signal models, and when the KCL equations of the AI circuit are solved, the equivalent inductance of the proposed circuit can be calculated as

$$L_{\text{act}} = \frac{C}{(g_{\text{m3}})^2}, \quad \text{if} \quad g_{\text{m3}} = \frac{g_{\text{m1}} g_{\text{m2}}}{(g_{\text{m1}} + g_{\text{m2}})}. \tag{4.2}$$

which shows that g_m values of the transistors M_1, M_2, and M_3 should be adjusted together to avoid disturbing the inductive behavior.

The proposed core circuit must be properly biased for the actual design so that transistor behavior similar to that of the small-signal representation is obtained. Thus, the transistor sizes and tail currents should be adjusted to guarantee that all transistors operate in saturation within the specified operating range. For this design, M_1 and M_2 transistors are chosen as NMOS due to the high speed of the NMOS type. Then,

M_3 transistor is selected as PMOS due to proper bias need. Figure 4.2 represents the biased version of the proposed circuit in differential (floating) form. While the proposed core circuit is a floating inductor, an AI is created by joining two core circuits at their V_1 nodes. This eliminates DC offset between the inductor's ports. Additionally, the differential circuit performs better in terms of the percentage total harmonic distortion (%THD) than the core circuit. Transistors M_1, M_2, and M_3 are the same as shown in Figure 4.1. Moreover, transistors M_4 and M_5 are added to the circuit for DC shifting purposes for proper biasing.

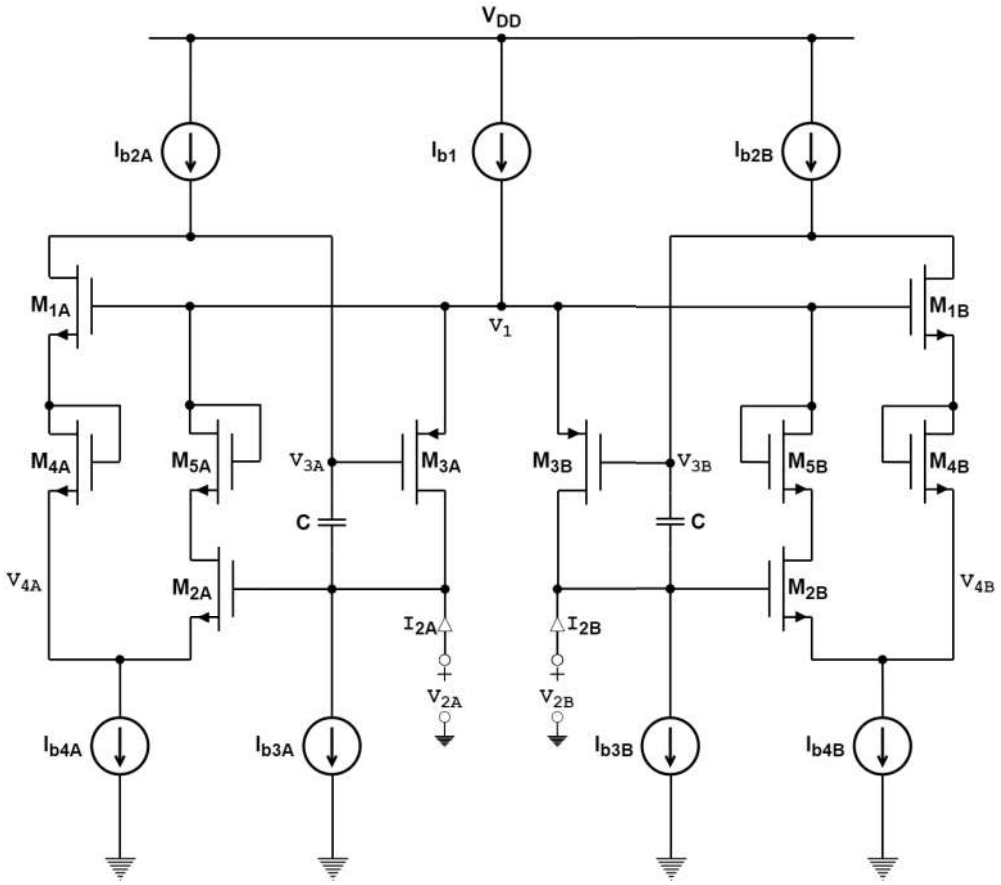


Figure 4.2. The biased version of the proposed AI circuit.

Taiwan Semiconductor Manufacturing Company (TSMC) 65 nm process design kit (PDK) with a core supply voltage of 1.2 V was preferred in this study. This supply voltage is appropriate in terms of power consumption (P_{dc}) and the lifetime of the

transistors. On the other hand, however, it restricts the number of transistors that can be stacked. As seen in Figure 4.2, there are three distinct lines between power and ground where transistors are stacked: the line of M_1, M_4, I_{b2}, I_{b4}; the line of M_2, M_5, I_{b1}, I_{b4}; and the line of M_3, I_{b1}, I_{b3}. Given that each of the current sources from I_{b1} to I_{b4} are implemented using a single transistor current mirror, the total number of stacked transistors for each line is not more than four, which is suitable for low voltage operation.

The parasitic capacitances and finite output impedances of the transistors are not taken into account when obtaining Equation (4.2). However, especially the large size of the transistor strengthens the parasitic effects. This causes the designed circuit to deviate from the calculated inductive behavior. In the useful frequency range, the behavior of the designed active inductor fits to the model in Figure 4.3. The computed corresponding values are listed in Section 4.3.

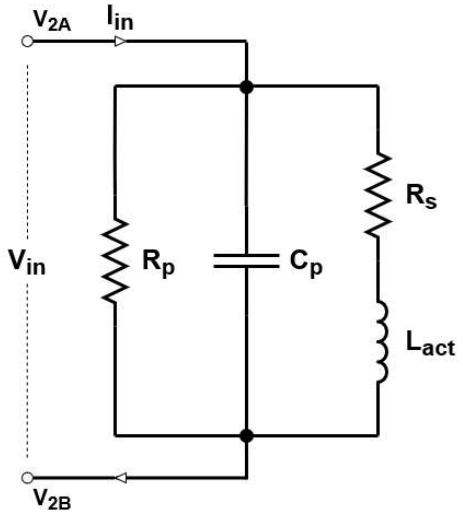


Figure 4.3. The equivalent RLC network of the lossy gyrator-C-based FAI.

The second chapter of [10] delves into small-signal analyses of gyrator-C networks and the parasitic effects on their inductive behavior. While designing the active AI for this design, attention will be paid to the points highlighted in [10].

In the proposed system shown in Figure 4.1, the main reason for R_p is the impedance seen from V_2 node when V_1 node is grounded, that is, the output impedance of the transistor M_3. Thus, in applications requiring a high-Q value, the R_p value can be enhanced by reducing the current flowing through M_3. On the other hand, decreasing current can reduce the g_{m3} value, hence raising the equivalent inductance of the circuit. Therefore, in circuits where low inductance is required, a trade-off between lowering the inductance value and increasing the Q value may occur.

The value of R_s is another factor that distracts AIs from their ideal behavior. The R_s value is inversely proportional to the g_{m3} value and the impedance seen from V_1 node. The other non-ideal component of the AI is C_p capacitance. C_p can be defined as the equivalent capacitor from AI input to the ground.

As highlighted above, a change to improve one of the non-ideal components of AIs may affect other parts. Thus, it is required to examine all parameters and improve in an iterative manner. This situation necessitates the use of advanced simulation environments. In this study, the Spectre Simulation Platform is used for circuit optimization. The impedance, inductance value, and quality factor graphs of the designed inductor circuit are given in Figure 4.4. The inductance values are calculated by taking the derivative of the imaginary part of the impedance graph. The quality factor is obtained by dividing the imaginary part of the impedance value by the real part.

4.3. LC-VCO Design

This Section explains the design of an LC-VCO circuit with the novel FAI suggested in the preceding section. While Section 4.3.1 discusses the preferred LC-VCO topology, Section 4.3.2 discusses the design approach and issues to consider throughout the design.

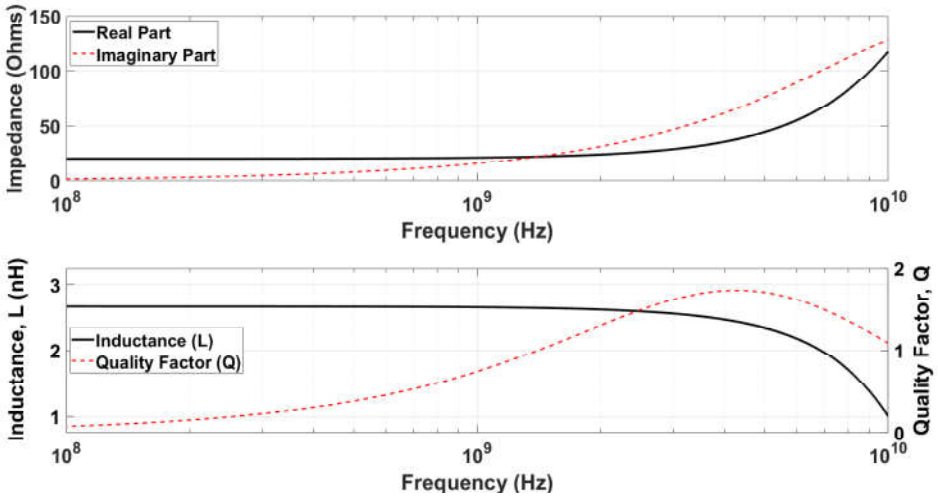


Figure 4.4. Characteristics of the proposed FAI.

4.3.1. Circuit Topology

The conventional LC-VCO structures include four categories of devices: inductors, capacitors, cross-coupled transistors, and current sources. Numerous alternative topologies have been proposed depending on the location of the inductors, types of cross-coupled transistors, and tail currents. To keep the chapter short, a comparison of various VCO topologies is not discussed here. Detailed information about comparing several architectures can be found in [40–42]. The suggested design employs a bottom-biased NMOS cross-coupled LC-VCO topology due to its superior high-frequency behavior and compatibility with AI applications as depicted in Figure 4.5.

The detailed schematic of the designed LC-VCO is presented in Figure 4.6. Transistors $M_{1A,B}$–$M_{5A,B}$ form the biased version of the proposed FAI, and transistors M_6, $M_{7A,B}$ and $M_{8A,B}$ correspond to the current sources I_{b1}, $I_{b2A,B}$, and $I_{b3A,B}$, respectively, as illustrated in Figure 4.2. As different from the Figure 4.2, cross-coupled transistors M_9 and M_{10} are inserted between the FAI ports and the current sink transistor M_{11}. As illustrated in Figure 4.6, the total number of stacked transistors in any line does not exceed four after the addition of cross-coupled transistors. This demonstrates that the final design will also work in a low-supply environment.

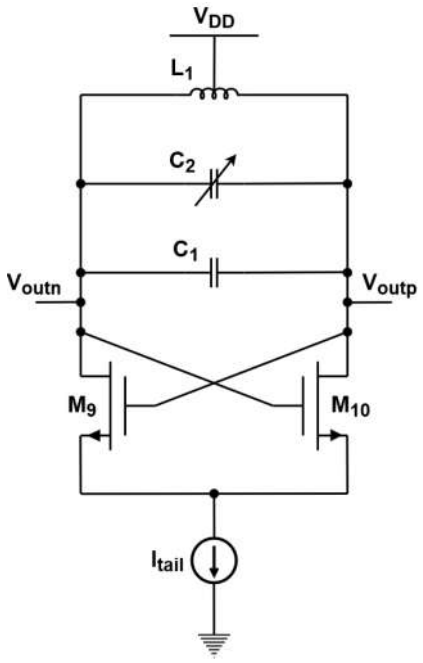


Figure 4.5. Bottom-biased NMOS cross-coupled LC-VCO scheme.

4.3.2. Design Procedure

In this section, an LC-VCO will be designed, working at 2.4 GHz–3.8 GHz with a $V_{\mathrm{DD}} = 1.2$ V supply voltage. In low-voltage systems, it is necessary to pay close attention to the number of stacked transistors to prevent headroom issues. As explained in Section 4.2, the proposed FAI is suitable for operation at low supply voltage. Due to the high operating frequency, short channel devices manufactured in the TSMC 65 nm technology were chosen for the design. Moreover, by designing a system in which both varactors and tail currents can control the operating frequency, the oscillator is provided to cover a wide frequency range. The remainder of this section describes the procedure for selecting VCO design parameters.

When designing classical LC-VCO structures with spiral inductors, the needed tail current and inductor $\mathrm{R_p}$ value are determined by considering the power budget and desired output voltage swing. It is vital to avoid exceeding a particular output swing in these systems, as there is a risk of cross-coupled transistors entering the

triode region. At this point, the FAI-based oscillator architecture used in this study is distinct from conventional structures. First, because the dynamic range of FAIs is already limited to a few tens of mV, it will not be sufficient to affect cross-coupled transistors. Secondly, as illustrated in Figure 4.6, the tail current of the oscillator affects the characterization of the inductor since it is also the bias current of the FAI. Thus, the required tail current and R_p value cannot be determined independently of each other. As a result, the inductance value required to achieve the target oscillation frequency will be determined first. Then, when the FAI reaches the appropriate inductance value at the defined frequencies, the required R_p value is determined to ensure that it does not exceed the dynamic range of the FAI.

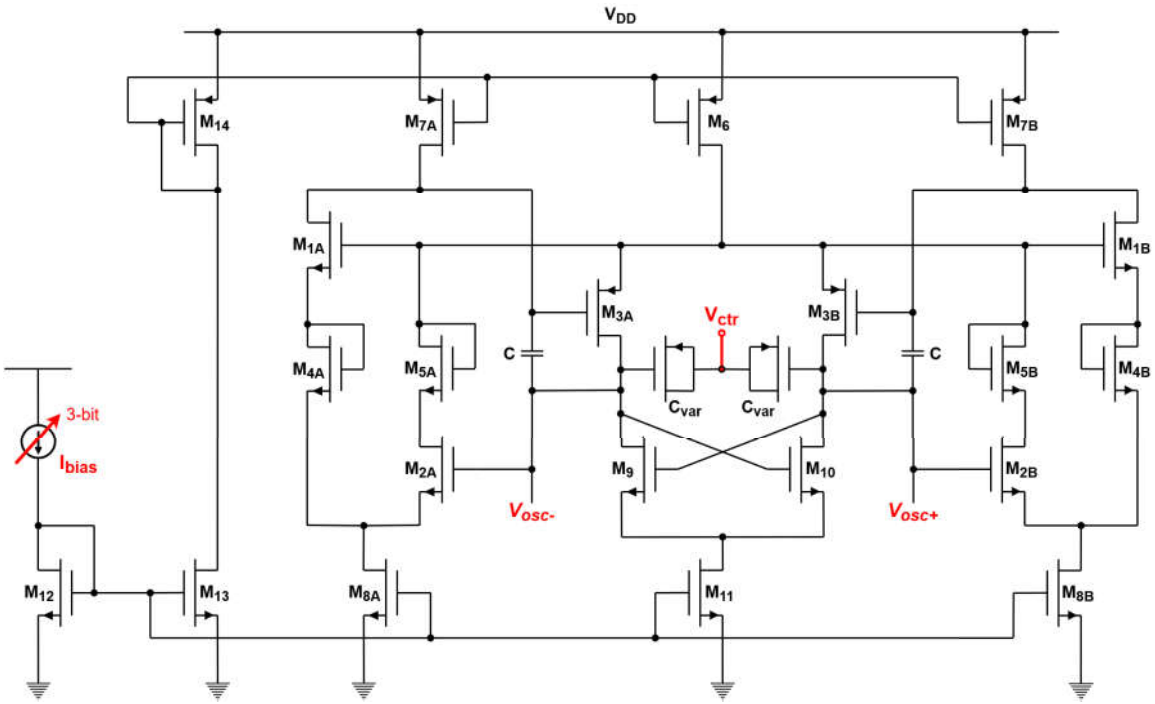


Figure 4.6. The detailed schematic of the designed LC-VCO.

The oscillation frequency equation of an LC-tank is as follows:

$$f_{\text{osc}} = \frac{1}{2\pi\sqrt{L_1 C_1}}, \tag{4.3}$$

while L_1 and C_1 are equivalent inductance and capacitance values of the LC-tank. When the equivalent capacitance of the LC-tank is assumed to be 1 pF, an inductance of around 2.8 nH is required for a 3 GHz oscillation. After allocating 300 fF of the tank's 1 pF equivalent capacitance to the varactor, the remaining part can be allocated to the FAI capacitances in two 350 fF halves as illustrated in

$$C_1 = C_{\text{var}} + 2C_{\text{ind}}, \tag{4.4}$$

while C_{var} represents the capacitance of the varactor and C_{ind} represents the capacitance seen from the ports of each FAI.

Then, considering Equation (4.2), the value of g_{m3} should be roughly 9 mS to achieve the desired inductance value in the proposed FAIs. It is sufficient to flow 1 mA current through $M_{3A,B}$ transistors to obtain desired g_{m3} value. The high current flowing through the $M_{3A,B}$ transistor reduces the R_p value of the FAI, hence the Q value of the inductor. However, this is not a problem for the LC-VCO design, as the output swing must be kept low due to the dynamic range constraint of the FAI.

Table 4.1. Parameters of the designed FAI for the $Cluster_{100}$ case.

Parameter Type	**Value**
Inductance, L_1 ($= L_{\text{act}}$)	2.55 nH
Quality Factor, Q	1.52
Parallel Resistance, R_p	567 Ω
Parallel Capacitance, C_p	350 fF
Series Resistance, R_s	12.17 Ω
Power Consumption (P_{dc})	9.6 mW

The approximate calculations described previously have been taken into account and the FAI has been designed with the parameters necessary to achieve the desired oscillation conditions. The bias current of the FAI is tuned in the designed LC-VCO to cover many frequency ranges referred to as clusters. As a result, the FAI's characteristics may vary between clusters. The parameters associated with the $Cluster_{100}$ state, which we can define as the nominal case, are listed in Table 4.1. The inductance (L_1) and quality factor (Q) values in this table are for the nominal oscillation frequency of 3.105 GHz. Additionally, the inductor's impedance-frequency responses for the nominal case are shown in Figure 4.4 in Section 4.2.

After obtaining the basic parameters related to the FAI, the design phase of the cross-coupled transistors was started. In order to guarantee that the oscillation will occur despite the non-ideal effects in the devices, the transconductance values of the cross-coupled transistors should be determined as follows:

$$g_{\mathrm{m9,10}} \geq \frac{3}{R_{\mathrm{p}}}. \tag{4.5}$$

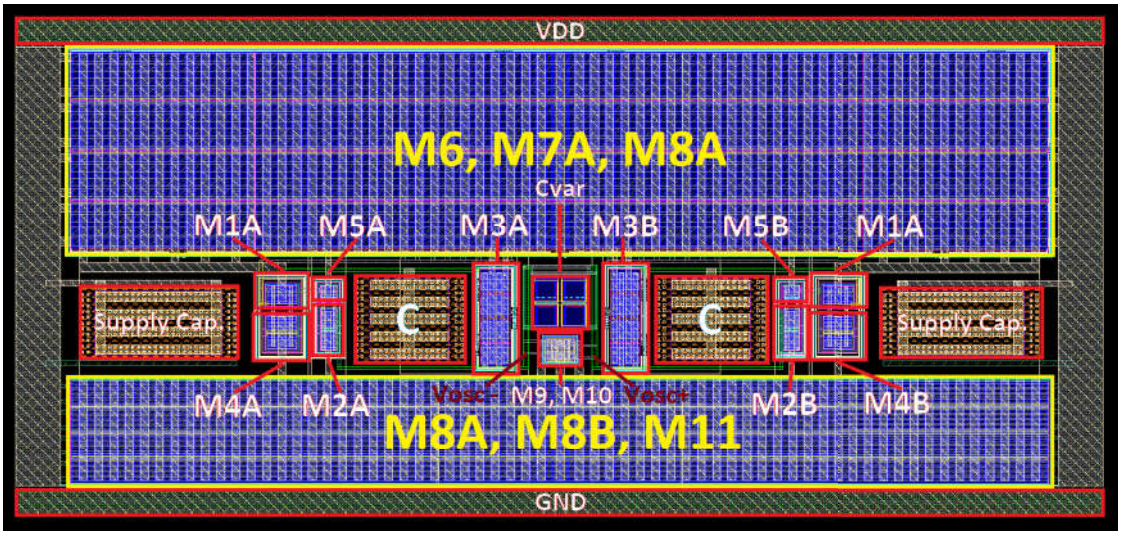


Figure 4.7. The layout of the designed LC-VCO.

Table 4.2. Aspect ratios of the transistors in the designed LC-VCO shown in Figure 4.6.

Transistor	**Width (W)**	**Length (L)**
M_{1A}, M_{1B}, M_{2A}, M_{2B}	40 μm	60 nm
M_{3A}, M_{3B}	204.8 μm	60 nm
M_{4A}, M_{4B}	57.6 μm	60 nm
M_{5A}, M_{5B}	10 μm	60 nm
M_6	2240 μm	1 μm
M_{7A}, M_{7B}	672 μm	1 μm
M_{8A}, M_{8B}	614.4 μm	1 μm
M_9, M_{10}	16 μm	60 nm
M_{11}	409.6 μm	1 μm
M_{12}, M_{13}	51.2 μm	1 μm
M_{14}	112 μm	1 μm

When the bias current is reduced for different cluster values, the R_p value will increase, and the transconductance values of the cross-coupled transistors will decrease. Thus, setting the transconductances slightly higher for the nominal case would be more robust. Considering this situation, the transconductances of transistors M_9 and M_{10} are determined as 5 mS. The transistor dimensions of the LC-VCO are listed in Table 4.2. The layout of the designed circuit is about 170 μm $\times$ 80 μm in size, as illustrated in Figure 4.7. If a spiral inductor was preferred in this design, a 180 μm $\times$ 160 μm structure as in Figure 4.8 would be needed. The inductor shown in Figure 4.8 was created using the inductance finder tool of the PDK, with a focus on minimizing the silicon area. Thus, it was attempted to enhance the inductance value by increasing the number of turns at the expense of obtaining a low quality factor. However, only the inductor alone has approximately twice the space of the LC-VCO layout shown in Figure 4.7. For the spiral inductor case, With the addition of current mirrors and capacitors, the consumed area will be more than twice that of the designed LC-VCO.

As seen in this example, the application of FAI is extremely cost effective in terms of silicon area.

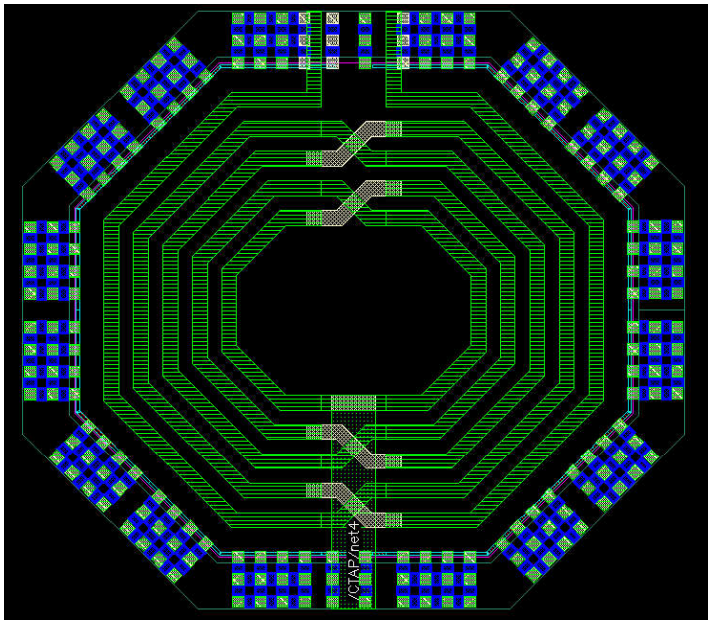


Figure 4.8. The spiral inductor with the same inductance value as the FAI used in the designed LC-VCO.

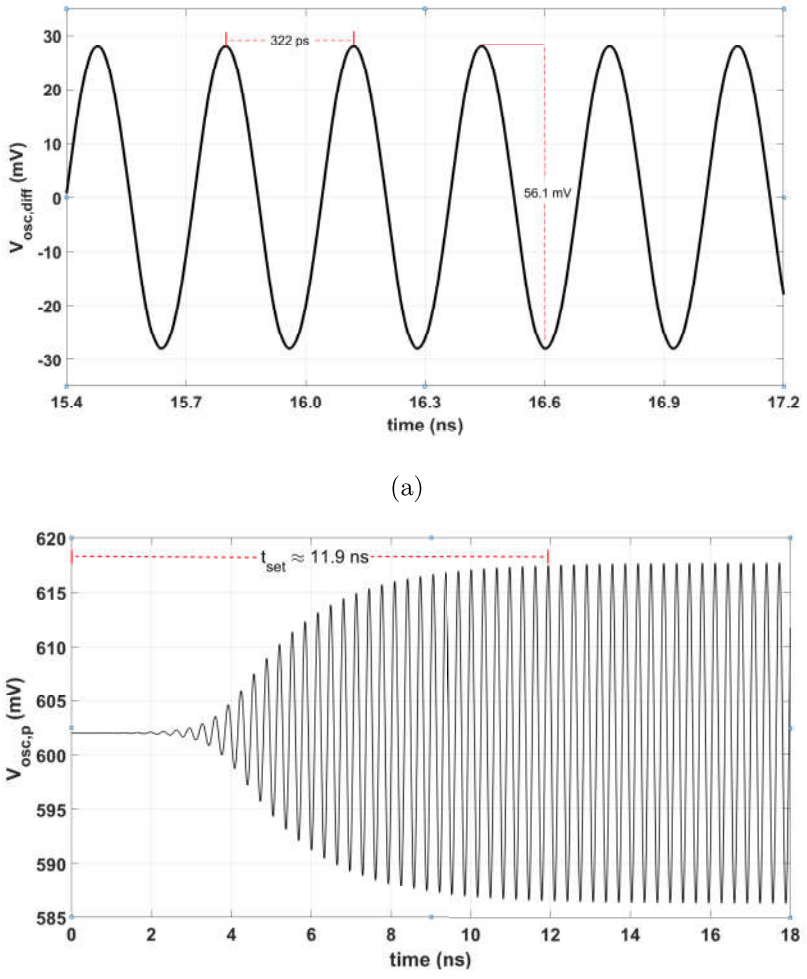
4.4. Simulation Results

To verify the circuit performance, the FAI and the LC-VCO are simulated using Cadence Design Suite in a TSMC 65 nm CMOS process. Parasitics from the layout are also considered in the simulations. The supply voltage is set to 1.2 V to minimize power consumption and enable the use of high-speed transistors in the process.

4.4.1. LC-VCO Dynamic Range and Phase Noise Analysis

Transient simulation results of the designed LC-VCO are shown in Figure 4.9(a). The oscillation occurs at 3.105 GHz with a differential amplitude of 56.1 mV. Moreover, the oscillator needs about 11.9 ns of settling time to start oscillating at the expected amplitude, as shown in Figure 4.9(b). Additionally, the THD value of 3.47% was

simulated. These simulation results were obtained when the circuit was in $Cluster_{100}$ state and analog control voltage of the varactor (V_{ctr}) was set to 1 V. Dynamic range is one of the most frequently noted shortcomings of AIs in the literature. Various studies have been conducted on this subject and numerous approaches have been explored as [15]. As previously stated, the narrow output voltage swing caused by the dynamic range limiting simplifies the LC-VCO design process. However, this poses a serious problem with the phase noise characteristics of the oscillator. The phase noise of an LC-VCO is inversely proportional to its amplitude, as it is clearly stated in [43], which includes an in-depth analysis of the phase noises of LC-VCOs.



(a)

(b)

Figure 4.9. (a) Differential output. (b) Settling time of the oscillator.

The phase noise characteristic of the designed circuit is shown in Figure 4.10. The LC-VCO, with a noise level of –80.22 dBc/Hz at a frequency offset of 1 MHz, appears to be insufficient for use in communication circuits where phase noise is crucial. However, it can be an acceptable trade-off for digital circuits where phase noise is not a key factor. To enable the usage of AIs in communication circuits, studies on the dynamic range should be accelerated. This is an excellent subject for further research.

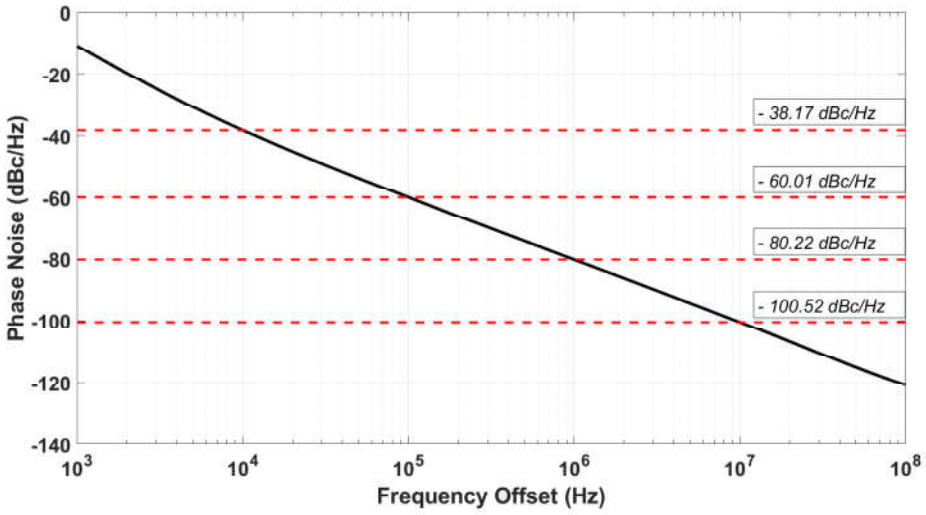


Figure 4.10. Phase noise of the designed oscillator.

4.4.2. Rail-to-Rail Output Swing Improvement

Although AIs significantly cut silicon costs, their small output swings make them unsuitable for LC-VCO designs. Here we introduce a system that transforms the oscillator output to rail-to-rail for applications where the phase noise performance of AI-based oscillators is adequate but not desirable due to the low output swing. Thanks to the buffer circuit whose schematic is given in Figure 4.11, the differential 56.1 mV signal swing obtained at 3.105 GHz can be increased to rail-to-rail by increasing the current consumption and silicon area a little more. The oscillator output is sensed using the capacitive coupling technique in the first stage of the buffer circuit, which isolates the signal from the common-mode voltage. When the C_{coup} value is set to 500 fF

and the R_{B1} and R_{B2} values are set to 60 kΩ, the desired sensing at the appropriate frequencies can be accomplished. Additionally, R_{B3} value is set to 600 Ω to bias the transistor M_{B1} properly. However, since the 28 mV signal amplitude is insufficient to drive the following inverter, it is first boosted in the second part using a simple common source amplifier. Finally, the circuit is terminated with three successive buffers. Thanks to these buffers, the driving strength of the entire circuit is raised while the common source amplifier's load is decreased. The buffer sizes here can be customized for varied loads depending on the application area in which the oscillator will be employed.

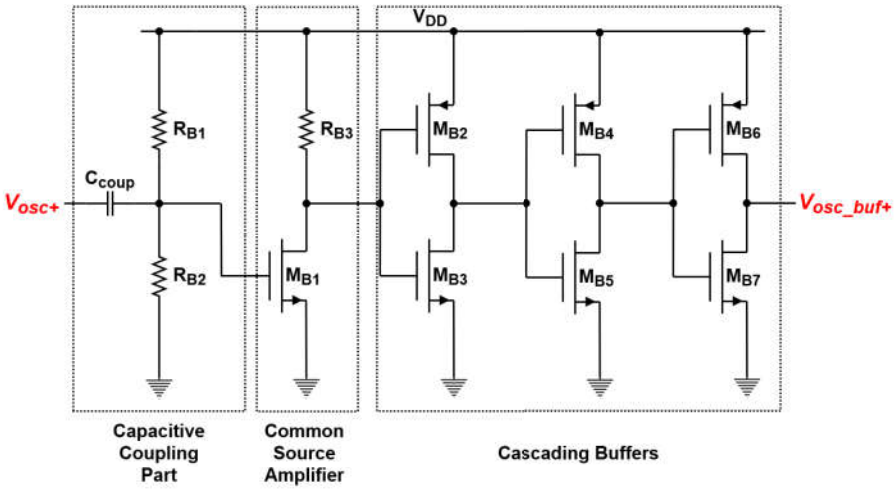


Figure 4.11. The buffer schematic for rail-to-rail oscillation.

To operate properly in the 3 GHz frequency, the buffer circuit requires around 1.25 mA current. Since two buffers will be utilized for the oscillator's positive and negative ends, the overall current consumption will increase by roughly 2.5 mA, consuming 0.006 mm^2 silicon area. While simulations have proven that the buffer circuit works, they are not included in the post-layout results to allow for a fair comparison to published studies. The transistor dimensions of the buffer are listed in Table 4.3.

Table 4.3. Transistor dimensions of the buffer shown in Figure 4.11.

Transistor Name	**Width (W)**	**Length (L)**
M_{B1}	24 μm	60 nm
M_{B2}, M_{B5}	1.2 μm	60 nm
M_{B3}	600 nm	60 nm
M_{B4}, M_{B7}	2.4 μm	60 nm
M_{B6}	4.8 μm	60 nm

4.4.3. Frequency Tuning Mechanism

As discussed previously, this design utilizes a tuning mechanism to ensure that a broad frequency range is covered. Within each cluster, a frequency range of about 300 MHz is spanned by changing the V_{ctr}. In addition, the bias current of the AI can be controlled digitally. The bias current (I_{bias}) of the circuit consists of a fixed current source of 170 μA, and digital controllable current sources with 20, 40 and 80 μA values. Thus, the bias current can be changed in increments of 20 μA between values of 170 μA and 310 μA. The tail current of the inductor is generated by mirroring I_{bias} current. While the I_{bias} is 250 μA in nominal condition, the oscillator consumes 8.5 mA. The overall current usage increases to 10.54 mA when the I_{bias} current is set to 310 μA for higher frequencies.

Figure 4.12 illustrates the simulation results of the control mechanism with 3-bit digital control, that is, with 8 different clusters. While V_{ctr} voltage is tuned to get various frequency values on each curve, I_{bias} current is digitally controlled to create transitions between the clusters. The circuit can continue to operate in this work when the bias current is varied between 170 μA and 310 μA. This way, a VCO operating between 2.4 GHz and 3.8 GHz was obtained. The percentage tuning range (PTR), which is expressed as the ratio of the difference between the higher frequency and lower frequency to the mean oscillation frequency (TR/$f_{\text{osc-mean}}$), is calculated as 45.16%. If wider tuning range is needed, more clusters can be obtained by increasing the number

of digital bits. But in such designs, care must be taken that the inductive behavior of the AI does not deteriorate with the change of the bias current.

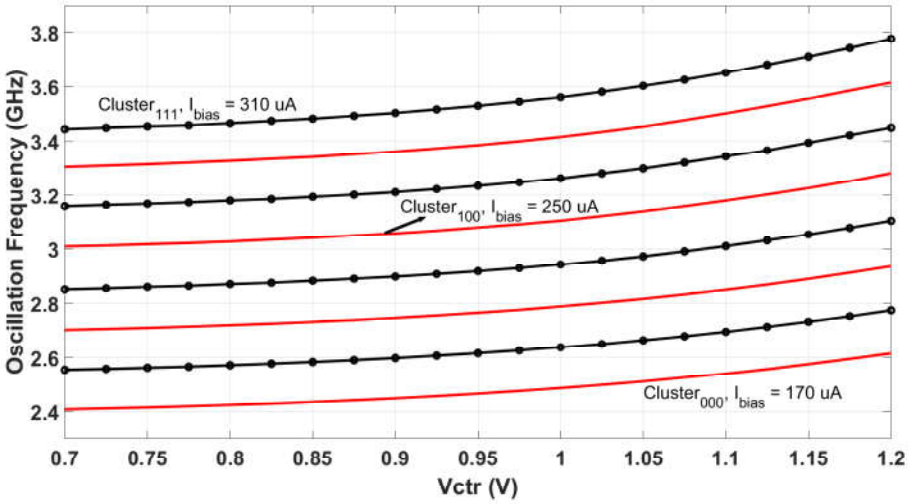


Figure 4.12. Oscillation frequency versus control voltage for each 8 clusters.

This tuning mechanism is extremely useful in devices such as PLLs, where the VCO's frequency is tuned and locked to the target value. To begin, the correct frequency value will be sought by adjusting the V_{ctr} voltage; if the V_{ctr} voltage is insufficient, the I_{bias} will be adjusted to toggle between clusters. In the case of certain changes in circuit behavior caused by non-ideal effects, distinct clusters were constructed to overlap by approximately 15% to ensure that no frequency values were missed during these transitions.

Spiral inductors, frequently used in classical LC-VCO topologies, cannot have tunable inductance values. Therefore, they may be insufficient in applications where a wide frequency range is covered such as the one described in this work. Traditionally, digitally-controlled capacitor bank architectures are favored for this reason [44]. Capacitor banks use a significant amount of silicon and complicate the layout due to matching requirements.

4.4.4. Literature Comparison and a Brief Discussion

The designed circuit's performance is presented in Table 4.4, along with data from state-of-the-art LC-VCO implementations [12, 21, 32–34, 45, 46]. Three figures of merits (FOMs), defined in [33], are used to compare the circuit performance. As seen in the table, the FoM values of the proposed circuit are slightly higher than those in the literature. However, the designed circuit is in a better position than the studies in the literature at a few points where the FoM values used do not show. Firstly, the consumed silicon area by the proposed VCO is considerably less than the other studies, which decreases the production cost. Additionally, this study is distinguished from others in the literature by the rise in operation speed to the 3.8 GHz band. Thirdly, 1.2 V supply voltage makes the proposed circuit applicable for advanced node CMOS processes. Furthermore, current consumption is well within the acceptable range in the literature and it has a reasonable output power (P_{out}) for VCOs designed with an AI [21, 32, 34, 45]. Further, as shown in Table 4.4, the phase noise performance of the designed FAI-based oscillator is the same as in [45] but limited compared to spiral inductor-based structures [46].

Table 4.4. Comparing the designed LC-VCO with the literature.

	This Work	**[21]**	**[45]**	**[32]**	**[46]**	**[33]**	**[12]**	**[34]**
Inductor Type	Active	Active	Active	Active	Passive	Active	Active	Active
CMOS Process (nm)	65	180	180	130	32	180	45	180
Power Supply (V)	1.2	1.8	1.8	1.2	1.8	1.8	±1	1.8
Oscillation Frequency (GHz)	2.4 ∼ 3.8	0.5 ∼ 3	0.5 ∼ 2	0.83 ∼ 3.72	3.3 ∼ 4	0.5 ∼ 2.8	1.1 ∼ 1.8	0.5 ∼ 3.6
Tuning Range (%)	45.16	142.86	120.00	127.03	19.18	139.4	48.27	151.2
Phase Noise (dBc/Hz) @1 MHz Offset	–80.22	–109.5	–84	–106.5	–125.0	–93.5	–98.37	–100.0
Output Power (dBm)	–19.3 ∼ –24.7	–14 ∼ –22	–20.8 ∼ –29	–0.9 ∼ –5	–	7.54	5.00	–17.89
Power Consumption (mW)	6.94 ∼ 12.6	6 ∼ 28	13.8	13	8.4 ∼ 11.2	5.3	1.1	8.1 ∼ 24.3
Area (mm^2)	0.013	0.045	0.09	0.108	0.238	0.030	0.002	0.018
FoM_1 (dBc/Hz)	–140.0	–156.8	–140.2	–154.9	–185.5	–154.4	–163.1	–149.5
FoM_2 (dBc/Hz)	–150.1	–171.2	–151.6	–166.0	–196.2	–161.6	–163.5	–163.4
FoM_3 (dBc/Hz)	–153.1	–179.9	–161.8	–177.0	–191.0	–177.2	–176.7	–173.1

4.5. Chapter Summary

An LC-VCO with a novel FAI was designed in this chapter. Designed with TSMC 65 nm PDK, the suggested VCO operates at a 2.4 to 3.8 GHz frequency range. It has a broad frequency range due to the introduced tuning mechanism that takes advantage of the FAI's tunability. The VCO shows a –80.22 dBc/Hz phase noise @1 MHz offset, and it has a THD value of 3.47% for the nominal case. This circuit consumes 10.2 mW of power when operated at a 1.2 V supply at the nominal case. Due to the use of an FAI rather than a spiral inductor, this is an area-efficient design with low power usage. It covers an area of 0.013 mm^2, significantly less than the literature. Owing to the use of transistors rather than spiral inductors, it has a low phase noise performance. The output swing is limited due to the dynamic range issue, valid for all AI-based solutions in the literature. However, because it operates at a low supply voltage and features a tuning mechanism that enables a wide frequency range, it may be preferable in systems where phase noise is not a significant concern. Future work will focus on improving the phase noise of AI-based VCO circuits.

5. A 4-BITS ACTIVE INDUCTOR-BASED LATTICE 24.5−50 PS ALL-PASS FILTER DESIGN FOR 5G APPLICATIONS

5.1. Chapter Introduction

Analog filters that pass all frequencies equally in amplitude but shift their phases are called all-pass filters (APFs). While most filters reduce the amplitude of the input signal at specific frequencies, APFs allow all frequencies to pass through without affecting the magnitude. They are essential components in analog signal processing applications of the fifth-generation (5G) communication system core blocks, such as quadrature oscillators [47], true-time delay cells [48], beamforming applications [49,50], and phase-locked loops [51], among others. APFs are designed to provide adjustable group delays in these applications to account for relative delay variations between different signal lines. As different regions have different spectrum availabilities, different bands have been rolled out for auction across the globe, as summarized in [52–54].

Due to the high silicon consumption problem of spiral inductors [24], inductor-less APFs are preferred in low-frequency applications. In this direction, current conveyor-based APF circuits are summarized in [55]. Although the presented studies obtained a high input impedance critical for filters, the operating frequencies of the topologies employed were limited to a few MHz. For this reason, researchers working toward 5G applications for the next-generation communication systems favored simple circuits with a small number of active elements over complex architectures. For instance, the circuit in [56] is a gm-RC-based first-order APF that operates at the $1 - 2.5$ GHz frequency. The primary drawback of this circuit is that it consumes a large amount of current. On the other hand, higher-order APF circuits are suggested in [57, 58]. These circuits operate across a wide frequency range, but require a large silicon area to achieve the required inductance value because they incorporate spiral inductors. Additionally, spiral inductors have low and non-tunable quality factors. These are the

significant obstacles to obtaining tunable APF circuits. However, as discussed in [59], symmetrical lattice networks are suitable for APF designs. It is feasible to build a lattice network circuit to be a constant-resistance network for a wide variety of circuit properties. Furthermore, higher-order filters can be built by cascading lattice filter structures. However, because lattice structures contain many inductors, they share the problems of spiral inductors discussed above. In this work, we designed an APF based on a lattice structure and employed floating active inductors (FAIs) rather than spiral inductors. In this approach, we avoided the space requirements associated with spiral inductors and acquired inductors with quality factors that spirals cannot achieve. Additionally, we achieved configurable quality factor and inductance values, another advantage of the active inductor circuits.

The chapter is arranged as follows: Section 5.2 discusses the procedure of deriving the required lattice filter's transfer function and determining the appropriate component values for the acquired transfer function. In Section 5.3, the architecture and design procedure of the FAIs which will be utilized in the designed APF are introduced. Section 5.4 presents the design optimization and the post-layout simulation results of the designed APF. Performance comparison with the state-of-the-art reported APFs is reported in Section 5.5. Finally, Section 5.6 concludes the study and discusses future work.

5.2. Description of the Lattice All-Pass Filter Topology

As shown in Equation (5.1), the numerator and denominator of the transfer function of APFs that simply shift the phase of the input signals without affecting their amplitudes are symmetrical with respect to the y-axis. Thus, it is sufficient to determine the transfer function of APFs by determining the denominator polynomial $E(s)$ as shown in

$$H(s) = \frac{E(-s)}{E(s)}. \tag{5.1}$$

Numerous studies have been published in the literature in an attempt to determine the denominator function $E(s)$ [59,60] (and references cited therein). In this study, we will compute it using the approach proposed in [60] as illustrated in Figure 5.1.

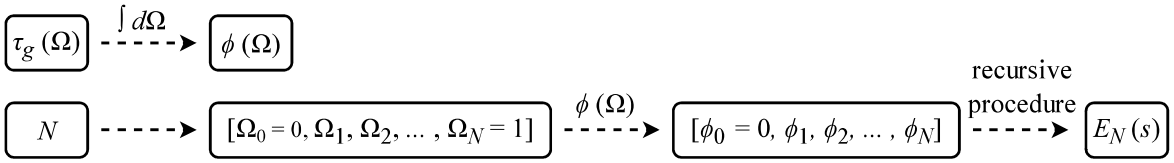


Figure 5.1. Flow graph of the procedure to generate the prototype all-pass filter denominator $E_n(s)$.

In Figure 5.1, $\tau_g\ (\Omega)$ denotes the group delay function, where Ω is the normalized frequency [59]. Ω can take a value between 0 and 1, as it indicates the normalized frequency. The numbers 0 and 1 here denote the circuit's operational frequency boundaries. The design procedure begins with determining the desired $\tau_g\ (\Omega)$ function. Then, by integrating this function with respect to the normalized frequency, the associated phase function $\phi\ (\Omega)$ is produced. The N in Figure 5.1 indicates the filter order. Over this N value, $N + 1$ normalized frequency values are calculated. The resulting normalized frequency values are then used to generate the phase function $\phi\ (\Omega)$ outputs. These acquired values are utilized to construct the $E(s)$ function through the individual equations

$$E_n(s) = \begin{cases} 1, & n = 0, \\ s + \alpha_0, & n = 1, \\ \alpha_{n-1}E_{n-1}(s) + (s^2 + \Omega_{n-1}^2)E_{n-2}(s), & n \geq 2, \end{cases} \tag{5.2}$$

$$\alpha_i = \begin{cases} \dfrac{\Omega_1}{\tan\phi_1}, & i = 0, \\ \cfrac{\Omega_{i+1}^2 - \Omega_i^2}{\alpha_{i-1} - \cfrac{\Omega_{i+1}^2 - \Omega_{i-1}^2}{\alpha_{i-2} - \cfrac{\Omega_{i+1}^2 - \Omega_{i-2}^2}{\ddots \cfrac{}{\alpha_0 - \cfrac{\Omega_{i+1}}{\tan\phi_{i+1}}}}}}, & i \geq 1. \end{cases} \tag{5.3}$$

Note that if the specified filter order cannot produce the desired delay response, the procedure is repeated with a different filter order or by adjusting the desired delay response function.

The purpose of this work is to design a second-order lattice network-based APF with the group delay response stated as

$$\tau_g\ (\Omega) = A\Omega + \tau_0 = -0.001\Omega + 0.9, \tag{5.4}$$

where A is the angular coefficient and Ω is the normalized frequency. Coefficient A is used to express the magnitude and sign of the phase slope. Then, τ_0 is a constant term of the desired group delay response, which is crucial in determining the filter's realizability. The transfer function generated by the initial coefficients A and τ_0 values may be unstable, or the components required to generate it may be incompatible with the complementary metal-oxide-semiconductor (CMOS). When this occurs, the coefficients should be modified, and the filter design procedure should be repeated with the updated coefficients.

For this design, a minimal group delay deviation has been taken into account when selecting the coefficients A and τ_0 values given in Equation (5.4). If a large phase shift throughout a wide range is desired, a larger coefficient can also be used. The lattice topology offers flexibility to the designer for different applications in this regard. When the desired group delay function described in Equation (5.4) is supplied as an input to the procedure illustrated in Figure 5.1, the denominator $E_n(s)$ is calculated as

$s^2 + 6.223s + 8.443$. Then, the transfer function generated as a result of the obtained $E_n(s)$ polynomial can be stated as

$$H(s) = \frac{E(-s)}{E(s)} = \frac{s^2 - 6.223s + 8.443}{s^2 + 6.223s + 8.443}. \tag{5.5}$$

In this study, we will use a lattice network to implement the APF structure, whose transfer function is indicated in Equation (5.5). Three major considerations influenced the lattice topology used for this research. To begin, it is an intrinsically balanced structure. Second, for a broad variety of circuit properties, it is possible to construct a lattice network circuit that is a constant-resistance network. Finally, higher-order filters may be designed by cascading lattice filter architectures. The schematic of the second-order lattice filter to be implemented is given in Figure 5.2.

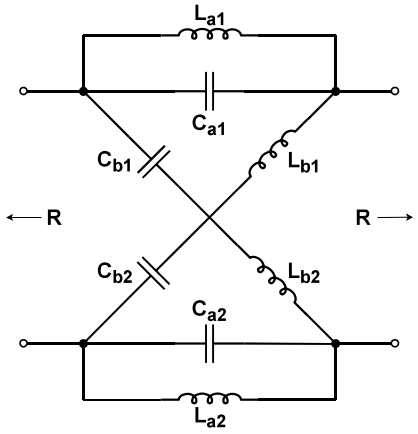


Figure 5.2. The schematic of the second-order lattice all-pass network.

To derive the component values of the second-order lattice APF network, its transfer function coefficients can be used. Firstly, prototype filter component values will be found, followed by the impedance and frequency scaling to determine the final values. The prototype component values can be calculated by using the equations $L_\mathrm{a} = C_\mathrm{b} = \frac{a}{b}$, $C_\mathrm{a} = L_\mathrm{b} = \frac{1}{a}$, while the APF transfer function is written as

$$H(s) = \frac{s^2 - as + b}{s^2 + as + b}. \tag{5.6}$$

Table 5.1. Component values of the proposed lattice filter.

Component Name	**Component Value**	
	Prototype	*Scaled*
L_{a}	0.4735 H	1.047 nH
C_{a}	0.1184 F	104.66 fF
L_{b}	0.1184 H	261.60 pH
C_{b}	0.4735 F	418.64 fF

The prototype component values required for the proposed lattice filter are determined using the transfer function defined in Equation (5.5). Table 5.1 contains the calculated prototype values with their scaled versions for 50 Ω impedance and 3.6 GHz frequency. The nominal frequency is determined to be 3.6 GHz since it is in the middle of the $3.4 - 3.8$ GHz band, which is assigned to 5G technologies in most countries [52–54].

Examining the capacitance and inductance values in Table 5.1, it is evident that they are suitable for CMOS implementation. P-channel MOS (PMOS) varactors can be selected to implement C_{a} and C_{b} components since they provide tuning capability, which is needed to make the designed APF programmable. On the other hand, unlike earlier studies in the literature, such as the one in [59], FAIs are used rather than spiral inductors to implement the required inductors in the lattice filter architecture. The manufacturing cost of the designed circuit is reduced thanks to FAIs that consume less silicon area than their spiral counterparts. Additionally, since FAIs have tunable quality factors and inductance values, the proposed filter's operating frequency range may be maintained relatively wide. The following section discusses the FAIs employed in the designed lattice filter.

5.3. Proposed Floating Active Inductors (FAIs)

In this APF design, FAIs should be capable of operating at frequencies up to 3.8 GHz, which is the frequency spectrum allocated by several nations for 5G technology [52–54]. Likewise, based on the calculations in Section 5.2, two different inductors are needed with inductance values of 261.6 and 1047 pH. Additionally, the inductor must have a high-quality factor and capability of driving low impedance because the lattice filter terminals are connected to 50 Ω. Taking into account these requirements, the active inductor architecture seen in Figure 5.3 is designed. In this schematic, back-to-back differential transconductance stages are employed similarly to [13]. Further, as discussed in the following, the cascode transistors added to the circuit increased its robustness against various fluctuations and facilitated high frequency operation. Due to the difficulty of designing a tuning mechanism that covers both 261.6 and 1047 pH inductances together, distinct FAIs are designed for these two values. The FAI-L_a circuit is designed for the inductors L_{a1} and L_{a2} depicted in Figure 5.2 whereas FAI-L_b is designed for the inductors L_{b1} and L_{b2}. The schematics of these two FAIs are identical, except for the size of several transistors.

The designed FAIs fit to the RLC model in Figure 5.4 for the useful frequency range. By substituting small-signal models for MOS transistors and solving the KCL equations of the circuit, it is discovered that the RLC parameters, are similar to those of conventional gyrator-C-based active inductor topologies [10] as described by

$$L_{\text{act}} = \frac{2C_1}{g_{\text{m1}}g_{\text{m2}}}, \quad R_{\text{s}} = \frac{2g_{\text{o1}}}{g_{\text{m1}}g_{\text{m2}}}, \quad C_{\text{p}} = \frac{C_2}{2}, \quad R_{\text{p}} = \frac{2}{g_{\text{o2}}}. \tag{5.7}$$

In Equation (5.7), C_1 represents the effective capacitance seen from the drain node of the first transconductance stage to the ground, while C_2 denotes the capacitance seen from the drain node of the second transconductance stage to the ground. The conductance values g_{o1} and g_{o2} are the effective output conductances at the drain nodes of the first and second stages, respectively. Finally, g_{m1} and g_{m2} are the transconductance values of the differential pair transistors of the first and second stages.

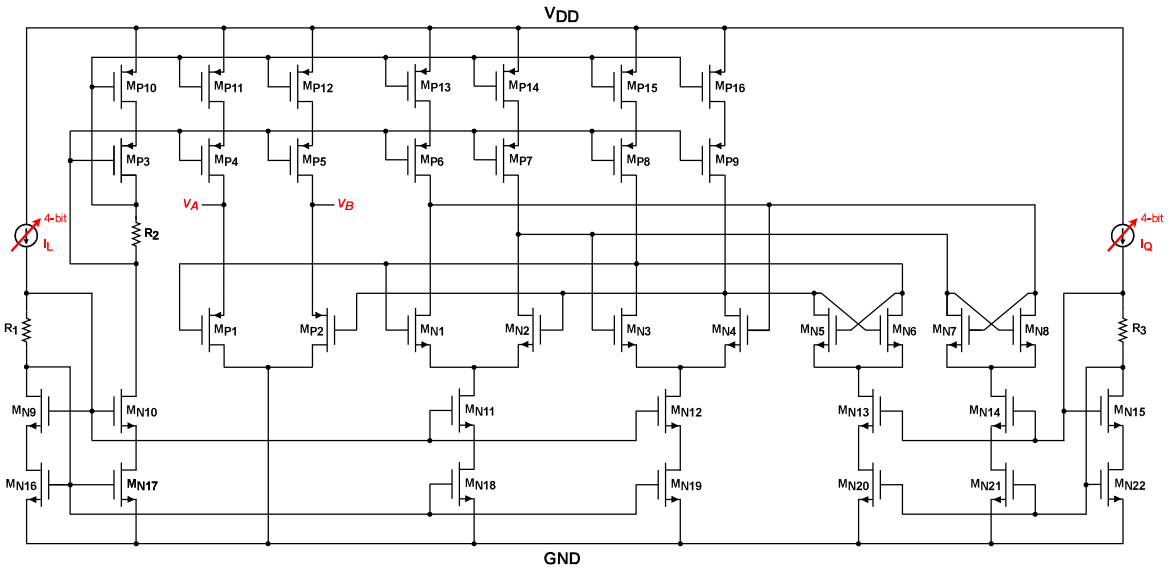


Figure 5.3. Proposed CMOS implementation of FAIs.

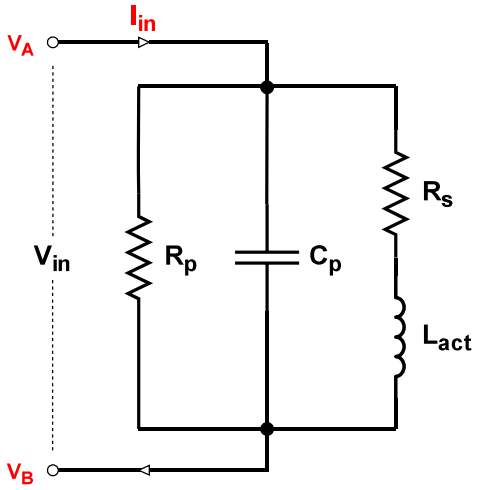


Figure 5.4. The equivalent RLC network of the designed FAIs.

Considering that the active inductance circuit is fully symmetrical, we can state that the C_2 parameter represented in Equation (5.7) will be described by the following equation:

$$C_2 = C_{\mathrm{dMN2}} + C_{\mathrm{dMP7}} + C_{\mathrm{gMN3}} + C_{\mathrm{dMN7}} + C_{\mathrm{gMN8}}, \tag{5.8}$$

where C_g represents the total effective capacitance between the gate of the corresponding transistor and the ground, and C_d represents the total capacitance between its drain and the ground. When the lattice filter design in Figure 5.2 is viewed, the C_a capacitors are obviously parallel to the L_a inductors. Rather of adding more extra PMOS varactors to implement the C_a capacitors, we may adjust the equivalent parallel capacitors C_p of the FAI-L_a to match C_a values. Thus, the silicon area is conserved in this way and the circuit becomes easier to run at high frequencies since no additional capacitors are required. Given the C_a value of 104.66 fF in Table 5.1, these values may be obtained using the gate and drain parasitic capacitances of the transistors as seen in Equation (5.8).

Transistor pairs $M_{N1} - M_{N2}$ and $M_{N3} - M_{N4}$ provide gyrator realization as back-to-back differential transconductance stages. The reason for using these devices as N-channel MOS (NMOS) is to attain a greater transconductance in the same dimensions and bias current, which results in the lowest parasitic capacitance possible while providing the required transconductance in high-frequency applications. Considering that two transconductance stages are symmetrical for this design, the inductance equation in Equation (5.7) can be organized as

$$g_{m1} = g_{m2} = \sqrt{\frac{2C_1}{L_{act}}}. \tag{5.9}$$

When the C_1 and L_{act} values are taken as 105 fF and 1.05 nH for the FAI-L_a circuit, the required g_m value is roughly determined as 14 mS. A similar method can be applied for the calculations of the FAI-L_b circuit.

As can be observed in Equation (5.7), as the g_m values are raised, an inductor with a low R_s value is created; however, this reduces the inductance value. There is such a trade-off in circuits that demand high inductance and high-quality factor. For this design, only the necessary inductance and capacitance values are considered when evaluating the g_m values of the $M_{N1} - M_{N2}$ and $M_{N3} - M_{N4}$ pairs. The high R_s value obtained in this scenario also results in an insufficient quality factor for the designed

FAIs. To solve this issue, cross-coupled pairs $M_{N5} - M_{N6}$ and $M_{N7} - M_{N8}$ form negative resistance circuits as a Q-enhancement technique as in [35]. It is critical to keep the cross-coupled devices minimal to avoid adversely affecting the circuit speed. Compensation for device shrinking can be accomplished by boosting the bias current of the cross-coupled pairs to obtain the desired transconductance from these devices. Furthermore, the bias currents of the cross-coupled transistors are designed to be digitally programmable. As a result, an adjustable circuit is implemented to meet the Q values needed.

Another critical feature of the desired FAIs is driving low resistance due to 50 Ω resistances at the filter ports. As a result, M_{P1} and M_{P2} transistors are added to both inductor terminals as source follower buffers, as suggested in [11]. These transistors resulted in a low-impedance output of the circuit at the expense of more power consumption. For both FAI-L_a and FAI-L_b circuits, each buffer consumes around 1.2 mA of current, representing a significant part of the power consumption of the designed APF.

Transistors $M_{N9–22}$ are utilized as NMOS current sources, whereas $M_{P3–16}$ transistors are employed as PMOS current sources. These current sources are cascoded to minimize bias current variation in the circuit. Moreover, the lengths of the $M_{P13–16}$ would have to be large to avoid channel length modulation in the absence of the $M_{P6–9}$ cascode transistors. This increases the parasitic capacitance on the drains of the transconductance stages and degrades the high-frequency performance of the circuit as seen in Equation (5.8). When we add cascode transistors and keep their lengths to a minimum, we eliminate channel length modulation effect and keep the parasitics on the drains to a minimal level. Finally, resistors $R_{1–3}$ have been added to generate the bias voltages of the cascoded current mirrors. The resistance values for R_1 and R_2 are set to 4 kΩ, and the resistance for R_3 is set to 8 kΩ for proper biasing.

For FAI-L_a, the bias current I_L consists of a fixed current source of 48 μA, and digital controllable current sources with 4, 8, 16, and 32 μA values. Thus, the bias

current can be changed in increments of 4 μA between values of 48 μA and 108 μA. On the other hand, the bias current I_{Q} can take values between 24 μA and 54 μA in increments of 2 μA. The control bits are configured to "1000" in the nominal state, and the bias currents I_{L} and I_{Q} are set to 80 μA and 40 μA, respectively. The FAI-$\mathrm{L_b}$ circuit is supplied with 1.5 times the currents specified for the FAI-$\mathrm{L_a}$ circuit. The transistor parameters of both FAIs are listed in Table 5.2, then the FAI-$\mathrm{L_a}$ layout, about 110 μm $\times$ 30 μm in size, is demonstrated in Figure 5.5.

Table 5.2. Aspect ratios of the transistors in the designed FAIs shown in Figure 5.3.

Transistor	**FAI-$\mathbf{L_a}$**		**FAI-$\mathbf{L_b}$**	
	Width (W)	*Length (L)*	*Width (W)*	*Length (L)*
$\mathrm{M_{N1}} - \mathrm{M_{N4}}$	102.4 μm	60 nm	307.2 μm	60 nm
$\mathrm{M_{N5}} - \mathrm{M_{N8}}$	12.8 μm	60 nm	25.6 μm	60 nm
$\mathrm{M_{N9}}$, $\mathrm{M_{N10}}$	2 μm	60 nm	2 μm	60 nm
$\mathrm{M_{N11}}$, $\mathrm{M_{N12}}$	80 μm	60 nm	80 μm	60 nm
$\mathrm{M_{N13}}$, $\mathrm{M_{N14}}$	12 μm	60 nm	12 μm	60 nm
$\mathrm{M_{N15}}$	1 μm	60 nm	1 μm	60 nm
$\mathrm{M_{N16}}$, $\mathrm{M_{N17}}$	4 μm	400 nm	4 μm	400 nm
$\mathrm{M_{N18}}$, $\mathrm{M_{N19}}$	160 μm	400 nm	160 μm	400 nm
$\mathrm{M_{N20}}$, $\mathrm{M_{N21}}$	24 μm	400 nm	24 μm	400 nm
$\mathrm{M_{N22}}$	2 μm	60 nm	2 μm	60 nm
$\mathrm{M_{P1}}$, $\mathrm{M_{P2}}$	256 μm	60 nm	256 μm	60 nm
$\mathrm{M_{P3}}$	4 μm	60 nm	4 μm	60 nm
$\mathrm{M_{P4}}$, $\mathrm{M_{P5}}$	120 μm	60 nm	80 μm	60 nm
$\mathrm{M_{P6}} - \mathrm{M_{P9}}$	80 μm	60 nm	80 μm	60 nm
$\mathrm{M_{P10}}$	8 μm	400 nm	8 μm	400 nm
$\mathrm{M_{P11}}$, $\mathrm{M_{P12}}$	240 μm	400 nm	160 μm	400 nm
$\mathrm{M_{P13}} - \mathrm{M_{P16}}$	160 μm	60 nm	160 μm	60 nm

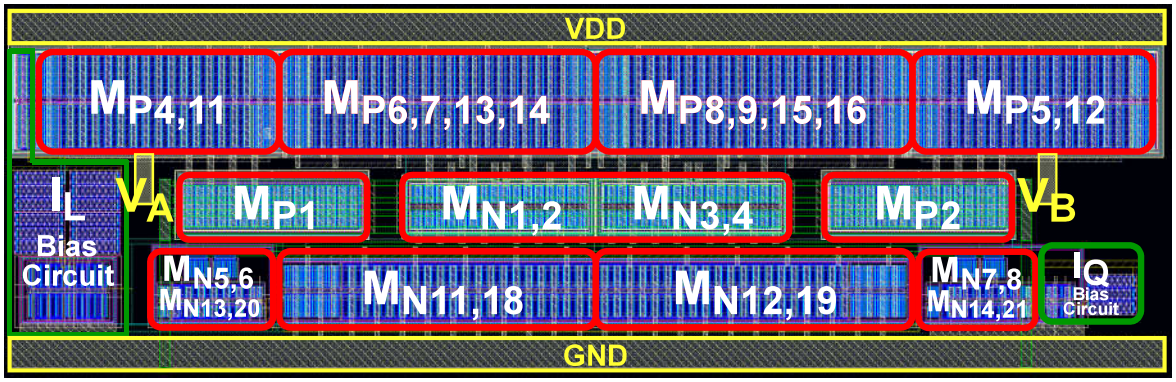


Figure 5.5. The layout of the FAI-L_a circuit with the dimension of 110 μm $\times$ 30 μm.

5.4. Simulation Results

This section includes post-layout simulation results for the APF circuit created by combining the FAIs designed in Section 5.3 with the lattice filter topology discussed in Section 5.2. The lattice APF, as described in Section 5.2, obtained its final shape following minor schematic revisions and optimizations during the post-layout simulation phase. The final schematic is depicted in Figure 5.6, while the final component values and their tuning ranges are listed in Table 5.3. As discussed in Section 5.3, the inductors in Figure 5.2 are implemented as FAIs. Additionally, the capacitances C_{a1} and C_{a2} are not apparent in Figure 5.6 since they are replaced by the parallel parasitic capacitances of the inductors L_{a1} and L_{a2}. Moreover, C_{b1} and C_{b2} capacitances are designed as PMOS varactors with an analog control voltage V_{ctr}, and ensure that when the inductance value of the FAIs are tuned, the capacitors C_{b1} and C_{b2} should be arranged to maintain the APF behavior. Additionally, when the filter response is degraded due to PVT effects, the tunable capacitors C_{b1} and C_{b2} may compensate for these effects. Each inductance tuning mechanism of the designed FAIs is controlled by a 4-bit digital signal in this design. The nominal setting of these control bits is determined as "1000" when only the most significant bit (MSB) is high. The nominal value of the V_{ctr} voltage is determined as 300 mV.

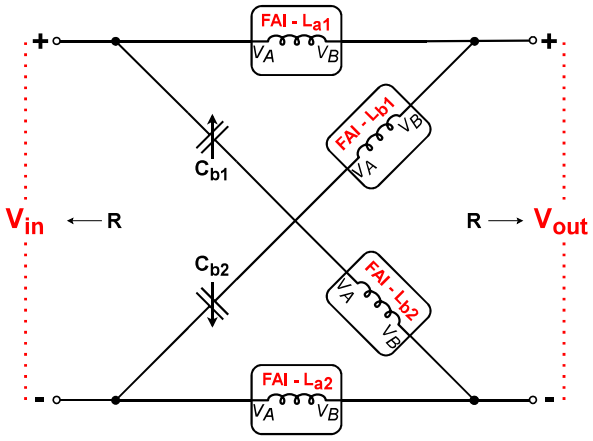


Figure 5.6. The final schematic of the designed second-order lattice APF.

Table 5.3. Final component values of the proposed lattice filter and their tuning ranges.

Comp. Name	**Nominal Value**	**Tuning Range**
L_{a}	980 pH	$600 - 1300$ pH
L_{b}	280 pH	$160 - 380$ pH
C_{b}	400 fF	$240 - 540$ fF

The layout of the designed lattice filter, about 240 μm $\times$ 70 μm in size, is illustrated in Figure 5.7. If CMOS spiral inductors were used in the place of FAI-L_{a} and FAI-L_{b} circuits, the required structures would be as seen in Figures 5.8 and 5.9. For 3.6 GHz operation, the inductor shown in Figure 5.8 has an inductance of 980 pH, a quality factor of 13.8, and dimensions of 195 μm $\times$ 170 μm. Figure 5.9 illustrates an inductor with a value of 280 pH, a quality factor of 15.1, and dimensions of 205 μm $\times$ 180 μm. The second spiral inductor has a lower inductance value but a larger silicon area than the first one due to the difference in the number of turns. When the number of turns on the second inductor is raised to 2, the inductance value of 280 pH is not obtained; thus, it is pushed to 1, which results in the diameter growing. Considering the dimensions of these spiral inductors, the area of the spiral counterpart of the APF circuit in Figure 5.7 would be approximately 400 μm $\times$ 360 μm. This area is more than

eight times larger than the area of the FAI-based architecture, which demonstrates the incomparable benefit of using FAI structures in terms of silicon consumption.

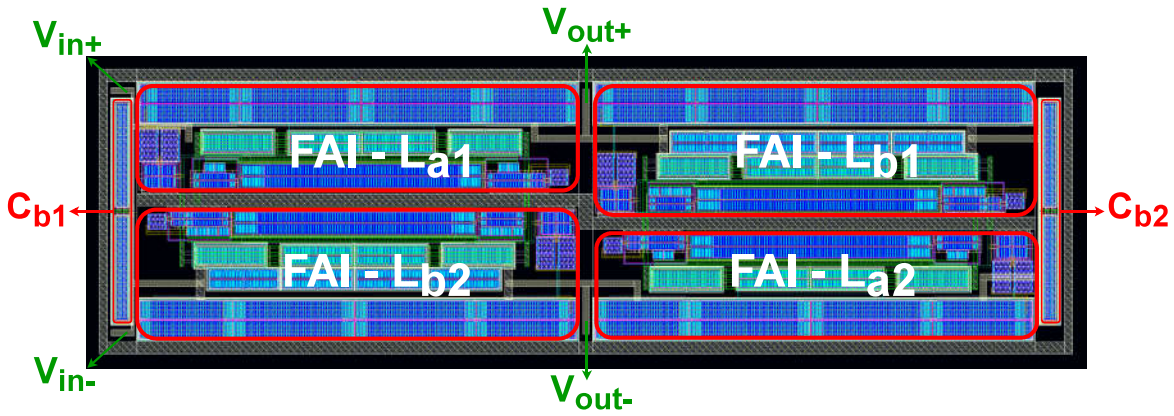


Figure 5.7. The layout of the designed lattice APF with the dimension of 240 μm $\times$ 70 μm.

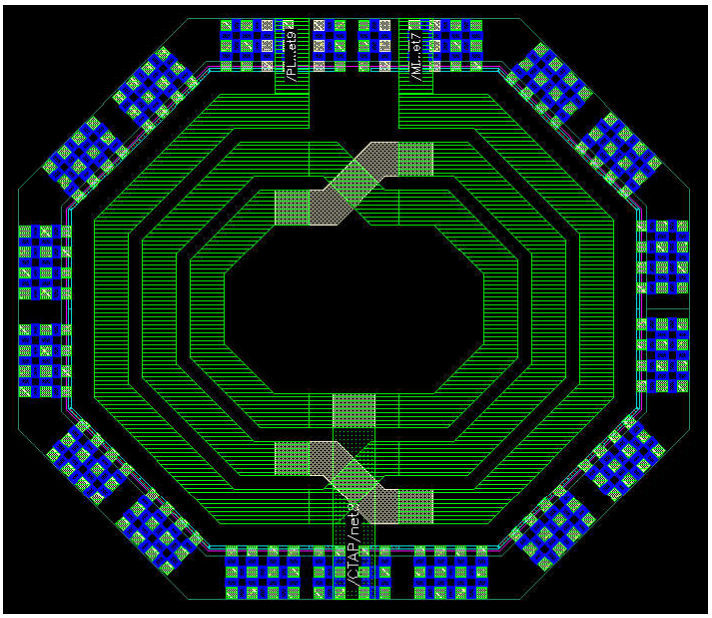


Figure 5.8. The spiral inductor with the same inductance value as the FAI-L_a circuit.

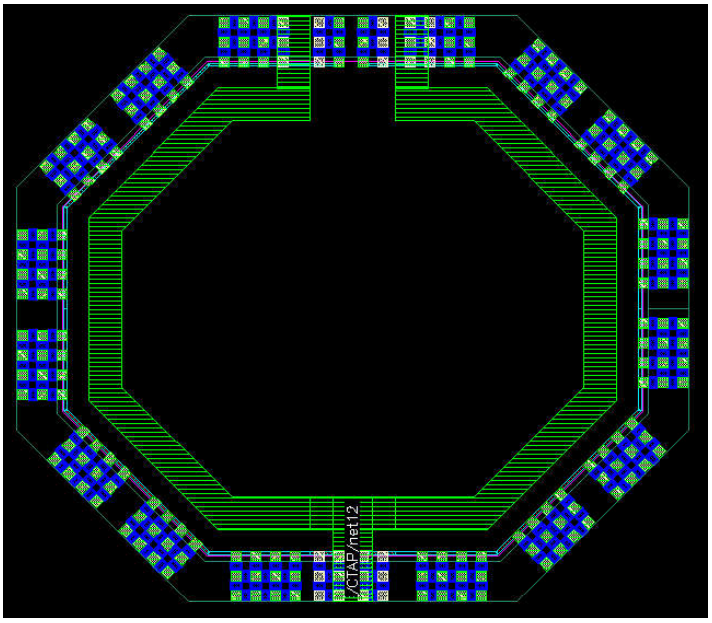


Figure 5.9. The spiral inductor with the same inductance value as the FAI-L_b circuit.

To validate the circuit performance, the suggested lattice all-pass filter with the proposed FAIs is simulated in Cadence Design Suite using the TSMC 65-nm CMOS PDK. The simulations also take into account parasitics from the layout. The supply voltage is chosen at 1.5 V to provide sufficient headroom for the MOS transistors to operate properly and enable a broad range tuning mechanism.

Figure 5.10 depicts the magnitude and phase responses of the designed APF for nominal condition and 16 distinct tuning configurations. These settings are obtained by trimming the bias currents I_L of the FAI-La and FAI-Lb circuits with 4-bits and adjusting the V_{ctr} voltage of the PMOS varactors. As illustrated in Figure 5.10, the filter gain decreases from -0.125 dB to -1.62 dB as the frequency increases to 5 GHz and does not vary significantly for different tuning configurations. On the other hand, it could be seen that phase values vary between tuning settings, resulting in variable delay values for each tuning level.

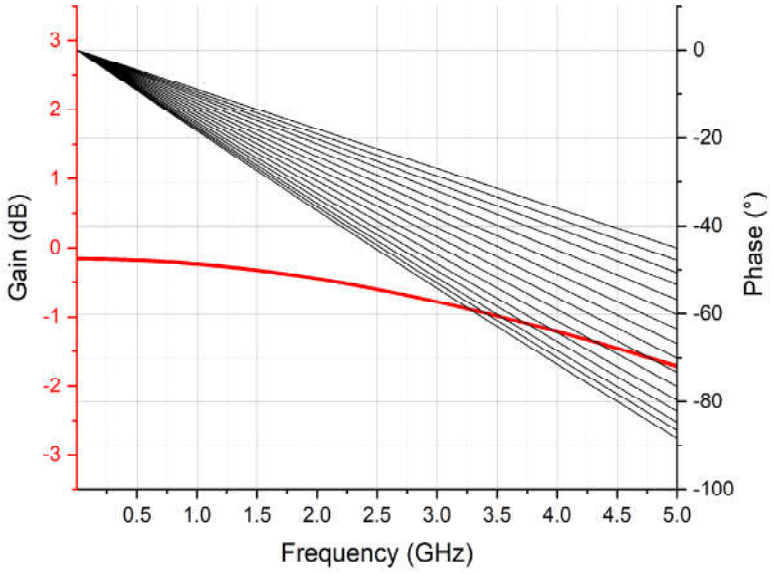


Figure 5.10. The frequency response of the designed APF for different tuning configurations.

The group delay values for the designed APF circuit for 16 tuning levels are shown in Figure 5.11. These curves, which have a nominal value of 38 ps and a range of $24.5 - 50$ ps, exhibit a rather flat characteristic up to 5 GHz. This is a handy feature for circuits that require constant delay across a specific frequency band. Figure 5.12 illustrates the delay variation percentages of each delay curve of tuning configurations. These variation values are calculated by dividing the difference between the minimum and maximum delays in each curve by the average delay value of this curve. For instance, the group delay error is 114 fs, which is a 0.294% variation in the nominal case.

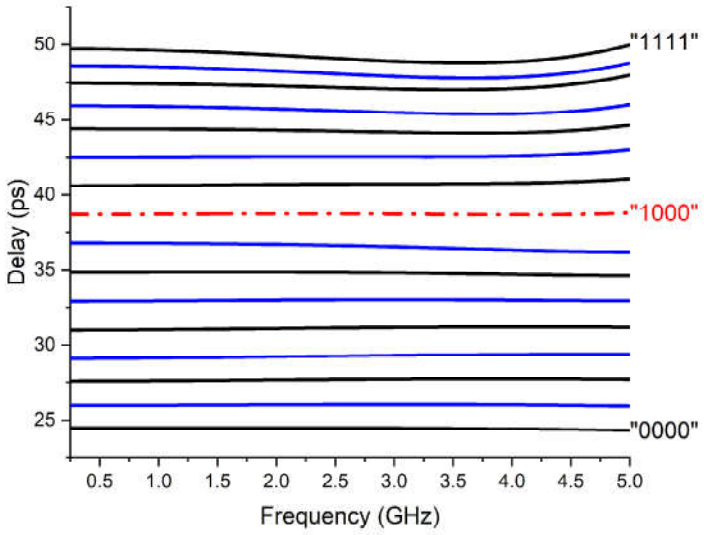


Figure 5.11. The group delay of the designed APF for different tuning configurations.

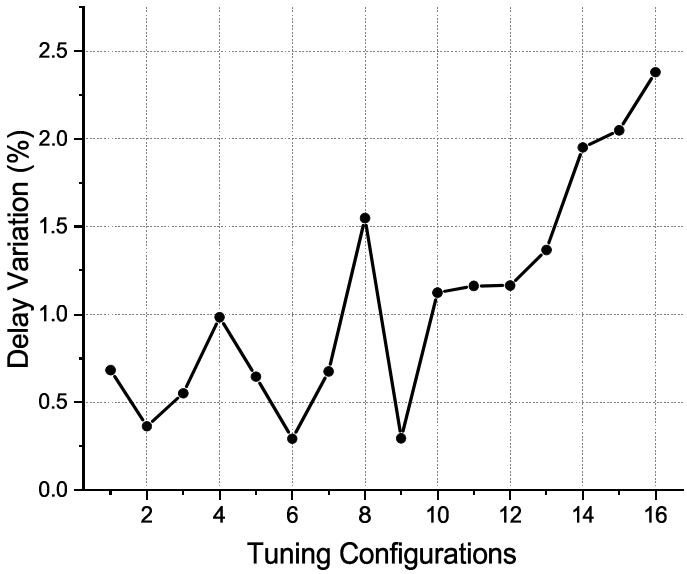


Figure 5.12. The group delay variations of the designed APF for different tuning configurations.

PVT analysis is critical for determining if it is feasible to fabricate a circuit. The group delay graphs of 4 PVT corners can be seen in Figure 5.13. As seen in Figure 5.13, the deviation of each curve is increased due to the PVT variation of the FAIs and the capacitors. The slope of the group delay can be controlled by tuning the inductance values of FAIs and the capacitance values of the C_{b1} and C_{b2} capacitors. As a result, separate tuning bits can be used to adjust for PVT variations at each corner value. In Figure 5.13, the compensated curves generated by simply adjusting the inductance values are denoted by dashed lines; this tuning method is referred to as 1-D tuning. For the corner of C8, where 1-D tuning is insufficient, 2-D tuning was used, which activates the V_{ctr} voltage as well. This is depicted in a dotted graph. Figure 5.14 also depicts the delay variation percentages for the nominal state and 8 PVT corners, described in Table 5.4. When Figure 5.14 is analyzed, delay variation greater than 25% due to the PVT effect is reduced to 10% with 1-D tuning and to less than 3% with 2-D tuning mechanism. Thus, despite PVT variations, an APF with a flat delay response is designed thanks to the tuning capability obtained as a benefit of using AIs.

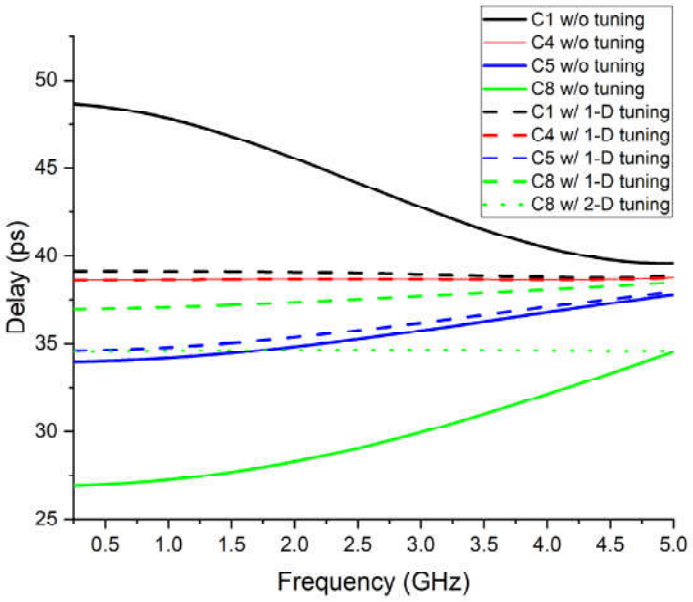


Figure 5.13. The group delay of the designed APF for PVT corners.

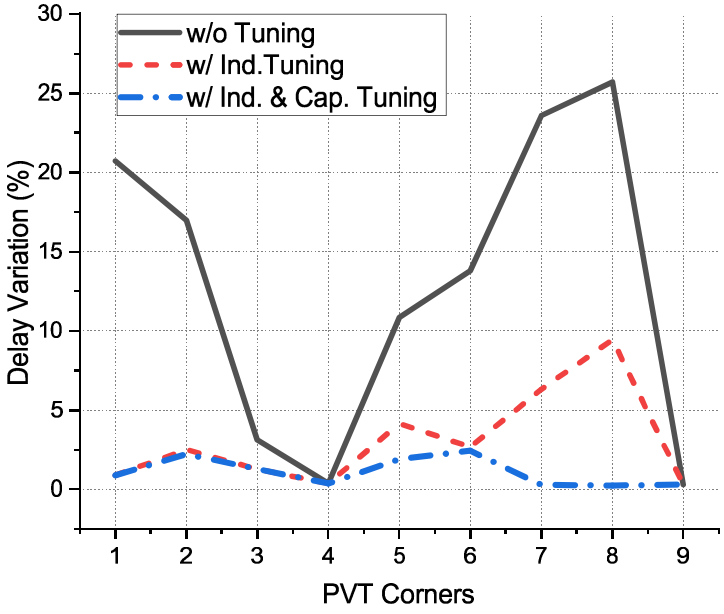


Figure 5.14. The group delay variations of the designed APF for PVT corners.

Table 5.4. Descriptions of each PVT corner introduced in Figures 5.13 and 5.14.

Name	**Process**	**Voltage (V)**	**Temp. (°C)**
C1	Fast-Fast	1.65	85
C2	Fast-Fast	1.35	85
C3	Fast-Fast	1.65	–40
C4	Fast-Fast	1.35	–40
C5	Slow-Slow	1.65	85
C6	Slow-Slow	1.35	85
C7	Slow-Slow	1.65	–40
C8	Slow-Slow	1.35	–40
C9	Typical	1.5	27

5.5. Review of the Literature and Comparison

Table 5.5 summarizes the performance of the designed APF in comparison to data from state-of-the-art APF implementations [57, 59, 61–64].

Table 5.5. Literature Comparison

	[57]	**[62]**	**[64]**	**[61]**	**[59]**	**[63]**	**This**
Process Node	65 nm	800 nm	180 nm	65 nm	130 nm	130 nm	65 nm
Supply Voltage	1	2.5	1.8	1	–	1.5	1.5
Filter Order	2nd	2nd	1st	1st	4th	1st	2nd
Frequency (GHz)	$0.4-2$	$3-10$	$0.1-5$	$0.3-3$	$0-3.5$	$0-3.8$	$0-5$
Delay (ps)	$30-57$	$50-75$	$59-72$	$12-40$	380	55	$24.5-50$
DTR (%)	62.1	40.0	19.8	107.7	–	–	68.4
Delay Var. (%)	4.98	13.34	6.88*	7.20	89.5**	20.0	0.294
Gain (dB)	–4.7	–4	0.18	0	–1.21	–1	–0.15
Gain Var. (dB)	<0.75	3.5	1.22	<1	0.3	–	1.47
Power (mW)	2.74	38.8	10	0.183	0	19	43.5
Area (mm^2)	0.00187	0.42	–	0.00038	0.91	0.023	0.0168

When compared to the works listed in Table 5.5, the proposed filter structure, along with [62,64], stands out for its high operating frequency. This circuit seems suitable for a wide variety of high-frequency applications due to its flat delay response up to 5 GHz. The frequency band of $3.4-3.8$ GHz, which is specified for 5G applications, might be used as an example of these applications. Besides its high-frequency operation, the suggested circuit offers significant convenience and flexibility for the systems it is utilized, thanks to the high delay tuning range (DTR) value of 68.4%. Compared to previous research, the most striking aspect of the proposed filter is its extremely low delay variation value due to the lattice topology. The delay variation of the proposed circuit in the nominal case is simulated as 0.294%, while this value is recorded as 4.98% in the study closest to it in [57]. Additionally, since the filter gain is extremely close to 0 dB, similar to [61], it can be utilized without any gain adjustment circuit. While the gain variation decreases to -1.62 dB at 5 GHz, it remains less than -1 dB until

the 3.5 GHz range. This is a reasonable number compared to other research published in the literature. Furthermore, the designed APF circuit consumes significantly less area compared to the spiral inductor topologies seen in the literature [59,62,63]. Along with the benefits mentioned above, the proposed filter consumes much power since it has four FAIs running at fast speeds and with low inductance. The nominal power of 43.5 mW is reduced to around 26.1 mW in the "0000" configuration.

5.6. Chapter Summary

This chapter describes the design of a lattice APF circuit which employs FAIs, unlike prior publications in the literature. The proposed APF is more resilient to PVT effects and has a wide variety of delay curves due to the tunability of the inductance and quality factor values of the utilized FAIs. Designed with TSMC 65-nm PDK, the suggested APF operates at a frequency of up to 5 GHz and has a delay range of $24.5 - 50$ ps. Additionally, the designed APF exhibits a 0.294% delay variation in the nominal case, crucial for systems requiring a flat delay response. Furthermore, the APF has a gain of -0.15 dB, enabling it to be used without gain compensation circuitry. The variance in gain is less than 1 dB at 3.5 GHz and less than 1.5 dB at 5 GHz. Moreover, the APF covers a silicon area of 0.0168 mm^2, and consumes 43.5 mW at a 1.5 V supply. The future research will focus on strategies to reduce the power consumption of AIs in high-frequency applications.

6. A DESIGN OF AUTONOMOUS CHAOTIC OSCILLATOR ROBUST AGAINST EXTERNAL INTERFERENCE

6.1. Chapter Introduction

The growing demand for digital signature applications, electronic financial transactions, and information confidentiality has contributed to the popularity of random number generators (RNGs) over the last decade. The literature contains RNGs with a variety of entropy sources. These sources of entropy can be exemplified as metastabilities of ring oscillators [65, 66], discrete-time chaotic maps [67, 68], electrical noise [69], phase jitters [70] and continuous-time chaotic oscillators [71, 72].

The purpose of this chapter is to design an autonomous continuous-time chaotic oscillator to illustrate another application of CMOS AIs. The chaotic oscillator in [73] is taken further by substituting FAIs for the off-chip spiral inductors. Since on-chip spiral inductors cannot be employed due to the high inductance requirements of this architecture, off-chip inductors are necessarily preferred in [73]. However, one of the most fundamental issues with off-chip inductors is their susceptibility to external interference [74]. As a result, chaotic oscillator designs utilizing off-chip inductors may exhibit loss of chaotic behavior in the presence of external magnetic effects, which weakens the robustness of the security systems that use these chaotic oscillators as their entropy sources. Additionally, there is no simple way to obtain a tunable off-chip inductor. The FAI circuits employed in this design enable the design of a low-power autonomous chaotic oscillator that is immune to electromagnetic influences, consumes less silicon area, and has a tuning mechanism to preserve the chaotic behavior in the face of possible variations.

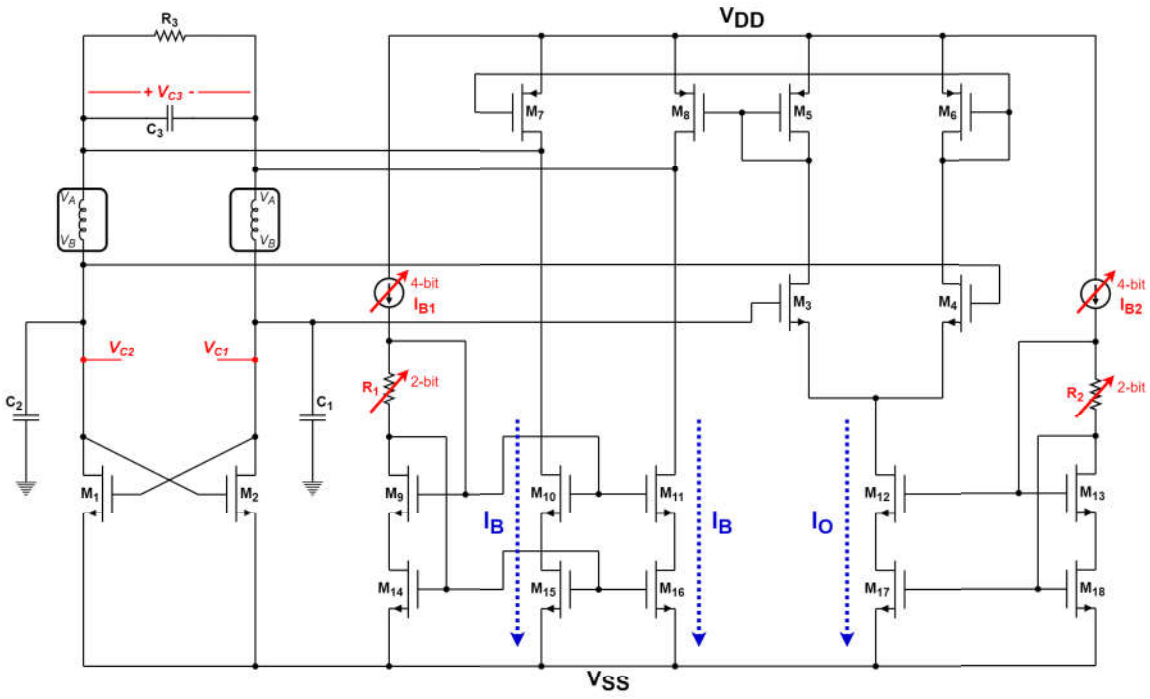


Figure 6.1. The schematic of the proposed chaotic oscillator.

6.2. Autonomous Chaotic Oscillator

Figure 6.1 illustrates the designed autonomous chaotic oscillator formed by combining an RC network and differential pairs with the classical cross-coupled oscillator, similar to [73]. The inductors required for this circuit have been built using FAIs, which is superior to previous studies. Thus, inductance values that are not practicable with spiral inductors can be achieved in a small silicon area. Additionally, since no off-chip inductor is utilized, security applications adopting the proposed chaotic oscillator will be immune to external interference. Moreover, the designed oscillator exhibits high power supply rejection and noise immunity thanks to its balanced architecture. Further, unlike [71], it operates on an autonomous principle that does not require an additional pulse to generate chaotic behavior.

As illustrated in Figure 6.1, the $M_{1\text{-}2}$ cross-coupled pairs provide the required negative resistance for oscillation, whereas the $M_{3\text{-}4}$ transistors form the differential

transconductance stage. The parallel R_3-C_3 is added to the circuit to provide chaotic behavior. As with conventional oscillator topologies, capacitors C_1-C_2 are employed to adjust the resonance frequency of the chaotic oscillator. Then, the bias circuit and current mirrors are formed using $R_{1\text{-}2}$ resistors and $M_{5\text{-}18}$ transistors. The cascode design of NMOS current mirrors is intended to limit the tail current variations and prevent the circuit from exhibiting chaotic oscillations in foreseeable variations due to high voltage swing. Additionally, the reference currents I_{B1} and I_{B2} are regarded to be 4-bit digitally controllable. Thus, after it is fabricated, if the designed circuit does not enter the chaotic region for nominal circuit parameters, suitable conditions can be established through trimming.

When the values of capacitors C_1, C_2, and C_3 are taken as C, the value resistor R_3 is R, and the inductance values of the FAIs are taken as L, the chaotic oscillator equations presented in Figure 6.1 are as follows

$$
\begin{aligned}
&C(v_{\dot{C}2} - v_{\dot{C}1}) = \frac{\beta}{2}(v_{C2} - v_{C1})[(v_{C2} + v_{C1}) - 2V_{th}] - \Delta i_L, \\
&L\Delta\dot{i}_L = v_{C2} - v_{C1} - v_{C3}, \\
&C(v_{\dot{C}2} + v_{\dot{C}1}) = kI_O - I_B, \\
&-\frac{\beta}{4}[(v_{C2} + v_{C1} - 2V_{th})^2 + (v_{C2} - v_{C1})^2], \\
&2Cv_{\dot{C}3} = \Delta i_L - \frac{2v_{C3}}{R}, \\
&+k\left\{\begin{array}{ll} I_O, & v_{C2} - v_{C1} \geq +V_{sat} \\ g_m(v_{C2} - v_{C1})\sqrt{1 - (\frac{v_{C2} - v_{C1}}{\sqrt{2}V_{sat}})^2}, & \mid v_{C2} - v_{C1} \mid < +V_{sat} \\ -I_O, & v_{C2} - v_{C1} \leq -V_{sat} \end{array}\right\},
\end{aligned}
\tag{6.1}
$$

where $\Delta i_L = i_L - i_R$ (differential inductor's current), $g_m = \sqrt{\beta I_O}$, $V_{sat} = \sqrt{\frac{2I_O}{\beta}}$, $\beta = \mu_n C_{ox}(\frac{W}{L})_{1,2}$; V_{th}, μ_n, C_{ox} and $\frac{W}{L}$ are the threshold voltage, the electron mobility, the oxide capacitance and the aspect ratio of M_{1-2} transistor pairs, respectively.

Using the normalized quantities: $R \equiv \sqrt{\frac{L}{C}}$, $x_1 = \frac{v_{C2}-v_{C1}}{2V_{ref}}$, $x_2 = \frac{v_{C2}+v_{C1}}{2V_{ref}}$, $y = \frac{\Delta i_L R}{2V_{ref}}$, $z = \frac{v_{C3}}{2V_{ref}}$, $t_n = \frac{t}{RC}$, and taking $V_{ref} = V_{th}$, the equations in Equation (6.1) can be transformed as following:

$$\begin{aligned}
\dot{x}_1 &= bx_1(x_2 - 1) - y, \\
\dot{y} &= x_1 - z, \\
\dot{x}_2 &= d - \frac{b}{2}[(x_2 - 1)^2 + x_1^2], \\
2\dot{z} &= y - 2z, \\
&+ k \left\{ \begin{array}{ll} c, & x_1 \geq +V_{sat} \\ \sqrt{2bc}x_1\sqrt{1 - (\frac{x_1}{\sqrt{2}x_{sat}})^2}, & \mid x_1 \mid < +V_{sat} \\ -c, & x_1 \leq -V_{sat} \end{array} \right\},
\end{aligned} \tag{6.2}$$

where $b = \beta R V_{th}$, $c = \frac{I_O R}{2V_{th}}$, $d = \frac{(kI_O - I_B)R}{2V_{th}}$, and $x_{sat} = \frac{V_{sat}}{2V_{th}} = \sqrt{\frac{c}{b}}$.

Equation (6.2) can exhibit chaotic behavior for different parameter sets. In [73], the numerical analysis results of the chaotic attractor obtained for the parameters b = 0.9, c = 0.15, d = 0.7 and k = 8 are shared as in Figure 6.2. Then, required component and tail current values are specified as L = $4.7\mu H$, C = 4.7 pF, R = 1 kΩ, I_O = 240 μA , and I_B = 100 μA, which necessitates using off-chip inductors due to the high inductance values needed. As a result, the system becomes sensitive to external interference. We will use FAIs to achieve the needed inductance values in this study, ensuring that the system is entirely on-chip and immune to external interference. Moreover, the designed chaotic oscillator will be compact and tunable since FAIs are used.

This study applies the following component values to design an oscillator exhibiting chaotic behavior, as illustrated in Figure 6.2. The inductance values of the FAIs are determined as 8 μH, the resistance R_3 is taken as 2.8 kΩ while the capacitance values of C_1, C_2, and C_3 are 1 pF. In addition, the bias resistors R_1 and R_2 are 2-bit programmable for different current settings with nominal values of 4 kΩ. The transistor dimensions of the designed chaotic oscillator are listed in Table 6.1. Finally, the

I_{B1} current is rated at 60 μA and trimmable between 10 and 160 μA, whereas the I_{B2} current is rated at 50 μA and trimmable between 10 and 160 μA.

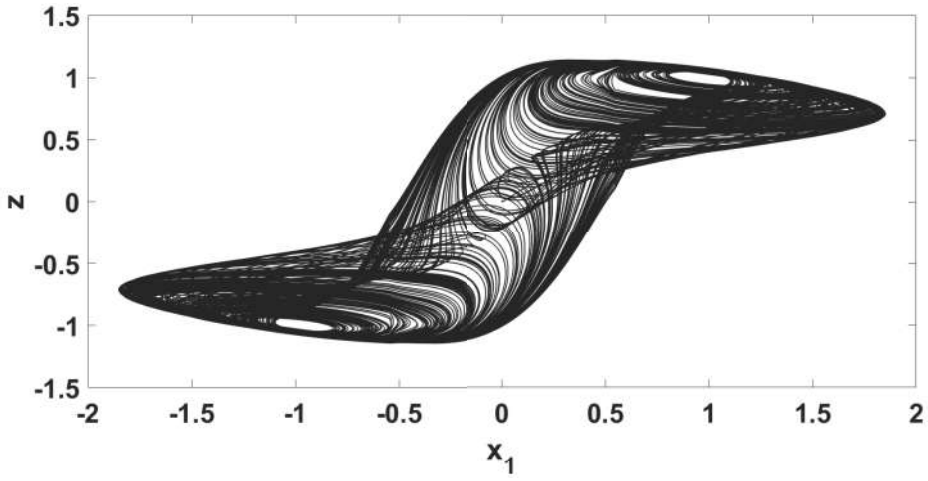


Figure 6.2. The chaotic trajectory of the designed system with numerical analysis.

Table 6.1. Aspect ratios of the transistors in the suggested chaotic oscillator (Figure 6.1).

Transistor	**Width (W)**	**Length (L)**
$M_{1\text{-}4}$	8 μm	500 nm
$M_{5\text{-}6}$	28 μm	1.6 μm
$M_{7\text{-}8}$	224 μm	1.6 μm
$M_{9\text{-}13}$	15 μm	180 nm
$M_{14\text{-}18}$	15 μm	1.2 μm

6.3. VDTA-Based Active Inductor

Although MOSFET-C-based AI topologies made with a small number of transistors are widely preferred in the literature due to their excellent high frequency responses, their low input mode range (ICMR) makes them unsuitable for applications

requiring large voltage swings. In this chapter, Voltage Differencing Transconductance Amplifier (VDTA)-based AI structure is preferred in the chaotic oscillator owing to the presence of a large output swing. The modified form of the AI topology presented in [12] is used in this structure. Figure 6.3 depicts the suggested FAI schematic and provides the aspect ratios of the current mirror transistors.

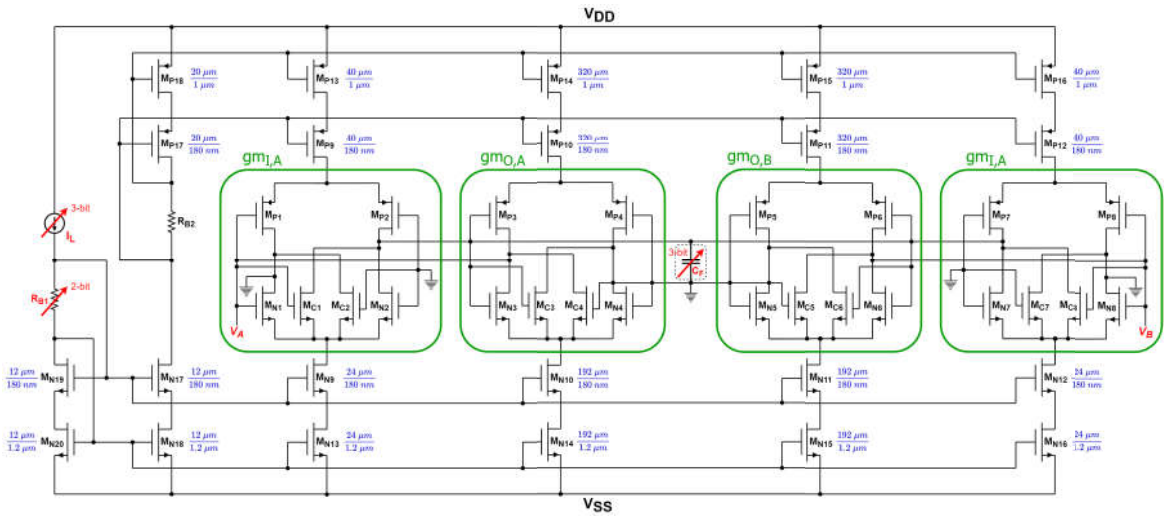


Figure 6.3. The schematic of the designed FAI.

Table 6.2. Transistor sizes of the transconductance stages of the designed FAI (Figure 6.3).

Transistor	**Width (W)**	**Length (L)**
$M_{N1,2,7,8}$, $M_{P1,2,7,8}$	800 nm	180 nm
$M_{N3\text{-}6}$, $M_{P3\text{-}6}$	6.40 μm	180 nm
$M_{C1,2,7,8}$	400 nm	180 nm
$M_{C3\text{-}6}$	2.4 μm	180 nm

In addition to the circuit described in [12], three fundamental modifications are made to the FAI architecture employed in this chapter. The first is to add cascode transistors to the current sources utilized in the VDTAs. Thus, it is planned to mini-

mize the change in the FAI's characteristic during oscillation by minimizing the effect of channel length modulation on the current sources. Second, the capacitance C_F is realized by using a 3-bit digital controllable capacitor bank. Hence, the inductance value and the quality factor adjustment can be performed via programmable C_F capacitance in addition to the I_L current. Lastly, cross-coupled transistor pairs ($M_{C1\text{-}8}$) are added to each transconductance stage to enhance the quality factor of the FAI.

Transistors $M_{P1\text{-}8}$ and $M_{N1\text{-}8}$ forms the g_{mI} and g_{mO} transconductance stages for each VDTA as seen in Figure 6.3. Given that two VDTA blocks of the designed FAI are symmetrical, the equivalent transconductance values of g_{mI} and g_{mO} can be expressed by the following equations

$$\begin{aligned} g_{mI} = g_{mI,A} = g_{mI,B} &= \left(\frac{g_{mn1}g_{mn2}}{g_{mn1}+g_{mn2}}\right) + \left(\frac{g_{mp1}g_{mp2}}{g_{mp1}+g_{mp2}}\right), \\ g_{mO} = g_{mO,A} = g_{mO,B} &= \left(\frac{g_{mn3}g_{mn4}}{g_{mn3}+g_{mn4}}\right) + \left(\frac{g_{mp3}g_{mp4}}{g_{mp3}+g_{mp4}}\right), \end{aligned} \tag{6.3}$$

where g_{mni} represents the transconductance of the transistor M_{Ni}, and g_{mpi} refers to the transconductance of the transistor M_{Pi}. If each transistor pair has equal g_m values among themselves (e.g., $g_{mn1} = g_{mn2}$, $g_{mp1} = g_{mp2}$), Equation (6.3) may be reduced as follows

$$\begin{aligned} g_{mI} &= 0.5(g_{mn(1,2,7,8)} + g_{mp(1,2,7,8)}), \\ g_{mO} &= 0.5(g_{mn(3,4,5,6)} + g_{mp(3,4,5,6)}). \end{aligned} \tag{6.4}$$

As discussed in [12], when the parasitic capacitances and resistances of the AI is ignored, the equivalent inductance of the proposed circuit can be calculated as

$$L_{act} = \frac{C_F}{2g_{mI}g_{mO}}. \tag{6.5}$$

According to Equation (6.5), the product of the g_{mI} and g_{mO} values should be minimal due to the high required inductance value in this study. Also, it is essential to maintain a high g_{mO} value to avoid limiting the output current driving strength of the designed

FAI. As a result, the required inductance of 8 μH is reached for $g_{\mathrm{mO}} = 8g_{\mathrm{mI}} = 1$ mS when C_F is set to 2 pF. It is discussed in detail the effects of parasitics on the inductive behavior of the FAI in [12]. It is difficult to examine complicated equations that include all parasitic components manually. The shrinkage of transistor lengths with newer processes makes transistor models diverge from the expected quadratic behavior, complicating manual calculations even further. As a result, complicated equations, including parasitics, are used to gain an intuitive understanding of the circuit, and in this direction, circuit optimization is made using advanced simulation systems. After that, the R_{B1} and R_{B2} resistances are designed as 2-bit trimmable with nominal value of 4 kΩ, and the transistor dimensions are listed in Table 6.2. The designed FAI circuit consumes 1.52 mA current for the nominal setting. Figure 6.4 illustrates the equivalent input impedance graph of the designed FAI using this method while Figure 6.5 demonstrates the quality factor and inductance values for both tuning mechanisms in which I_L and C_F are controlled.

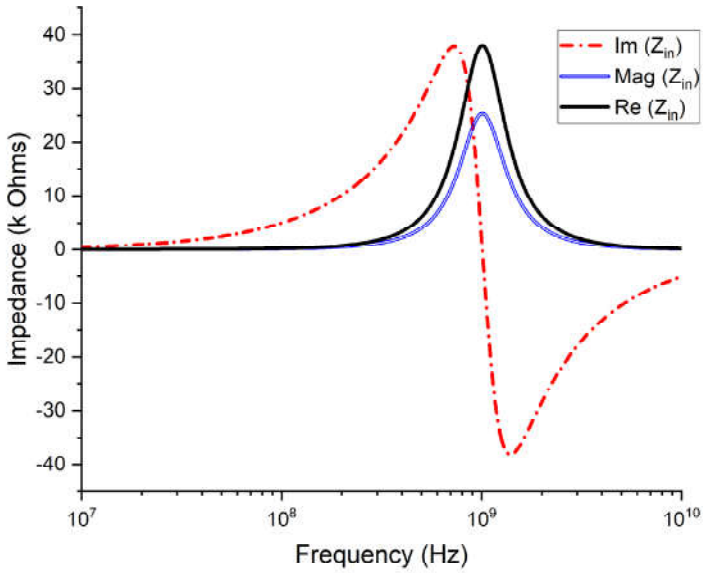


Figure 6.4. The input impedance graphs of the designed FAI for the nominal tuning setting.

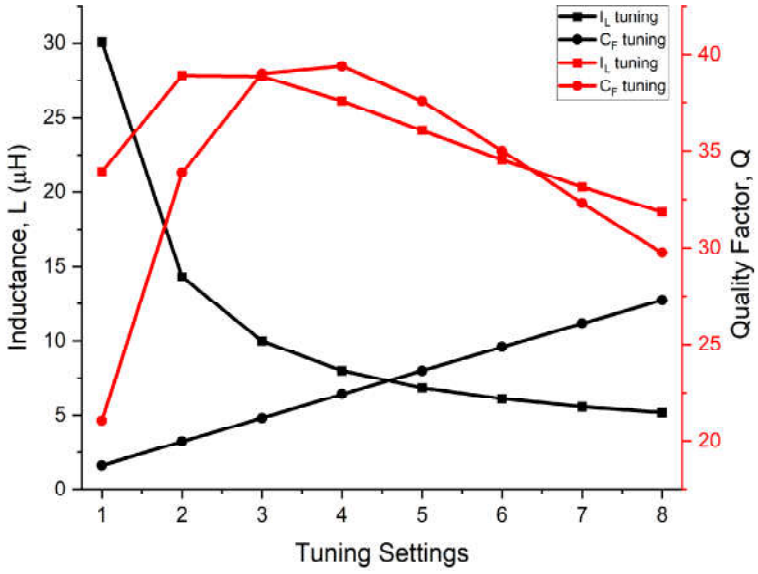


Figure 6.5. The inductance and quality factor of the FAI for different tuning settings.

6.4. Simulation Results

To validate the circuit functionality, simulations were run using the TSMC 180 nm PDK in the Cadence Design Suite. Further, the supply voltage is set at ±1.65 V to offer sufficient headroom for the transistors, ensuring that they retain their linear behavior in the presence of high signal swing. Figure 6.6 shows the transient simulation results for the v_{C1} node of the designed chaotic oscillator. This figure illustrates that the chaotic signal oscillates randomly in two distinct regions. In Figure 6.7, the v_{C2}-v_{C1} signal is plotted relative to v_{C3} to demonstrate that the random oscillation observed in Figure 6.6 is similar to the predicted chaotic trajectory, plotted in Figure 6.2.

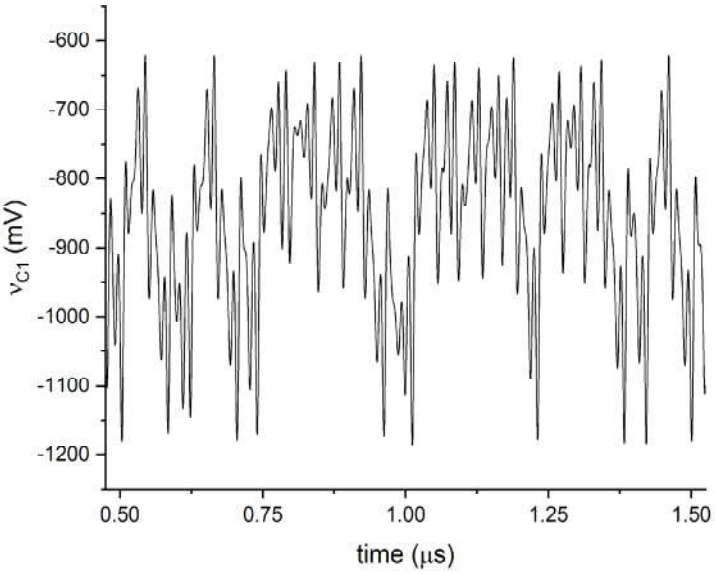


Figure 6.6. Transient simulation results for the v_{C1} node.

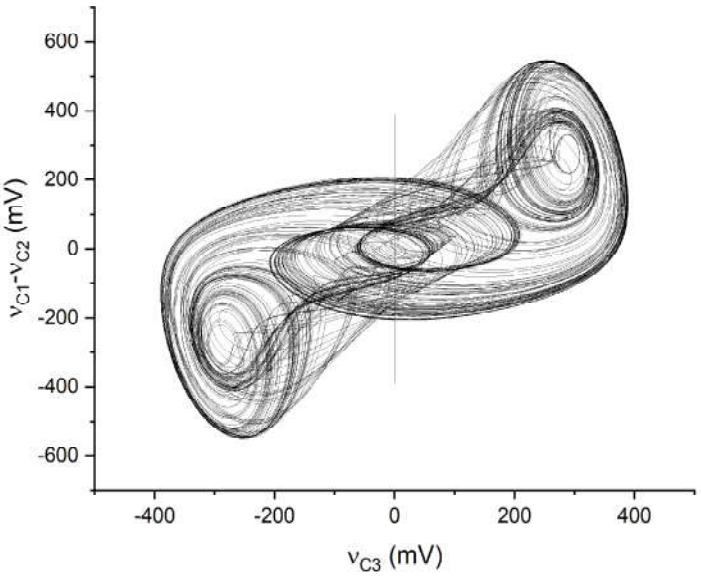


Figure 6.7. The simulated chaotic trajectory of the designed oscillator.

6.5. Chapter Summary

An autonomous chaotic oscillator design is presented. Compared to previous studies, VDTA-based FAIs are employed rather than off-chip inductors in this design. FAIs make the proposed chaotic oscillator immune to external interference, require less silicon area than spiral inductors, provide configurable inductance and quality factor, and allow to obtain high inductance values that cannot be achieved with their spiral counterparts. Further, a high quality factor needed in the oscillator is obtained by adding cross-coupled transistors to implement negative resistance. The numerical analysis of the chaotic oscillator is presented, and its CMOS feasibility is verified on Cadence Design Suite with TSMC 180 nm technology models. The proposed circuit consumes 11.88 mW power at the $\pm$1.65 V supply. Consequently, the presented circuit is a great alternative for use as an entropy source of a random number generator (RNG) in critical security systems thanks to its robustness to external interference.

7. CONCLUSION

Active inductance circuits, which are used in place of spiral inductors, can be constructed in a variety of methods. Each architecture has distinct characteristics that stand out from the others. Thus, certain topologies can be more suitable for specific application areas due to their prominent characteristics. The topology diversity of AIs enables them to be used in many fields. This thesis presents three CMOS implementations of AIs. With these circuits, it has been shown that AIs can be used in a wide variety of CMOS applications.

The first application discussed in this thesis is the low-voltage wide-tunable LC-VCO circuit. A novel MOSFET-C based FAI has been proposed in the designed LC-VCO. Thanks to the small number of transistors of the proposed FAI, the designed VCO consumes less silicon area and operates at high frequencies compared to the studies in the literature. Additionally, it has a wide operating frequency range due to the tunable FAI. On the other hand, its noise behavior is worse than that of VCOs with spiral inductors due to its AI-based structure. Hence, the designed VCO is well suited for applications in which phase noise is not essential.

The thesis also discusses a lattice network-based all-pass filter design suitable for 5G applications. A FAI having differential pair transconductance stages, capable of operating at high frequencies, driving a low resistance load, and having a high Q value is designed for this circuit. Thus, an allpass filter with wide-tunable delay values, minimal silicon consumption, and a decent gain response has been designed in accordance with published research. Thus, it has been shown that active inductors can also be used to build a filter for use in 5G technology, which is becoming more and more popular.

Finally, the use of AIs in hardware security applications is discussed with an autonomous chaotic oscillator design. In contrast to the literature, this design utilizes VDTA-based FAIs rather than off-chip inductors. Because the proposed oscillator

requires a large voltage swing, a VDTA-based AI architecture with a high ICMR characteristic is selected. FAIs give immunity to external interference, need less silicon space than spiral inductors, provide configurable inductance and quality factor, and enable the proposed chaotic oscillator to achieve inductance values that are not possible with spiral inductors. As a result of its immunity to external interference, the proposed circuit is an excellent candidate for use as an entropy source for RNGs in critical security systems.

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