A HIGH VOLTAGE TRIBOELECTRIC ENERGY HARVESTING SYSTEM UTILIZING PARALLEL-SSHI RECTIFIER AND DC-DC CONVERTERS FOR SUB-5 HZ MOTIONS

by

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ABSTRACT

A HIGH VOLTAGE TRIBOELECTRIC ENERGY HARVESTING SYSTEM UTILIZING PARALLEL-SSHI RECTIFIER AND DC-DC CONVERTERS FOR SUB-5 HZ MOTIONS

In this thesis, the first integrated circuit (IC) implementation of parallel synchronized switching harvesting on inductor (parallel-SSHI) is presented for triboelectric energy harvester targeting 1 Hz to 5 Hz mechanical motions. It is accompanied by on-chip buck and switched-capacitor DC-DC converters, all capable of handling 70 V levels. Unlike piezoelectric harvesters, triboelectric nanogenerators (TENGs) can produce very high open-circuit voltages; thus, the proposed system utilizes this property within the technology limits to maximize the extracted power.

An in-house manufactured TENG using steel and polytetrafluoroethylene (PTFE) is modeled for sub-5 Hz motions. The energy is extracted and stored in an external capacitance until its voltage reaches 70 V, which is achieved in three press-and-release mechanical cycles. 70-to-2 V down conversion is carried on by a 70-to-10 V buck converter followed by a 10-to-2 V switched-capacitor DC-DC converter. A chip is manufactured in TSMC 0.18 μm HV BCD process with an active area of 6.25 mm^2. End-to-end peak efficiency is measured as 32.71% for 1 Hz motion with a 722 μW total power delivery to the load for 4 ms.

ÖZET

5 HZ ALTI HAREKETLER İÇİN PARALEL-SSHI DOĞRULTUCU VE DC-DC ÇEVİRİCİLER KULLANAN YÜKSEK GERİLİM TRİBOELEKTRİK ENERJİ HASATLAMA SİSTEMİ

Bu tezde, 1 Hz ile 5 Hz mekanik hareketleri hedefleyen triboelektrik enerji hasatlayıcılar için indüktör (paralel-SSHI) üzerinde paralel senkronize anahtarlama yönteminin ilk entegre devre (IC) uygulaması sunulmaktadır. Her biri 70 V seviyelerini kaldırabilen yonga içiresinde buck ve anahtarlamalı kapasitör DC-DC dönüştürücüler sisteme entegre edilmiştir. Piezoelektrik hasatlayıcıların aksine, triboelektrik nanojeneratörler (TENG'ler) çok yüksek açık devre gerilimleri üretebilir; dolayısıyla, bu tezde önerilen sistem, çıkarılan gücü en üst düzeye çıkarmak için teknoloji sınırları dahilinde kullanılmıştır.

Çelik ve politetrafloroetilen (PTFE) kullanılarak kendi laboratuarımızda üretilen bir TENG, 5 Hz altı hareketler için modellenmiştir. Hasatlanan enerji, gerilimi 70 V'a ulaşana kadar harici bir kapasitansta depolanır, bu da arka arkaya üç basma ve bırakma mekanik döngüsüyle elde edilmektedir. 70 ile 2 V aşağı dönüşüm iki aşamada yapılmıştır; 70 V'tan 10 V'a dönüşüm buck dönüştürücü ile ve ardından 10 V'tan 2 V'a dönüşüm anahtarlamalı kapasitör DC-DC dönüştürücü ile gerçekleştirilir. TSMC 0.18 μm HV BCD teknolojisiyle, 6.25 mm^2 aktif alana sahip bir yonga üretilmiştir. Uçtan uca maksimum verimlilik, 1 Hz'lik hareket için % 32.71 olarak ölçülmüştür ve yüke 4 ms için toplam 722 μW güç aktarımı yapılmıştır.

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LIST OF SYMBOLS

A	Effective Contact Area
C_{dm}	Depletion-Layer Capacitance Per Unit Area
C_{ox}	Gate-Oxide Capacitance Per Unit Area
d	Thickness of PTFE Layer
V_D	Voltage Drop on Diode
V_T	Thermal Voltage
V_{th}	Threshold Voltage of MOSFET
ε_0	Permittivity of Air
ε_r	Dielectric Constant of PTFE Layer
σ	Surface Charge Density

LIST OF ACRONYMS/ABBREVIATIONS

3D	3-Dimensional
AC-DC	Alternating Current - Direct Current
BCD	Bipolar-CMOS-DMOS
BFR	Bias Flip Rectifier
CMOS	Complementary Metal Oxide Semiconductor
CNC	Computer Numerical Control
DC-DC	Direct Current - Direct Current
DCM	Discontinuous Conduction Mode
ESR	Effective Series Resistance
FBR	Full-Bridge Rectifier
HSS	High Side Switch
HV	High Voltage
IC	Integrated Circuit
IoT	Internet of Things
LDO	Low Dropout Regulator
LSS	Low Side Switch
MEMS	Micro-Electro-Mechanical Systems
MiM	Metal-Insulator-Metal
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPPT	Maximum Power Point Tracking
NMOS	N-type Metal Oxide Semiconductor
PCB	Peinted Circuit Board
PFM	Pulse Frequency Modulated
PLA	PolyLactic Acid
PMOS	P-type Metal Oxide Semiconductor
PTFE	Polytetrafluoroethylene
PVT	Process-Voltage-Temperature
PZT	Lead Zirconate Titanate

QFN	Quad-Flat No-leads
RF	Radio Frequency
SECE	Synchronous Electric Charge Extraction
SMD	Surface Mount Device
SPICE	Simulation Program with Integrated Circuit Emphasis
SSHI	Synchronized Switching Harvesting on Inductor
TENG	Triboelectric Nanogenerator
ZCD	Zero-Current Detector
ZnO	Zinc Oxide

1. INTRODUCTION

In the last few decades, technology has emerged in such a way that almost every information surrounding us is needed to be collected and processed to understand and provide profound knowledge for our existence in the universe. Advancements in manufacturing techniques have made required sensors and integrated circuits (IC) small, low power, low cost, and long-lasting. On the other hand, the wide usage of batteries due to lack of substitutes puts constraints on size, weight, and lifetime. Therefore, energy harvesting from the surrounding environment as an alternative to batteries is becoming popular to power up the sensors and ICs.

Energy harvesting systems are used to convert natural sources of energy, e.g., solar, wave, wind, and kinetic energy, etc., to electricity and store it to supply power for trending devices such as wireless sensor systems, wearable technologies, smart buildings and other applications of internet of things (IoT). Piezoelectric [2], thermal [3], photovoltaic [4], RF [5], electromagnetic [6], electrostatic [7] and triboelectric [8] energy harvesters are developed for this purpose. One of the popular categories of energy sources is low-frequency mechanical activities such as walking, tapping, typing, and other human motions, and ambient movements such as door opening, etc., with frequencies less than 5 Hz. Electromagnetic harvesters are widely used to generate power from them, but they are heavy and large in size due to permanent magnet usage. Also, their response to low-frequency movements (< 5 Hz) is less efficient than triboelectric ones [9]. Electrostatic methods are easy to integrate with ICs, but they need external voltage sources or electrets, which complicates their usage. Piezoelectric harvesters use some special materials such as lead zirconate titanate (PZT) and ZnO. These materials are fragile and costly to integrate with ICs. They cannot convert low-frequency motions efficiently either [9]. Thus, triboelectric methods have become one of the promising energy harvesting solutions in the last decade.

The above reasons have made triboelectric harvesters one of the promising solutions in the last decade. Triboelectric energy conversion is a result of triboelec-

trification and electrostatic induction: When two surfaces, solid-liquid or solid-solid, are contacted to each other and separated, a specific amount of charges with opposite signs are induced on both surfaces [10]. Induced charges can be electrostatically collected by intimately contacting electrodes on the back of the surfaces. Since the system works with surface interaction, it can be made lightweight, flexible, and stacked. Cost-effective films like polymers can be used to make it common and easy to produce. Using two materials that can be charged positively and negatively with respect to each other after contact and coating their backsides with metals is sufficient to create a triboelectric system [8, 11]. Triboelectric energy harvesters produce very high instantaneous open-circuit voltage peaks that can reach to hundreds to thousands of volts. Also, maximum instantaneous short circuit currents on the order of μA per cm^2 are generated. The voltage peaks are significantly disadvantageous and dangerous for electronic circuits. These voltage and impedance levels are not suitable for electronic circuits. In this thesis, we propose high voltage circuits that cope with these problems.

There are many piezoelectric harvesters that convert mechanical energy to electrical energy. Most of the studies in the literature use some active interface circuits to increase the efficiency of the piezoelectric harvesters. Some of these methods are maximum power point tracking (MPPT), synchronous electric charge extraction (SECE), and synchronized switching harvesting on inductor (SSHI). Most of the piezoelectric energy harvesters consist of a full-bridge rectifier followed by a DC-DC converter, which tracks the load impedance [12–15]. When buck DC-DC converters are used to match the load impedance and operated in discontinuous conduction mode (DCM), they effectively behave like a varying resistor [16]. Nevertheless, to realize maximum energy transfer, load impedance should be equal to the complex conjugate of the energy harvester impedance. However, matching the conjugate impedance requirement of low-frequency vibrations is hard to realize due to the large required inductance values. On the other hand, piezoelectric harvesters working close to the resonance frequency can be matched with resistive loads and achieve 75% efficiency [13]. To match the real part of the piezoelectric harvester impedance, a Maximum Power Point Tracking (MPPT) algorithm is used to maximize the output power of the DC-DC converter

by changing its pulse amplitude. Hence, maximum power transfer is realized. In [14], an MPPT algorithm usage results in 88% efficiency with a 60 V input voltage.

Non-linear harvesting methods have become popular to increase efficiency further. As shown in [17], switching piezoelectric harvester on top and bottom voltage levels can increase harvested power up to 8x [18]. Dicken *et al.* compared the SECE method with different non-linear harvesting methods. It concluded that switching piezoelectric harvester on top and bottom voltage levels maximizes transferred charges since the voltage of the internal capacitor gets ready for the charge extraction. A more transferred charge to the output means more power at the output. Hence, theoretically, up to 8x power can be obtained compared to the MPPT method [18–23]. In [19], this method is further optimized by connecting a parallel inductor to the internal capacitor and switching it to change the voltage levels immediately to transfer more charge to the output capacitor. In this study, parallel SSHI circuitry followed by DC-DC converter can reach 85% efficiency. In [20], a series SSHI circuitry is used with a transformer to achieve 75% efficiency. Finally, the harvester circuit presented in [21] allows input levels up to 200 V, which can be used in triboelectric harvester systems.

Although significant improvements in triboelectric nanogenerators (TENGs) have been achieved since 2012 [24], these studies have mainly interested in material and device developments to achieve higher power density rather than developing power management circuits for them [25, 26, 26–30]. Also, studies were made to understand the electrical characteristics of TENGs [31–33]. On the other hand, there are newer studies that focus on the power management of the triboelectric energy harvesters to implement some functional applications [23, 34–41]. These studies utilize either bridge rectifiers or active rectifiers to achieve AC-DC conversion. Many of these circuits are followed by a DC-DC converter to obtain an efficient power at the output of the system. SECE, SSHI, unidirectional switches, flipping capacitors are applied to the bridge rectifiers to improve the power extraction process. Also, almost all of these systems are implemented with discrete components. Very recently, [39] implemented an IC to harvest energy from TENG by applying MPPT circuitry to high voltage dual input buck converter to increase the efficiency. [40] presented some simulation

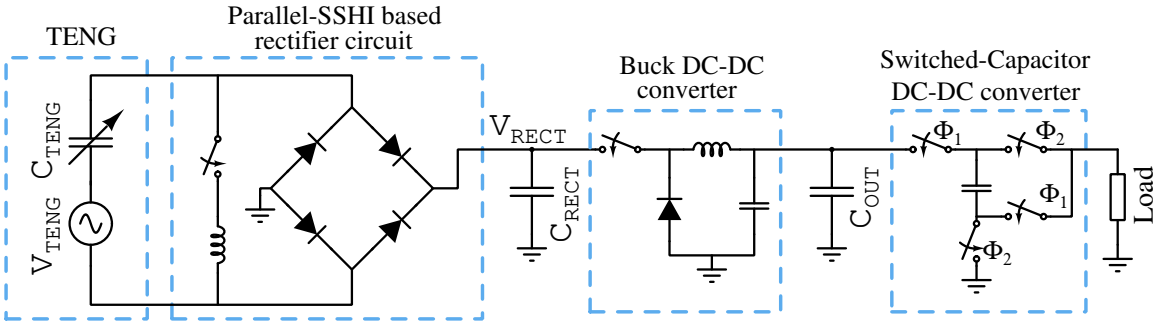

Figure 1.1. System architecture of the triboelectric energy harvesting integrated circuit.

results to demonstrate that discrete capacitors and switches without inductors can be used to implement SSHI style extraction from full-bridge rectifiers. By the time of the measurements made for this thesis, [41] presented the first SSHI rectifier for TENGs implemented with discrete components.

In this thesis, the first integrated circuit SSHI rectifier for triboelectric energy harvester is presented. The system shown in Figure 1.1 is implemented to store harvested energy on an external capacitor C_{RECT} at 70 V level, then the voltage is down-converted to 10 V level by a buck DC-DC converter to be further down-converted to 2 V level by a switched-capacitor DC-DC capacitor. High-voltage (HV) circuits are designed to implement SSHI rectifier and related circuits such as V_{RECT}-to-5 V low dropout regulator (LDO) to power-up the circuits needed by the SSHI rectifier, high-voltage switches with their driver circuits, etc. Some other HV circuits like level shifters are designed to operate for buck converter to deal with 70 V voltage level. The system charges a capacitor to 70 V with a 1-5 Hz mechanical motion, then detects 70 V level and enables the buck converter to start the down-conversion with the help of switched-capacitor DC-DC converter aiming for power delivery of 722 μW to the load for up to four milliseconds to power up a sensor or transmitter IC.

Chapter 2 explains the details of the TENG and the comparison of the conventional full-bridge rectifier with the SSHI rectifier. TENG measurements and effect of

frequency and contact separation distance variations to the delivered power amounts are discussed. Also, the modeling of the TENG for sub-5 Hz and its parameters are discussed.

The proposed parallel-SSHI implementation is detailed in Chapter 3. Difficulties of high voltage usage on integrated circuits are discussed and detailed. Also, the realization of high voltage solutions with ultra-low power circuits is explained. In Chapter 4, 70-to-10 V conversion step is explained. The buck converter and its sub-blocks are given in detail to elaborate the conversion. In Chapter 5, 10-to-2 V conversion step is explained in detail. The sub-blocks and additional blocks that are used for buck conversion are given in this chapter.

The integration of all the large blocks is discussed in Chapter 6. The designed chip and test setup for measurements are given with their key properties to understand the difficulties in measurements. Then, manufactured IC's measurement results are given in this chapter. Also, the measurement results are discussed, and performance comparison with the designs from literature is discussed.

Chapter 7 concludes this thesis with final remarks and discusses what can be done for future works for further improvements.

2. TENG MODELLING AND RECTIFIER COMPARISON

2.1. Introduction

In this chapter, the energy source of the system, which is a triboelectric nanogenerator, will be comprehensively explained. The in-house manufactured TENG used in this thesis is tested under various conditions, such as different frequencies, triboelectrification with paper, and different maximum contact separation distances between the film layers. These conditions affect the power sent to the load; thus, the best possible case from tests can be selected for further development of the interface circuits to maximize the extracted power from the triboelectric nanogenerator. In Section 2.2, the obtained measurement results from these tests are given. Furthermore, these measurement results are used to model the electrical properties of the TENG, which are very significant for simulations, and thus designing the interface circuits.

After determining the electrical properties of the TENG from the modeling process, the interface circuit choice is another important factor that affects the amount of power extracted from the TENG. In the literature, there are many interface circuits that are used for power extraction from energy generators like piezoelectric, electrostatic, and triboelectric generators. These interface circuits can extract a few folds more power compared to each other. In Section 2.3, two of the most used interface circuits from literature are compared with each other, and their qualifications as an interface circuit are explained in detail.

2.2. TENG Analysis and Modelling

A metal-to-dielectric contact-separation type TENG is fabricated in-house using a 50 μm thick steel film and 150 μm thick polytetrafluoroethylene (PTFE) film. Steel is a good material for micro-systems as an alternative to commonly used silicon, glass, plastics, and metals, which can be used to form both the electrode and mechanical spring and actuation mechanism of the TENG. PTFE is selected because it has the

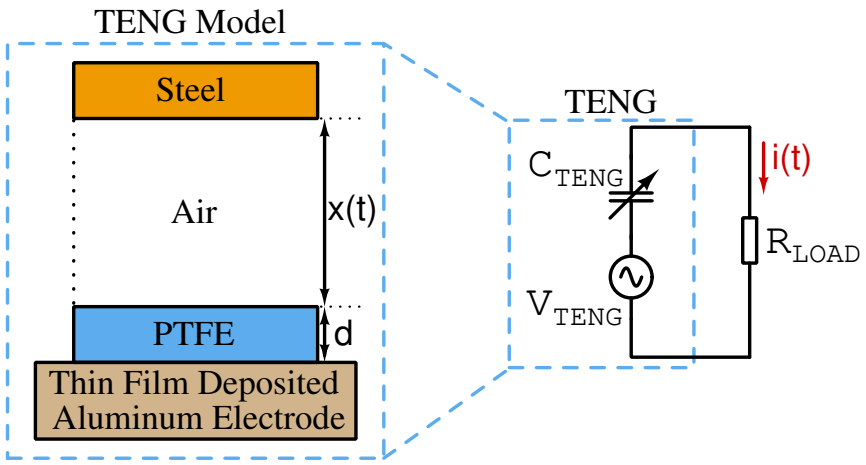

Figure 2.1. TENG model and equivalent circuit [1].

highest electronegativity in the triboelectric series. An electrode is formed on the backside of the PTFE film by depositing 200 nm thick aluminum film using a high vacuum thermal evaporator. The charges due to the triboelectrification are transferred to the electrodes that are attached to the back of the steel and PTFE upon the separation of these two layers, which are already in contact, as shown in the left side of the Figure 2.1. Right after the triboelectrification, charges on the electrodes are sent to load, and some of them returned to surfaces.

Triboelectrification between steel and PTFE surfaces is needed to be characterized. For this purpose, we performed SPICE simulations and measurements. Generated power values of TENGs depend on velocity, distance, frequency, and force magnitude of the motion and thickness and area of the PTFE. Hence, controlling the z-axis movement becomes very important, and realized with a three-axis computer numerical control (CNC) router machine. The machine is controlled with a software, which is called Mach3. This sowtfare utilizes a G-code to define the gap and motion. For identical press and release sequences, two custom-designed 3D printed poly(lactic acid) (PLA) blocks that are attachable to the CNC machine are used. Steel and PTFE films are attached to the surfaces of the 3D blocks. Electrical connections to the Al electrode of the PTFE film and the steel film are achieved by mechanically securing

electrical cables to them. Repeatable sine wave-like movement is achieved with the use of the CNC router machine. In Figure 2.1, the equivalent circuit model of TENG is shown. This model is used for SPICE simulations. Structural layers of the device are also drawn in this figure showing related device parameters. Figure 2.2 shows generated instantaneous current values for different frequencies when the load resistance is 30 $M\Omega$. These experiments are repeated for different load resistances and frequencies. The current on the load is measured with an electrometer for high accuracy. The average of the maximum peak current values for different loads is used to calculate the instantaneous power on the load.

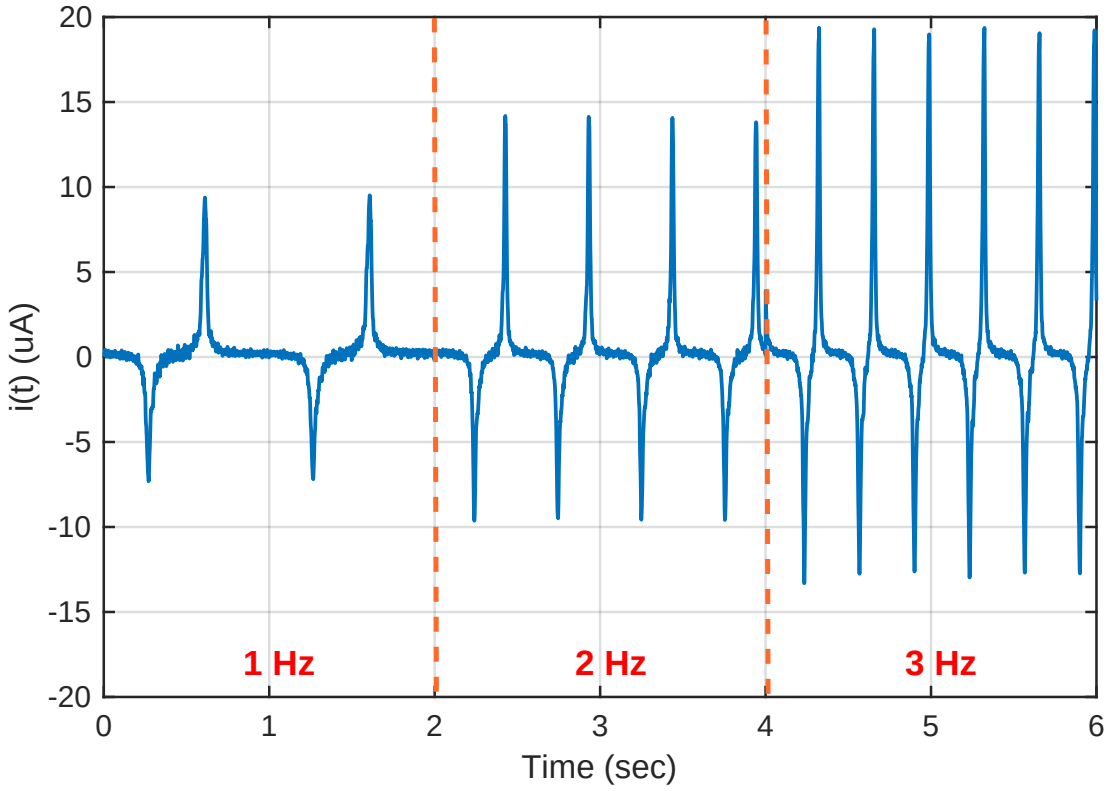

Figure 2.2. Current vs. time measurement for characterization of triboelectrification between steel and PTFE ($R_{load} = 30M\Omega$).

This measurement scheme is repeated for different frequencies, triboelectrification with and without paper, and different maximum contact separation distances in order to see their effect on maximum attainable power on load. The measurement results are given in Figures 2.3-2.8. Figure 2.3 and 2.4 demonstrate the increase in delivered power to the load by the increase of frequency. This is a result of the increase in the velocity of the press-release scheme. Another point is that delivered maximum power point shifts towards the left of the graph, indicating that smaller loads are enough to match the TENG's internal resistance to deliver the maximum amount of power.

The shift to the left of the maximum power point can be shifted further by increasing the triboelectrifaction by rubbing paper to the surfaces of the TENG layers. This effect can be seen from the Figures 2.4 and 2.5. Also, triboelectrification by paper significantly increases the power sent to the load, as it is shown in Figure 2.6. On the other hand, this effect is temporary and diminishes after a short amount of time. However, it can be used when the load needs a high amount of power. This property is duplicated by the MEMS laboratory by polymeric modification on one of the surface layers [8]. This process resulted in a significant increase in delivered power. However, the cost of this process is too much to use for common applications.

Another parameter that plays an essential role in delivered power amounts to the load is the maximum contact separation distance between the TENG surface layers. This distance amount is another control parameter for velocity. If we increase the maximum contact separation distance while keeping the frequency constant, we will increase the overall velocity for the press-release scheme, resulting in power increase. This situation is observed during the tests, and the related measurement result is shown in Figure 2.7.

The model needed for the design of the rest of the circuits is extracted from these measurement results. By looking at Figure 2.8, all the key parameters are extensively monitored, and the best suitable parameter set is chosen for modeling. The next step is modeling the TENG's electrical characteristics from the measurements.

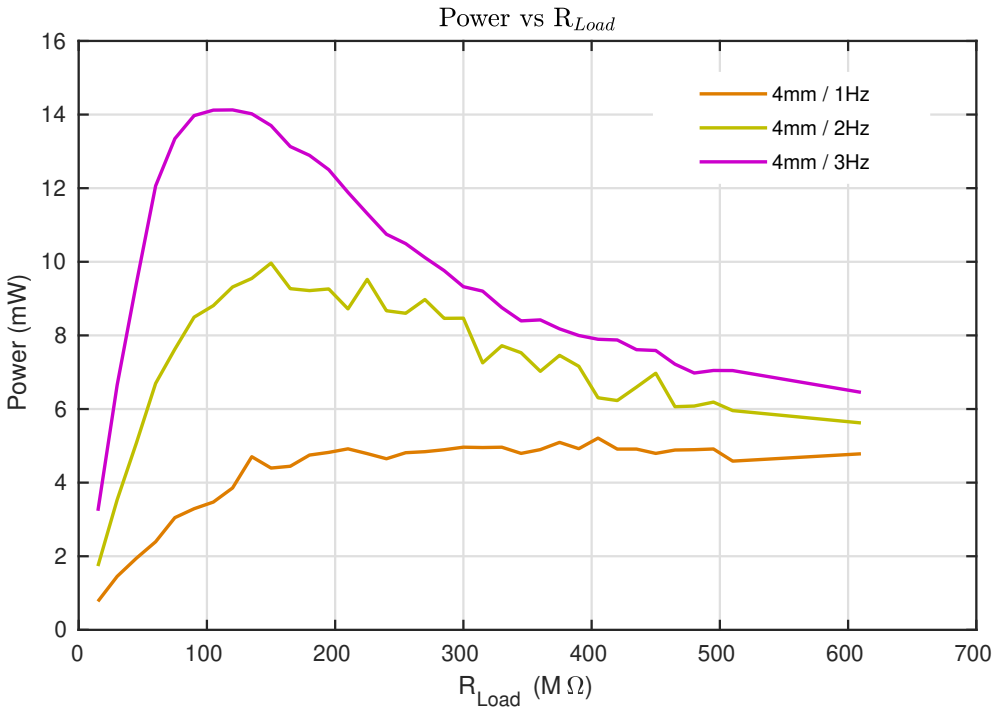

Figure 2.3. Measured power on resistive load for different frequencies, $x(t) = 4$ mm.

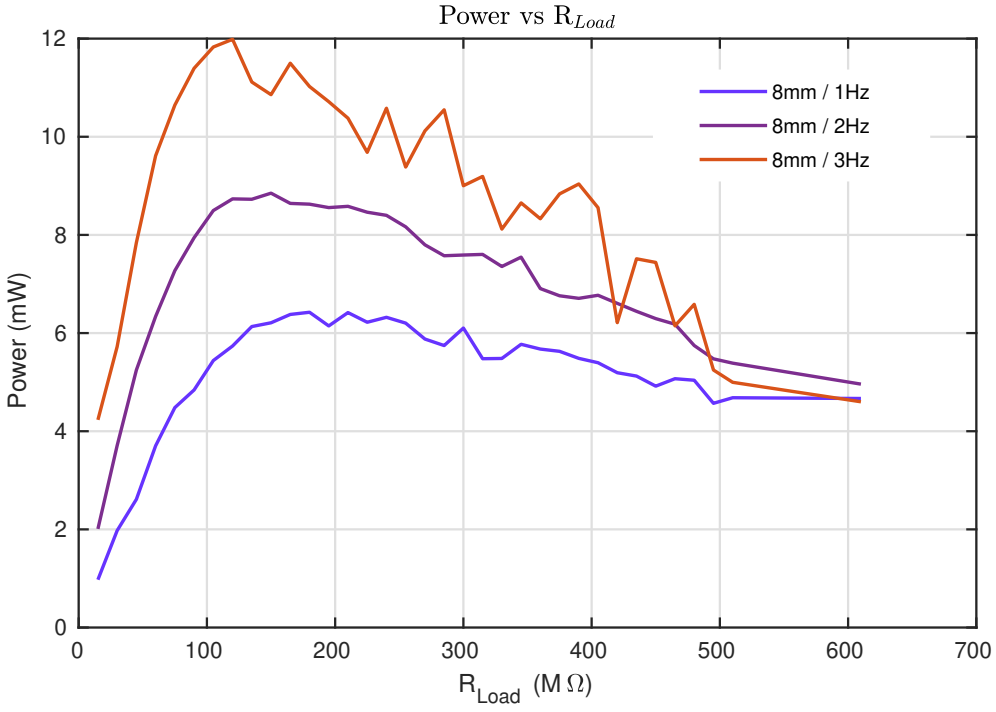

Figure 2.4. Measured power on resistive load for different frequencies, $x(t) = 8$ mm.

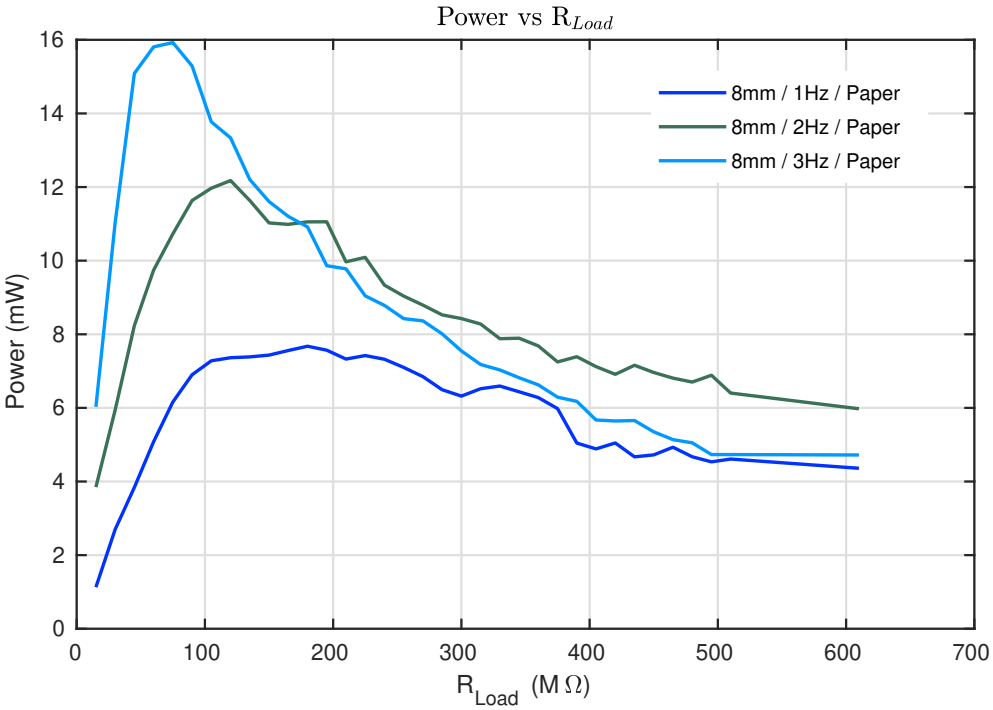

Figure 2.5. Measured power on resistive load for different frequencies, $x(t) = 8$ mm and triboelectrification with paper.

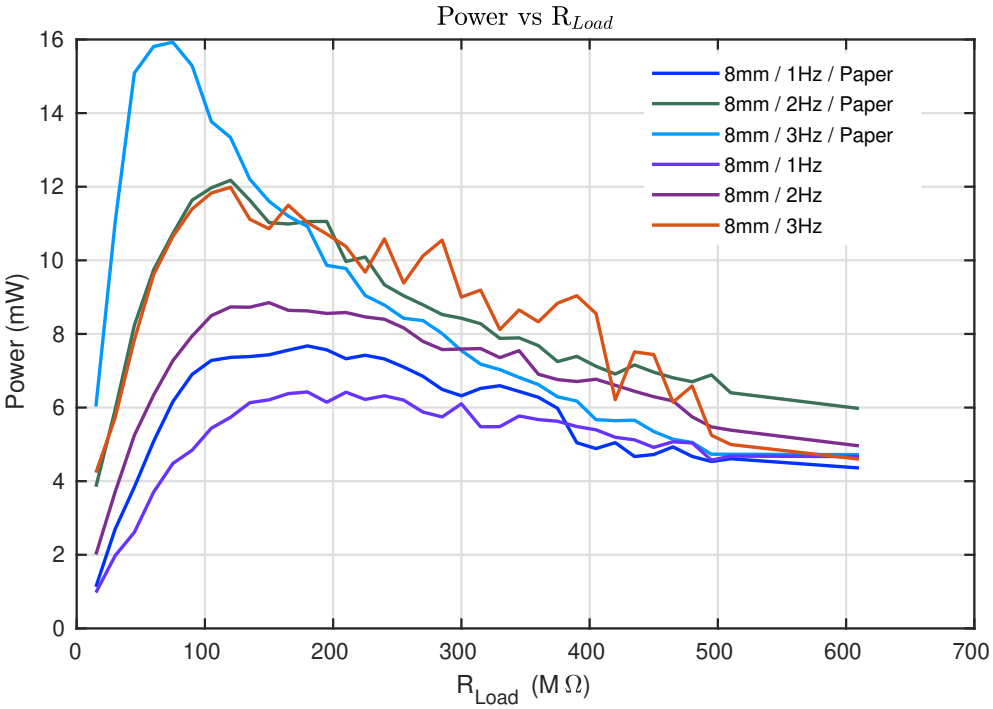

Figure 2.6. Measured power on resistive load for different frequencies, $x(t) = 8$ mm and triboelectrification with and without paper.

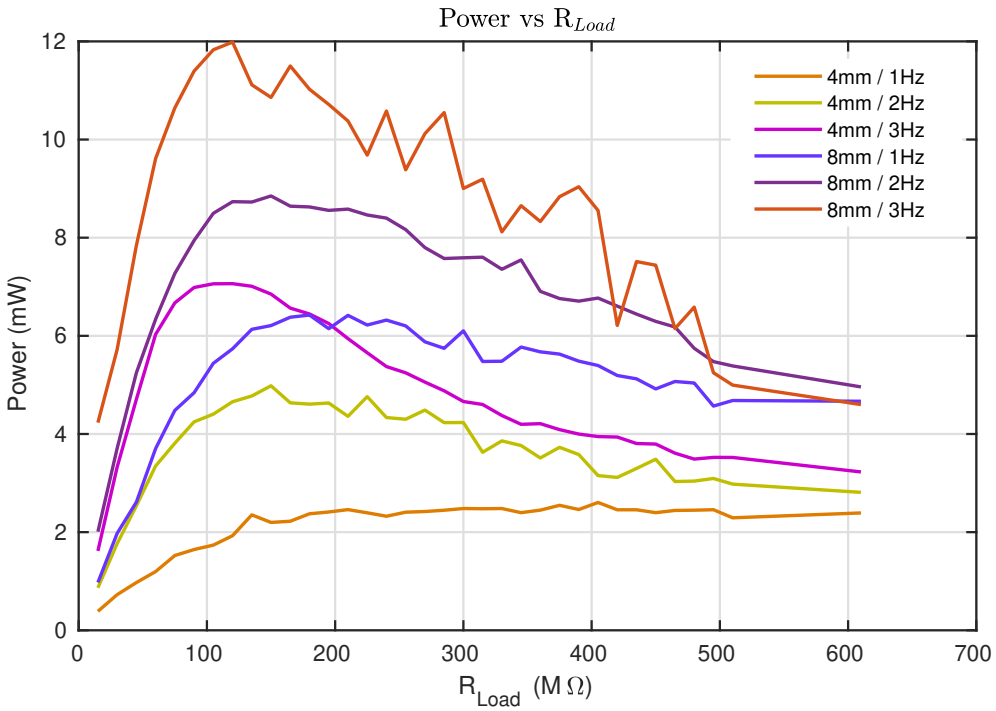

Figure 2.7. Measured power on resistive load for $x(t) = 4$ mm and $x(t) = 8$ mm.

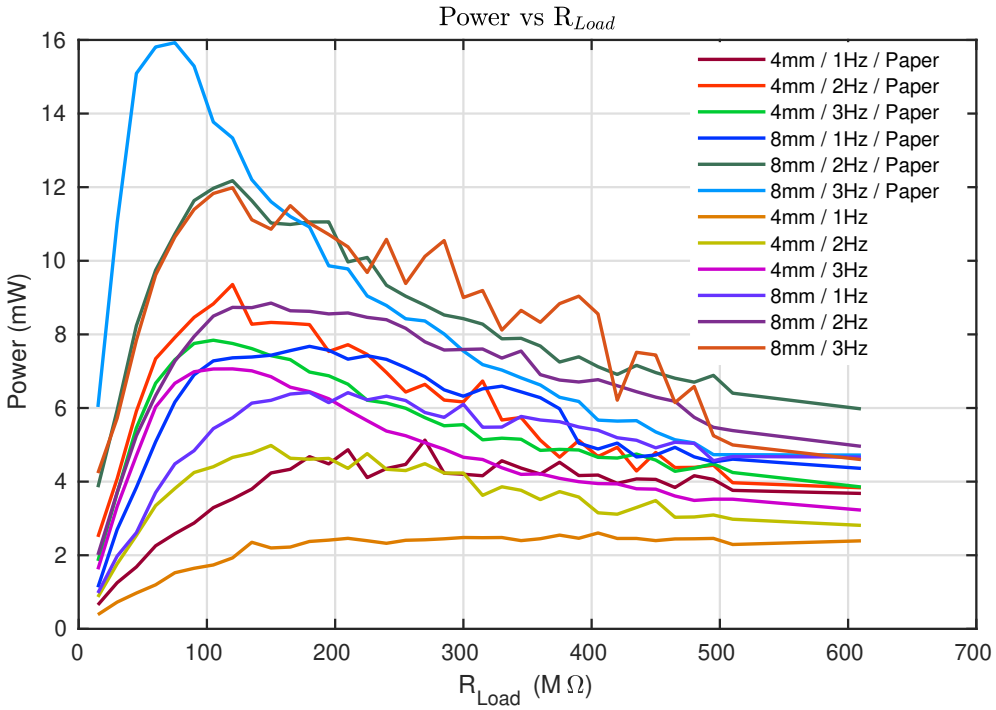

Figure 2.8. Measured power on resistive load for all cases.

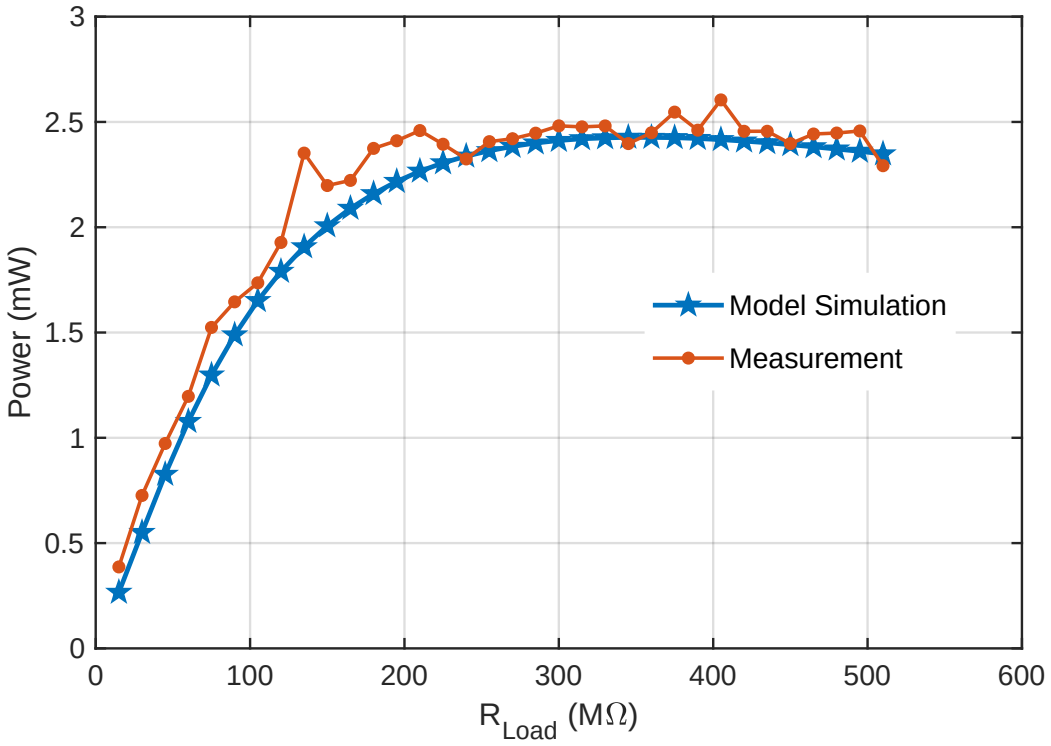

Figure 2.9. Model simulations that fit to the experimental power measurements made using 1 Hz mechanical motion.

According to model given in Figure 2.1, voltage generated by TENG (V_{TENG}) and its internal capacitance (C_{TENG}) can be described by the following equations:

$$V_{TENG} = \frac{\sigma x(t)}{\varepsilon_0} \tag{2.1}$$

$$C_{TENG} = \frac{\varepsilon_0 A}{(\frac{d}{\varepsilon_r}) + x(t)} \tag{2.2}$$

where d is the thickness, ε_0 is the permittivity of air, σ is the surface charge density, and ε_r the dielectric constant of the PTFE layer, A is the effective contact area between steel and PTFE surfaces, and $x(t)$ is the time-varying gap between steel electrode and PTFE. An energy harvester with $\sim$150 μm PTFE thickness d, 66.5 cm^2 effective area A, and maximum displacement distance of 8 mm between PTFE and steel surfaces

are used in measurements. These values are used to characterize triboelectric effect between steel and PTFE. Then, they are utilized to extract the surface change density. Surface charge density, σ, is extracted as $17.5 \times 10^{-6} C/m^2$ from the SPICE simulations that fit experimental power measurements made using 1 Hz mechanical motion, as shown in Figure 2.9. Table 2.1 shows the model parameters that are used in the simulations.

Table 2.1. Parameters used for modelling the TENG

Surface charge density	σ	$17.5 \times 10^{-6} C/m^2$
Effective contact area	A	66.5 cm^2
Thickness of the PTFE film	d	$\sim$150 μm
Dielectric constant of the PTFE film	ε_r	2.1
Permittivity of air	ε_0	$8.854 \times 10^{-12} F/m$
Maximum time variant gap	$x(t)$	8 mm

2.3. Comparison of full-bridge rectifier with parallel-SSHI rectifier

Full-bridge rectifiers (FBRs) are one of the most common interface circuits that are used to extract energy from harvesters. Figure 2.10 shows a conventional full-bridge rectifier connected to the TENG. The current of the TENG can be considered as a sinusoidal waveform;

$$i_{TENG} = I_{TENG} sin(\omega_{TENG} t) \tag{2.3}$$

where $\omega_{TENG} = 2\pi f_{TENG}$ and f_{TENG} is the motion frequency of the TENG [42]. The maximum power extraction from the piezoelectric or triboelectric harvester is only possible by a load with a conjugate impedance match. In this case, an inductor with an impedance of $L = 1/((\omega_{TENG})^2 C_{TENG})$ is needed to extract maximum power from the energy harvester. This impedance value is in the order of tens of Hs, which makes it impossible to implement in any real-life application. Therefore, theoretical maximum

power can be calculated as [42]:

$$P_{RECT,TH}(max) = \frac{(I_{TENG})^2 R_{TENG}}{8} = \frac{(Q_{TENG})^2 (V_{TENG})^2}{8R_{TENG}} \tag{2.4}$$

where V_{TENG} is the open-circuit voltage of the TENG, Q_{TENG} is the quality factor. These values can be expressed as $V_{TENG} = I_{TENG}/(\omega_{TENG} C_{TENG})$ and $Q_{TENG} = \omega_{TENG} C_{TENG} R_{TENG}$.

Several studies showed that full-bridge rectifiers cannot harvest energy efficiently due to the voltage drop, V_D, on the diodes and internal capacitance of the piezoelectric/triboelectric harvesters. The TENG current, i_{TENG}, first charges the internal variable capacitance C_{TENG} to the output voltage $V_{RECT} + 2V_D$, then flows through diodes to C_{RECT}. This current flow to C_{RECT} lasts until i_{TENG} changes direction. At this point, i_{TENG} discharges C_{TENG} and then charges in the opposite polarity until its voltage reaches $V_{RECT} + 2V_D$. The shaded areas in Figure 2.10 show energy loss of the system during the charging and discharging of the internal capacitance C_{TENG}. Active rectifiers, which generally consist of negative voltage converter in series with active diodes, decrease the voltage drop on diodes significantly to increase the efficiency of the power extraction.

Mathematical analysis from [42] shows the maximum obtainable power from the energy harvester in the case of the full-bridge rectifier with ideal diodes is

$$P_{RECT,FBR}(max) = C_{TENG}(V_{TENG})^2 f_{TENG} \tag{2.5}$$

The comparison of this power with the maximum obtainable power in the case of conjugate match, which is given in Equation (2.4), gives

$$\frac{P_{RECT,TH}(max)}{P_{RECT,FBR}(max)} = \frac{4}{\pi Q_{TENG}} \tag{2.6}$$

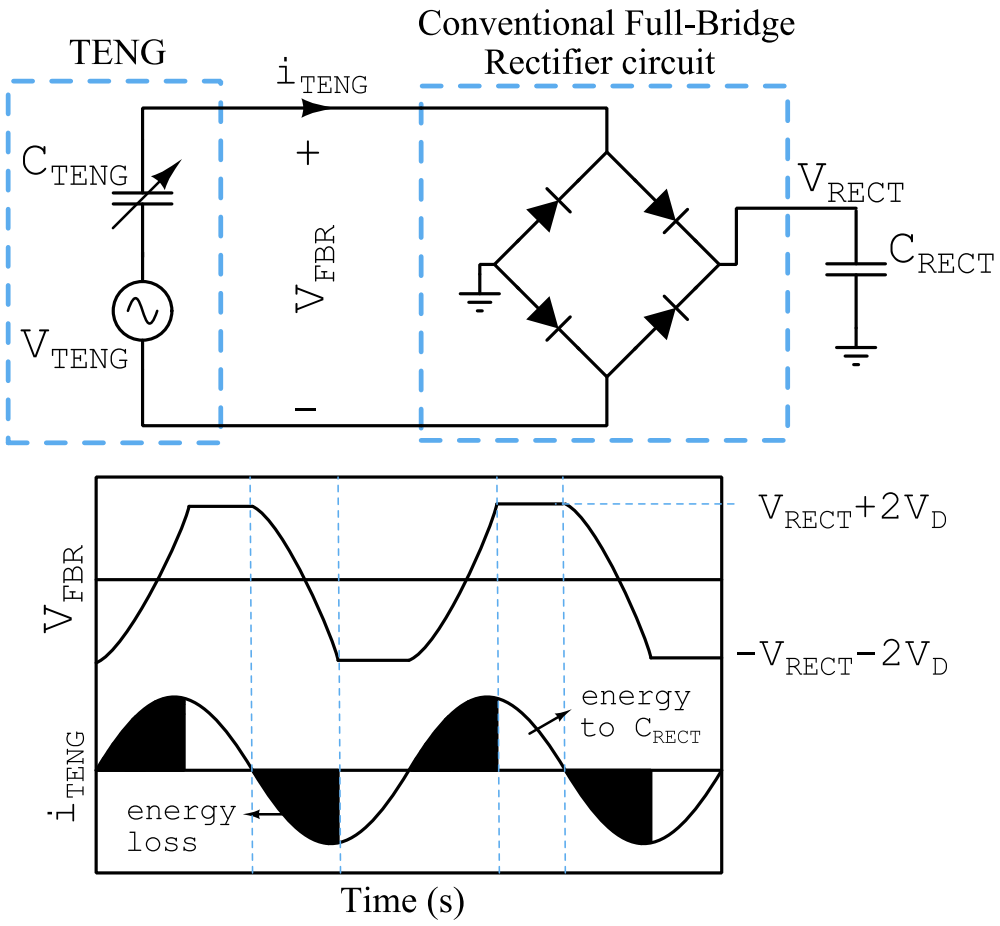

Figure 2.10. Conventional full-bridge rectifier connected to the TENG.

According to [42], the commercial piezoelectric harvester tested by them is capable of extracting %12.5 in the case of ideal diodes. When the non-ideal diodes with their internal voltage drop V_D are taken into account, this obtainable power from the energy harvester will be much smaller. Also, obtainable power from the energy harvester in the case of the non-ideal diode can be calculated as

$$P_{RECT,FBR} = 4C_{TENG}V_{TENG}f_{TENG}(V_{TENG} - V_{RECT} - 2V_D) \tag{2.7}$$

The parallel-SSHI technique, also known as bias-flip rectifier [19], has become a popular method due to its simplicity and efficient power extraction capability. It simply utilizes an inductor and a switch to bypass charging and discharging of the

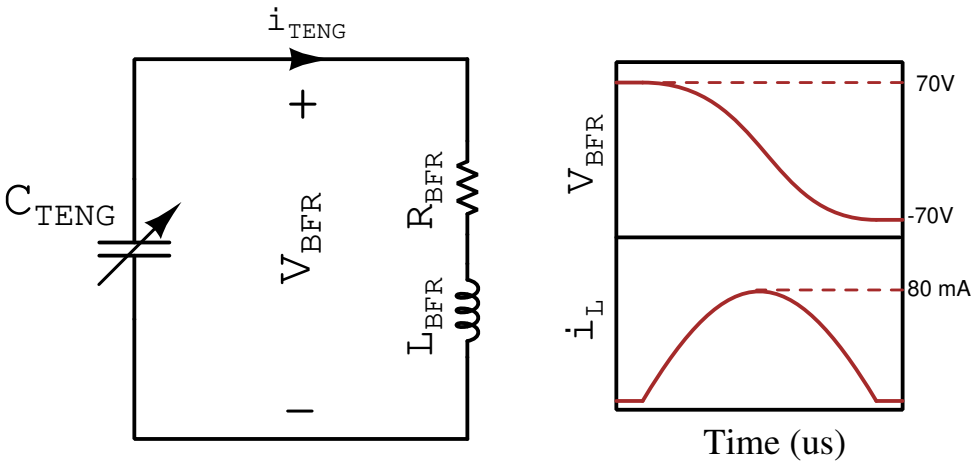

Figure 2.11. Resonance path on the bias flip rectifier network.

internal capacitance of the piezoelectric/triboelectric harvester by creating an LC resonant circuit, as shown in Figure 2.11. Figure 2.12 shows the basic version of the bias flip rectifier. The switch is closed when i_{TENG} changes direction and a current ramp up then down through the inductor. At the exact moment, when the current on the inductor turns back to zero, the switch is opened again. As a result, the voltage across the harvester legs, V_{BFR}, immediately flips from $V_{RECT} + 2V_D$ to $-(V_{RECT} + 2V_D)$ if Q of the LC tank is infinite. However, switch-on resistance and parasitic losses on the inductor prevent the ideal flipping of the rectifier's input voltages. Thus, as shown with the shaded areas in Figure 2.12, there is still some energy loss in the system due to the charging and discharging of the internal capacitance of the piezoelectric/triboelectric harvester. Nonetheless, the majority of the charge is transferred to the external capacitance C_{RECT}, and the final voltage across the TENG legs becomes

$$V_{BFR}(final) = -V_{RECT}e^{\frac{-\pi\beta}{\omega_{TENG}}} \tag{2.8}$$

where $\beta = R_{BFR}/2L_{BFR}$, $\omega_{TENG} = \sqrt{\omega_o^2 - \beta^2}$ and $\omega_o = 1\sqrt{L_{BFR}C_{TENG}}$. Finally, the derived extracted power by the bias-flip rectifier can be calculated with the following

equations [42]:

$$P_{RECT,FBR} = 2C_{TENG}V_{TENG}f_{TENG} \times \left(2V_{TENG} - (V_{RECT} + 2V_D)(1 - e^{-\tau}) - \frac{\pi k_{BFR}(V_{RECT} + 2V_D)}{Q_{TENG}}\right) \quad (2.9)$$

where

$$k_{BFR} = \frac{(V_{TENG} + (V_{RECT} + 2V_D)e^{-\tau})\omega_{TENG}t_1}{\pi(V_{RECT} + 2V_D)} - \frac{V_{TENG}sin\omega_{TENG}t_1}{\pi(V_{RECT} + 2V_D)} - \frac{\pi - \omega_{TENG}t_1}{\pi} \quad (2.10)$$

and

$$\omega_{TENG}t_1 = cos^{-1}\left(1 - \frac{(V_{RECT} + 2V_D)(1 - e^{-\tau})}{V_{TENG}}\right) \quad (2.11)$$

The maximum output voltage obtainable from harvester with the bias-flip rectifier can be calculated from Equation (2.9):

$$V_{RECT,BFR}(max) = \frac{V_{TENG}}{1 - e^{-\tau} + \frac{\pi k_{BFR}}{Q_{TENG}}} - V_D \quad (2.12)$$

In [42], a new term Q_{BFR} is introduced as a new quality factor that combines quality factors of the TENG and resonant path of C_{TENG} and L_{BFR}:

$$Q_{BFR} = \frac{1}{1 - e^{-\tau} + \frac{\pi k_{BFR}}{Q_{TENG}}} \quad (2.13)$$

Hence, the maximum power that bias-flip rectifier can extract from the TENG is calculated as:

$$P_{RECT,BFR}(max) = 2C_{TENG}\left(V_{TENG} - \frac{V_D}{Q_{BFR}}\right)^2 Q_{BFR}f_{TENG} \quad (2.14)$$

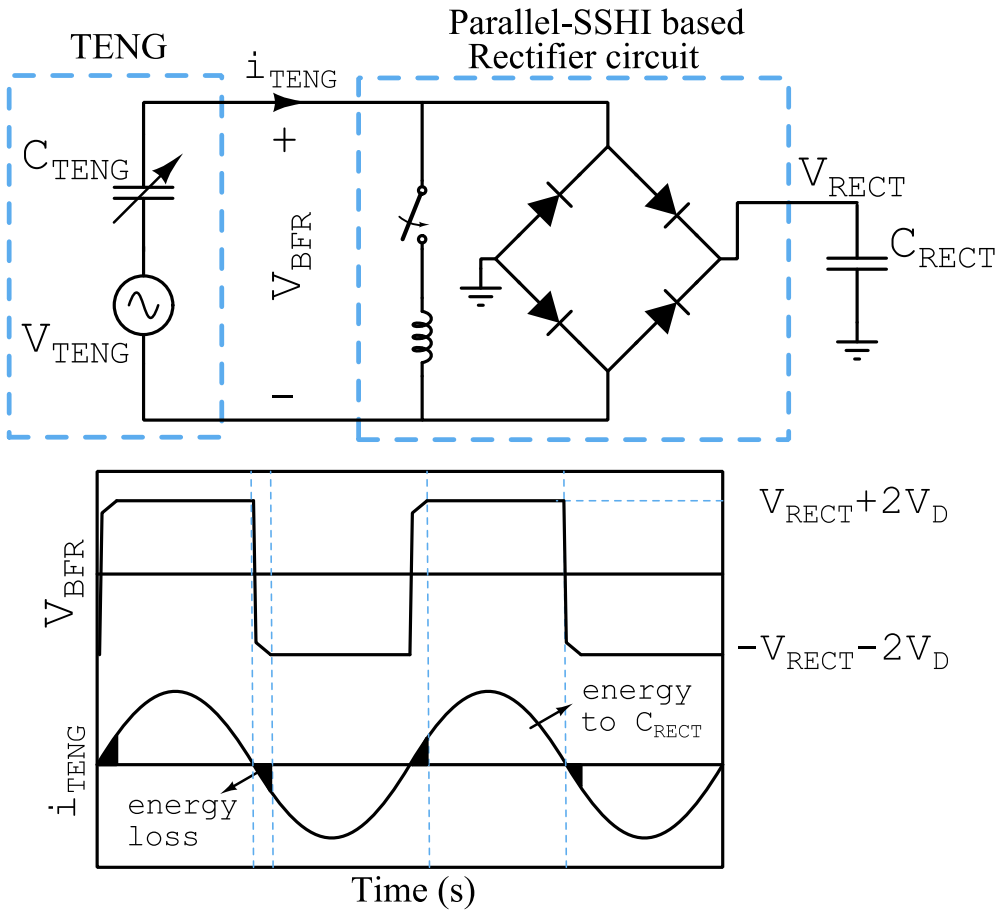

Figure 2.12. Parallel-SSHI rectifier connected to the TENG.

Until now, the power capabilities of the full-bridge rectifier and the bias-flip rectifier are derived through the Equations (2.3)-(2.15). Their maximum power extraction capabilities will give a hint about how to proceed with the rest of the designs. However, the maximum power extracted from the TENG by the full-bridge rectifier can be derived further

$$P_{RECT,FBR}(max) = C_{TENG}(V_{TENG} - 2V_D)^2 f_{TENG} \tag{2.15}$$

By taking Equation (2.15) and (2.14) into account, proportion to each other becomes

$$\frac{P_{RECT,BFR}(max)}{P_{RECT,FBR}(max)} = \frac{2Q_{BFR}\left(V_{TENG} - \frac{V_D}{Q_{BFR}}\right)^2}{(V_{TENG} - 2V_D)^2} \tag{2.16}$$

As it can be calculated from the above expression, the bias-flip rectification scheme improves the power extraction by a factor of 3 to 8 according to various studies in the literature [18–22]. However, all of these studies focus on piezoelectric harvesters, which have limited open-circuit voltages. This limitation could be both disadvantageous and beneficial for energy harvesting. When open circuit voltage is low, the voltage drop on the diodes reduces the harvested power drastically. However, nonlinear harvesting methods like parallel-SSHI or SECE can be used to achieve 3 to 8 times more power harvesting by multiplying the output voltage on the external capacitor by a few folds.

Moreover, if the harvester is triboelectric rather than piezoelectric, the open-circuit voltage can reach tens-to-thousands of volts, which is advantageous but brings in some design challenges. Consequently, with a proper design, high power densities can be obtained from the triboelectric harvesters. [39] used MPPT and HV CMOS process to implement an on-chip triboelectric energy harvester system. In [41], the parallel-SSHI method is used for the first time with the triboelectric energy harvester with off-chip components, which achieves 2.43x more power harvesting compared to the full-bridge rectifier harvester. In the next section, a new parallel-SSHI method and its implementation with on-chip components are explained in detail.

3. PARALLEL-SSHI IMPLEMENTATION

SSHI or SECE type energy harvesters are best suitable when the open-circuit voltage is low as in piezoelectric harvesters. Triboelectric harvesters may have very high open-circuit voltages. In this case, energy extraction becomes dependent on off-chip components, making triboelectric harvester less preferable due to larger size and weight. In recent years, advances in high-voltage processes have opened a gate for triboelectric harvesters to become small, lightweight, and preferable than piezoelectric harvesters. The design of the harvester in this work, shown in Figure 1.1, is implemented in 0.18 μm HV BCD process. This technology node offers devices that can operate up to 70 V with a maximum gate-to-source voltage of 5 V limited by the oxide breakdown. Diodes shown in Figure 3.1 are implemented with the body diodes of 70 V NMOS transistors that are turned-off. Hence, the maximum voltage at the input of the buck DC-DC converter is limited by the body diode breakdown voltage of these transistors.

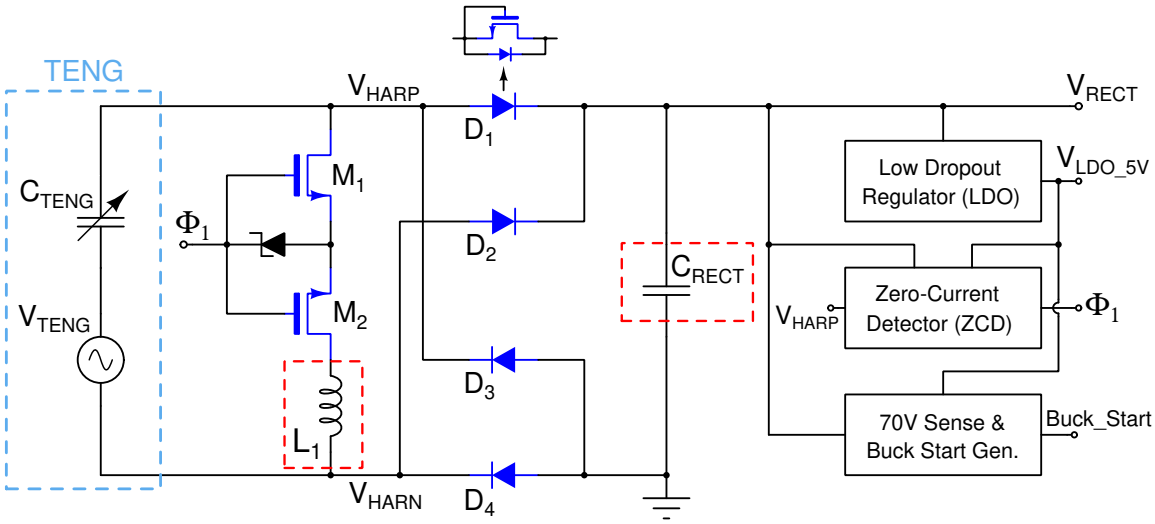

Figure 3.1. Proposed parallel-SSHI implementation.

The TENG manufactured in our laboratory works with press-and-release mechanical motions that have frequencies from 1 Hz to 5 Hz. It sends power to the buck converter discretely with peak power levels at the time instances corresponding

to press and release. However, the buck converter demands continuous power. Thus, first charging external capacitor C_{RECT} to 70 V and then converting this voltage via a series of DC-DC converters to a low voltage is the best option to harvest energy from the TENG. Our design strategy is to realize the charging of the C_{RECT} to 70 V in at most three cycles, and then to detect the 70 V level to generate a buck start signal. Figure 3.1 shows the proposed parallel-SSHI implementation. An off-chip 1 mH inductor, L_1, and an off-chip 5 nF capacitor, C_{RECT}, are used. In the rest of this thesis, all the external components are illustrated with the dashed red rectangles. All the transistors and diodes, including zener diodes are on-chip from manufacturer's physical design-kit library, and high-voltage components are colored blue. Furthermore, unless stated explicitly, all other transistors in the proposed design have thick oxides, making them operable with 5 V.

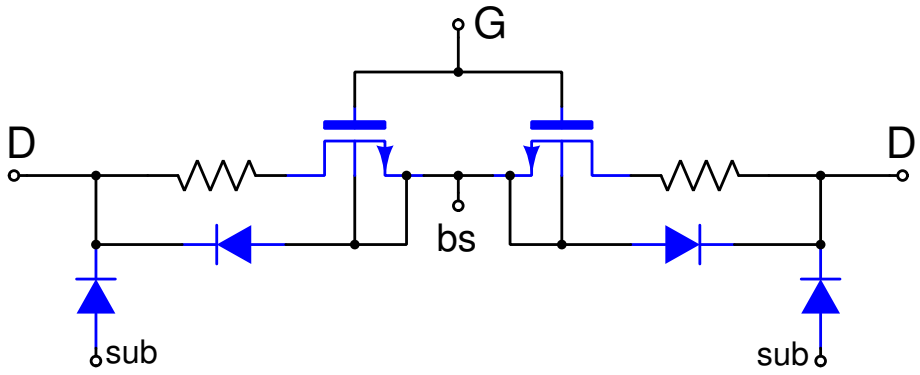

Figure 3.2. High-voltage switch realization using two unilateral NMOS transistors.

The transistors used as high voltage (HV) switches are unilateral; two of them are connected as shown in Figure 3.2 to take advantage of their internal high voltage diodes to block the current flow in the off state. Switching these transistors ON and OFF at exact peak values of V_{TENG} via ϕ_1 signal results in V_{HARP} to flip from $-V_D$ to $V_{RECT} + V_D$ and V_{HARN} to flip from $V_{RECT} + V_D$ to $-V_D$, or vice versa, which keeps $V_{HARP} - V_{HARN}$ difference, V_{BFR}, between $\pm(V_{RECT} + 2V_D)$ where V_D is the voltage drop over the body diodes of 70 V NMOS transistors. It should be noted that a zener diode is connected between the gate and source terminals of the switch transistors. When the flipping is completed, the gate voltage of the transistors is pulled down to

the ground, and source voltage cannot response that fast. Hence, the source-to-gate voltage rises above 5 V, which causes the gate-oxide of the transistor to breakdown. This zener diode allows the source to fully discharge to the ground and clamp the gate-source voltage above a certain value to protect gate oxide against breakdown. In order to generate a proper control signal, ϕ_1, a zero current detector circuit is needed to sense the peak values of V_{HARP}. Since the system does not have any external steady power source, a self-start-up low dropout regulator is designed to obtain 5 V from the V_{RECT} to power up the zero current detection circuits, and the other circuits that are used for 70 V sense and buck start signal generation.

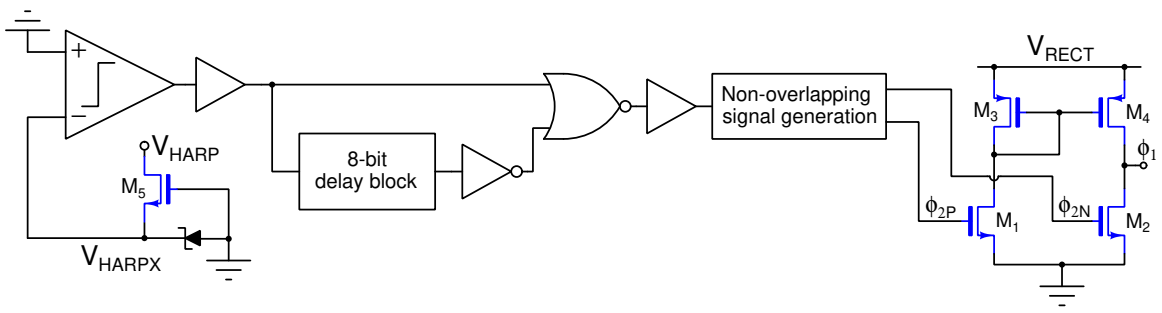

Figure 3.3. Overall zero-current detector (ZCD) circuitry.

3.1. Zero Current Detector

The main challenge in the design of the zero current detector is the generation of accurate switch control signals. The control signal can be generated by monitoring the current through the inductor. Since voltage leads current by a 90-degree phase, voltage peaks of the V_{TENG} are monitored to detect the zero-crossings. In [19], a continuous-time comparator is used to detect the zero-crossing of the piezoelectric current by looking at the voltage peaks. A similar approach, shown in Figure 3.3, is adapted for the solution used in this thesis. The comparator is self-biased hysteresis type and consumes only 16 nA current from the 5 V coming from the LDO. Hysteresis is adjusted to prevent fake detections for up to a few millihundred volts in the comparator's inputs. Thus, power losses due to possible wrong switching activity are prevented. Another aspect here is the delay trade-off preference made in favor of the low power property

of the comparator. The TENG's working frequency is in the hertz range, whereas the comparator works at 250 Hz in the worst case, which is acceptable. The schematic and layout of the comparator are given in Figure 3.4 and Figure 3.5, respectively.

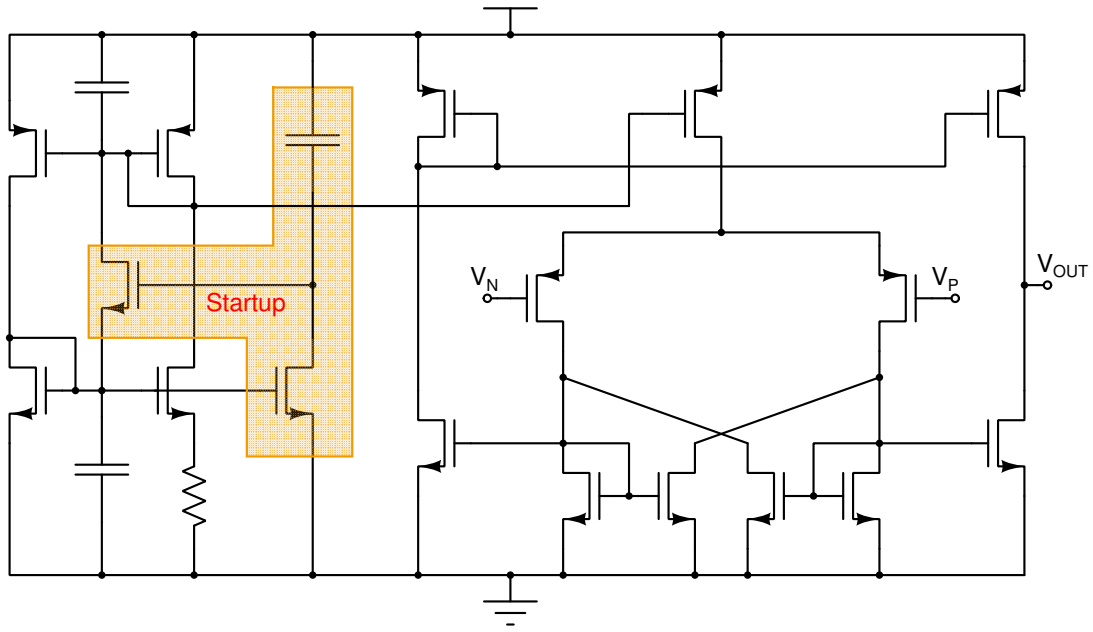

Figure 3.4. Schematic of the comparator used for zero current detection.

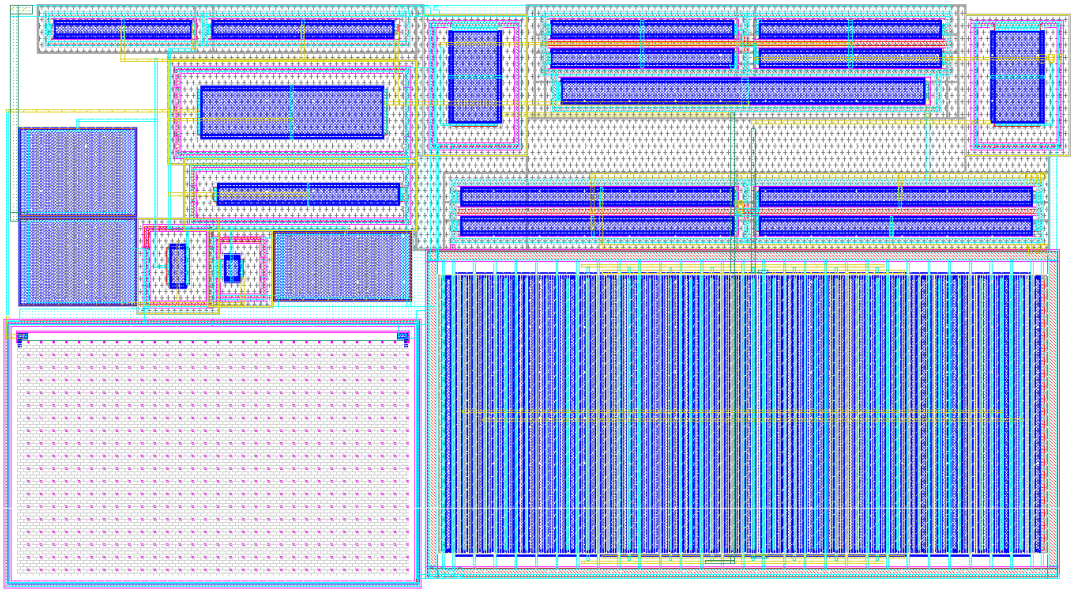

Figure 3.5. Layout of the comparator used for zero current detection.

For maximal flipping, which is described in the previous section, the inductor needs to pass current in one direction during half of the resonance period, $T/2 = \pi\sqrt{LC_{TENG}}$, formed by the external inductor and internal capacitance. This scheme is shown in Figure 2.11. Equation (2.1) and (2.2) show that the variable internal capacitance C_{TENG} takes its maximum and minimum values at peak values of V_{TENG}. Hence, the time required by the inductor to pass current differs from each other at the two peak values of V_{TENG}. The latest version of the TENG manufactured in our laboratory has a very small internal capacitance (7.3 pF from (2.2)) at the maximum separation point, which results in very low efficiency if it is switched at this peak separation. For this purpose, only the V_{HARP} voltage is monitored to track the zero-current passing at the other peak values of V_{TENG}. A zener diode and an OFF-state HV transistor, namely M_5 from the Figure 3.3, are used to track the V_{HARP} voltage and limit it to V_{HARPX}, which does not exceed 5 V at the input gate of the comparator because of the zener diode. This behavior of the limiting circuit is justified with the simulation, as shown in Figure 3.6, and its layout is given in Figure 3.7.

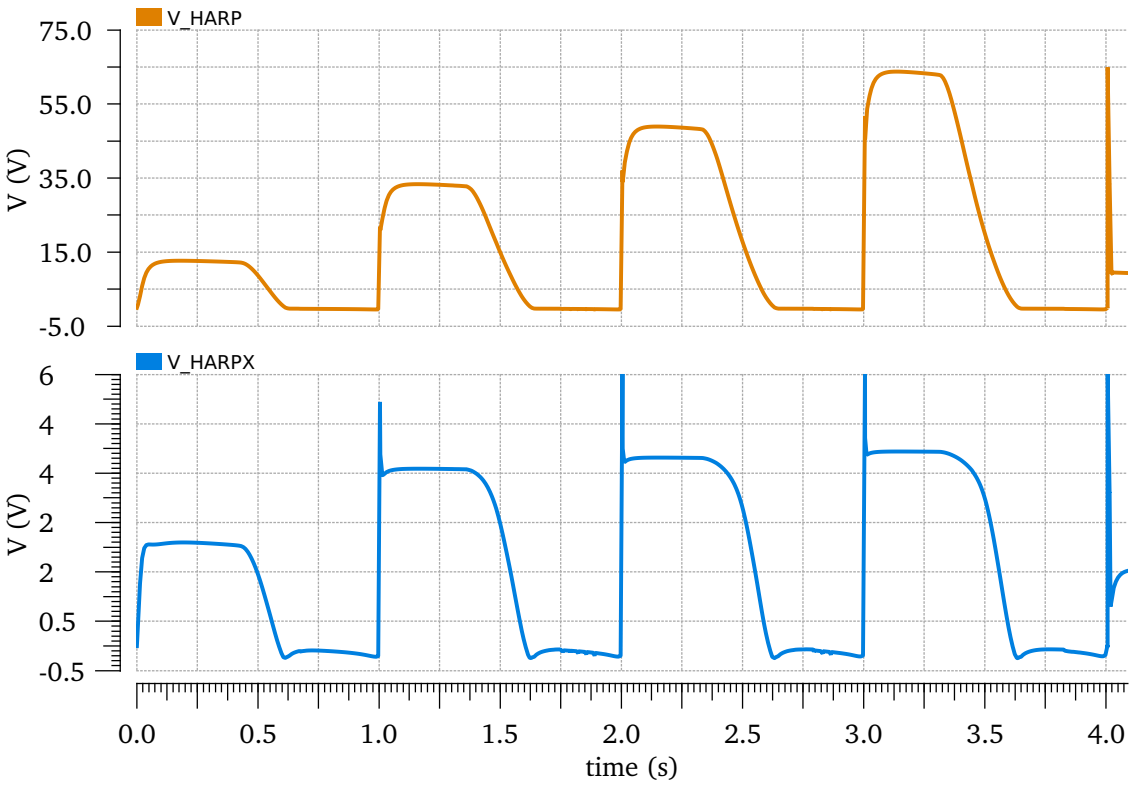

Figure 3.6. Simulation result of the V_{HARP} limitation circuit.

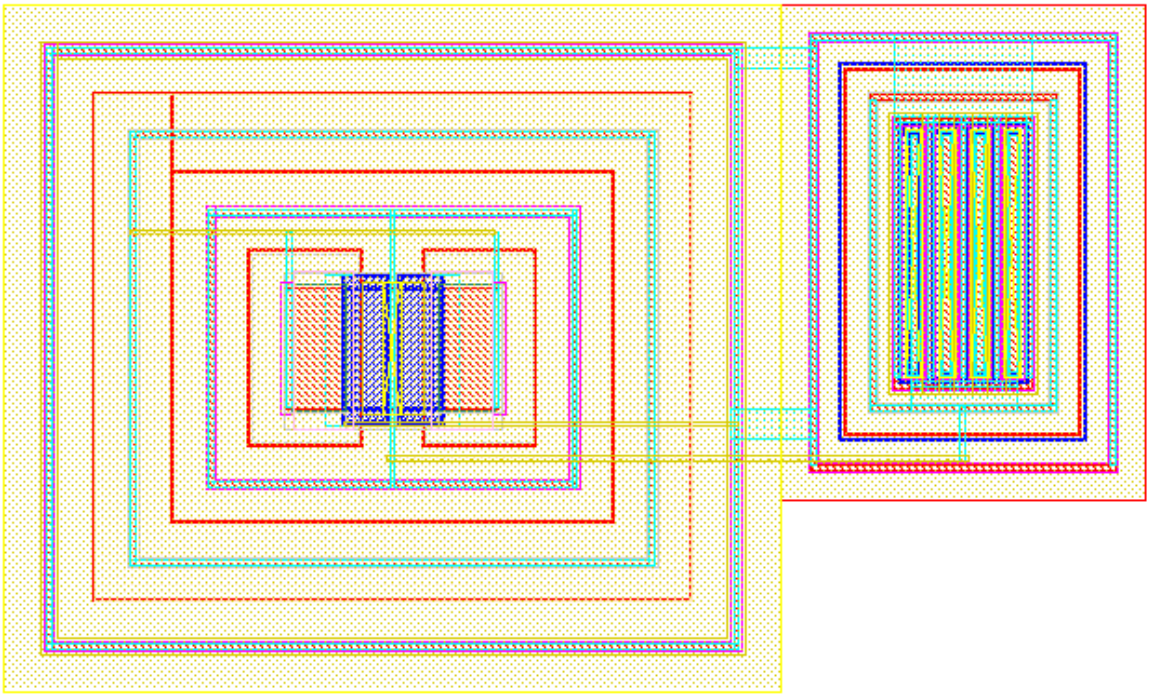

Figure 3.7. Layout of the V_{HARP} limitation circuit.

The comparator senses the zero current crossing when V_{HARPX} voltage is close enough to zero volt, and its output with its delayed form are fed to a NOR gate to generate a pulse with a width of $T/2 = \pi\sqrt{LC_{TENG}}$. The timing requirement is achieved with a programmable 8-bit delay block, which consists of a 4-bit inverter chain based coarse delay block and 4-bit RC time constant-based fine delay block. Their schematics and layouts are shown in Figure 3.8, Figure 3.9, Figure 3.10, and Figure 3.11, respectively. All the delay circuits and digital circuits consume 6 nA current from the 5 V coming from the LDO. These control bits, along with any other control implemented in the design, are set by integrated shift registers that we program with an I2C interface.

Additionally, the above delay blocks should meet accuracy and long delay time requirements simultaneously. Fine delay block is based on RC time constant delay and has a resolution of 50 ns, which makes a total of 800 ns delay. This 800 ns delay length is not enough for the bias-flipping switching activity. Thus, the coarse delay block is combined with the fine delay block in order to meet both accuracy and long delay requirements. The delay elements on coarse delay block consist of 14 inverters

whose transistor lengths are very long, which provide a 400 ns long delay. This means a total of 6.8 μs delay is obtained from the combination of fine and coarse delay blocks, which have 800 ns and 6 μs total delays, respectively.

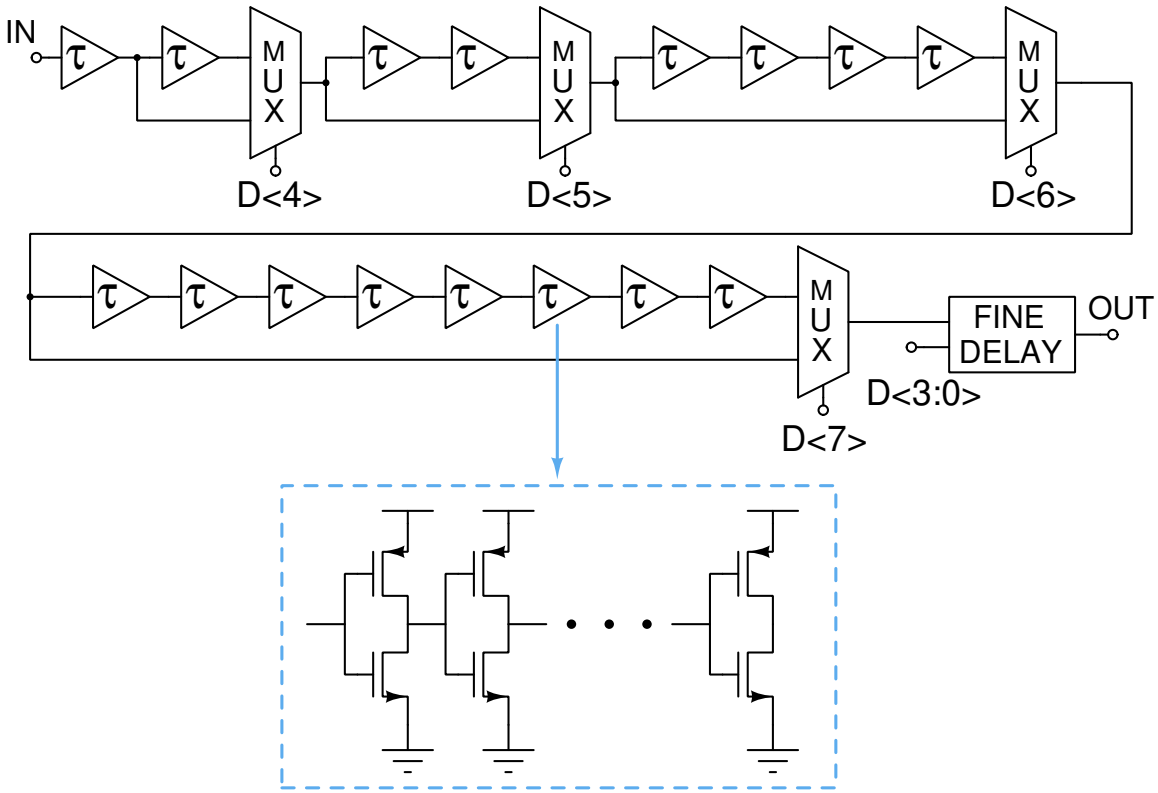

Figure 3.8. 8-bit inverter chain based coarse delay block.

The generated pulse cannot be applied directly to the switch transistors' gates, as shown in Figure 3.1 since the source voltages of the switches change during the flipping activity. In order to keep switch transistors ON or OFF, the gate-to-source voltage needs to be 5 V or 0 V, respectively. The differential amplifier shown in Figure 3.3 is used to generate a level-shifted control signal to keep the gate-to-source voltage of the switches constant by tracking the source terminal as it charges up when the switches turn on. As shown in Figure 3.3, zero-current detector circuits generate two control signals, namely ϕ_{2P} and ϕ_{2N}. When a zero-current is detected, ϕ_{2P} and ϕ_{2N} signals are set to logic '1' and '0', respectively. In this case, transistors M_1 and M_3 generate a current mirrored by M_4 transistor to ϕ_1 port to charge up the gate capacitances of the switch transistors in Figure 3.1. After a time period equals to $T/2 = \pi\sqrt{LC_{TENG}}$

is passed, ϕ_{2P} and ϕ_{2N} signals are set to logic '0' and '1', respectively. In this case, no longer a current is generated by M_1 and M_3 transistors, and a very large transistor, namely M_2, immediately pulls down the ϕ_1 port to ground, which turns off the switch transistors. Hence, the flipping process is completed, and the transistors M_1, M_3, and M_4 are powered down by ϕ_{2P} to eliminate unnecessary constant current consumption. This scheme is implemented to keep the gate-source voltage of the switch transistors less than 5 V so that oxide breakdown is prevented while allowing a full flipping. If the switch transistors' gate-source voltage exceeds the zener reverse breakdown voltage, sources of the switch transistors are pulled up by the zener diode path.

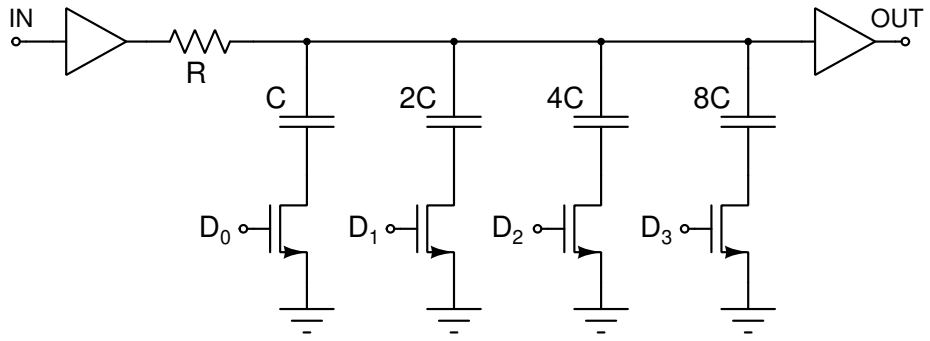

Figure 3.9. 4-bit RC delay based fine delay block.

The above working scheme is justified with the simulations. In Figure 3.12, the circuits are operated for several cycles to observe charging of the external capacitor C_{RECT} to 70 V. Zero-cross detection occurs every cycle and current passes through the external inductor. We observe the V_{HARP} to flip from $-V_D$ to $V_{RECT}+V_D$ and V_{HARN} to flip from $V_{RECT}+V_D$ to $-V_D$, or vice versa. We also observe the $V_{HARP}-V_{HARN}$ difference, which is stated as V_{BFR}. When the V_{RECT}, the voltage on the C_{RECT}, reaches to 70 V, a buck start signal is generated, and 70-to-10 V down conversion is realized by the buck converter. In Figure 3.13, the changes in the TENG legs are shown during the bias-flipping activity. Moreover, the current on the external inductor along with the ϕ_1 is shown. The significant point here is the inductor current is very similar to the ideal waveform shown in Figure 2.11. The overall zero-crossing detector circuitry layout is given in Figure 3.14, which also shows the HV transistors' separation distances that are required to prevent possible latch-ups.

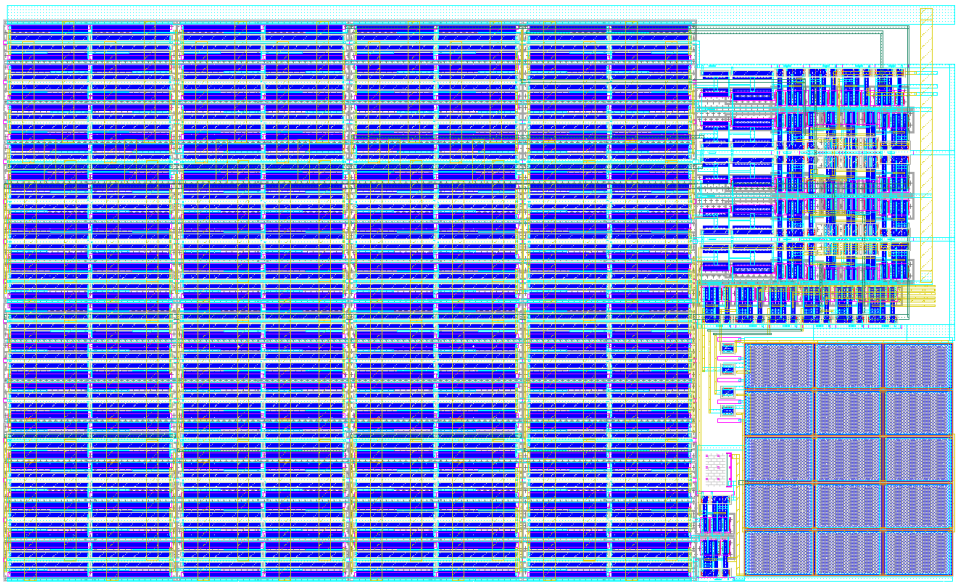

Figure 3.10. Layout of the 8-bit inverter chain based coarse delay block.

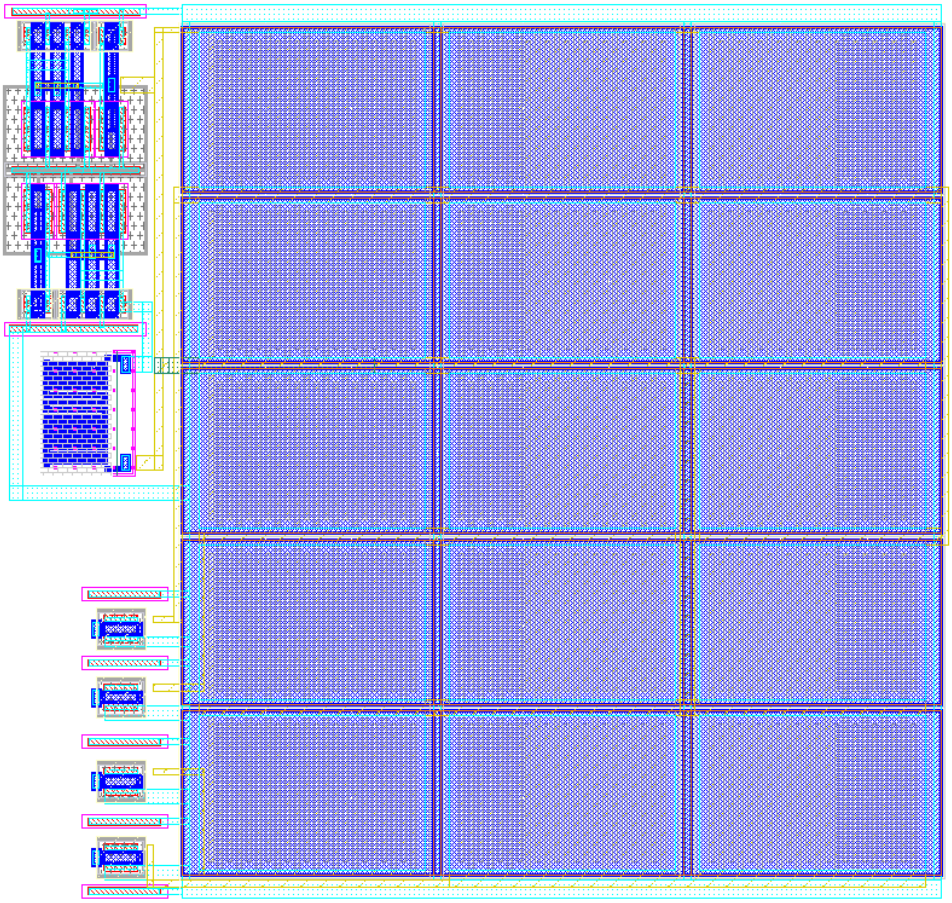

Figure 3.11. Layout of the 4-bit RC delay based fine delay block.

Figure 3.12. Simulation of the parallel-SSHI method.

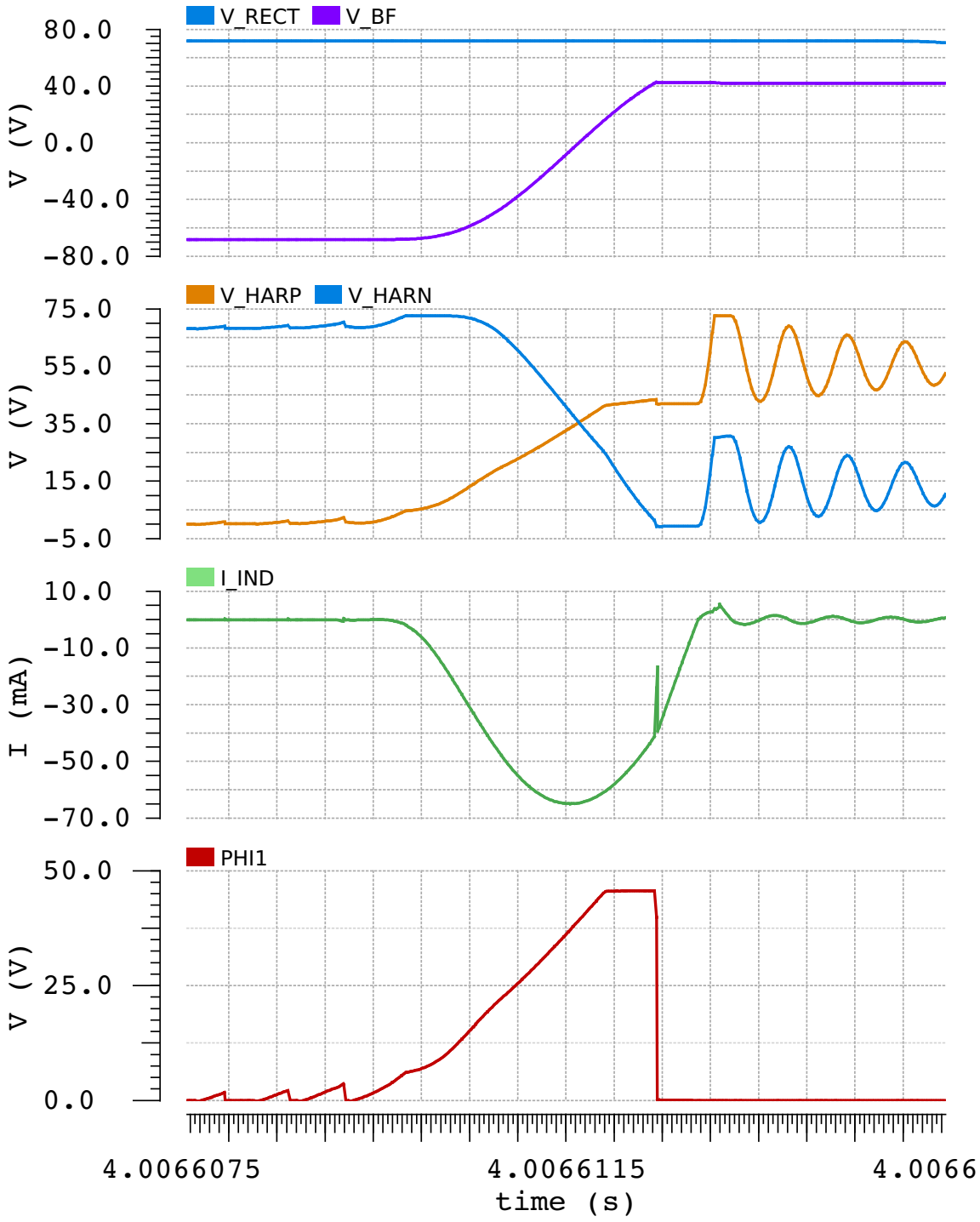

Figure 3.13. A close looking up to the zero-cross detection and bias-flipping activity.

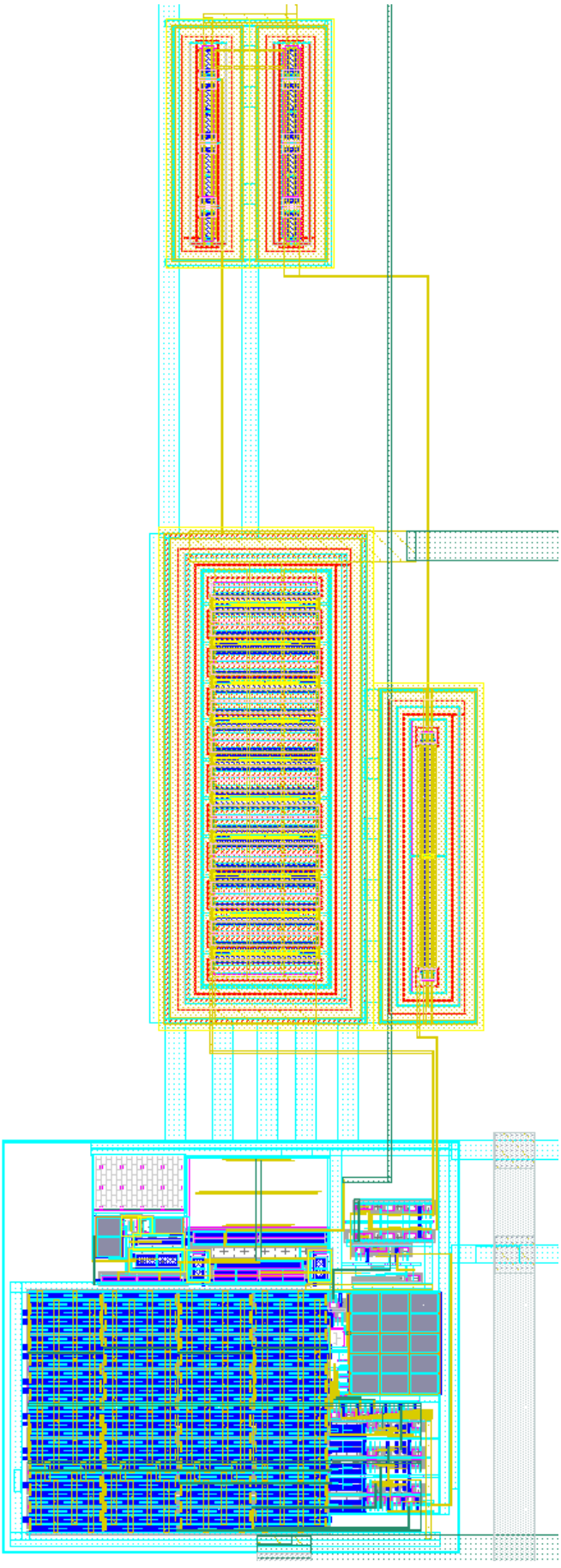

Figure 3.14. Layout of the overall zero-current detector (ZCD) circuitry.

3.2. Low Dropout Regulator

As previously explained, the energy produced from our TENG is initially stored on an external capacitor, and it will not deliver any power to the buck converter in the early press-release cycles of the mechanical motion. When the voltage level on the external capacitor reaches 70 V, typically in three cycles, a start signal is generated to power up the buck converter and the switched-capacitor DC-DC converter. However, for maximum power extraction from the TENG, the zero current detector needs to be running all the time, which results in a constant 5 V supply requirement. The start signal generation circuits also require a 5 V supply to track and sense the 70 V levels. For this reason, an LDO that is supplied from the stored energy on the external capacitor is used to generate a constant 5 V.

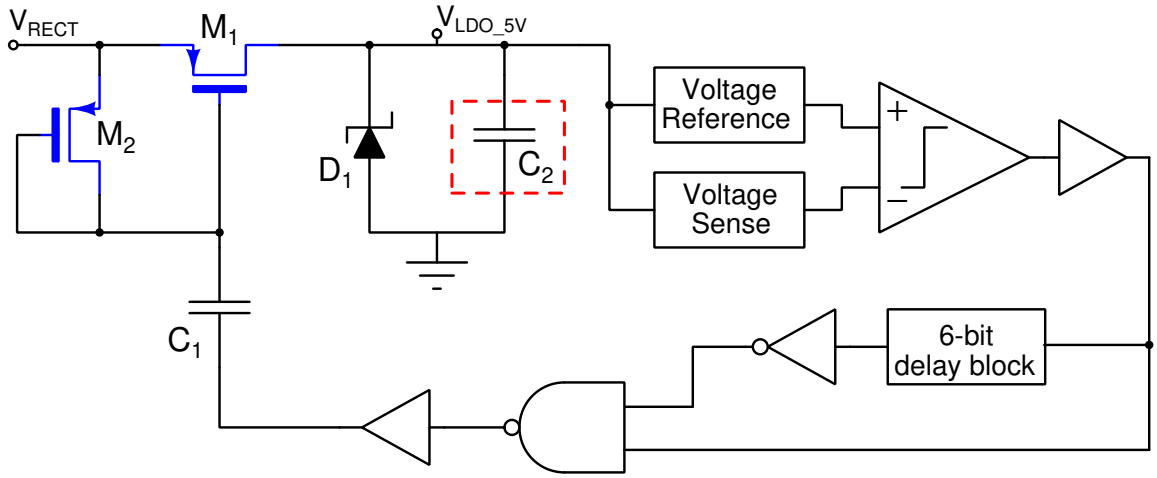

Figure 3.15. Low dropout regulator circuitry to power internal parallel-SSHI circuits.

Low dropout regulators are commonly used in the literature for voltage regulation, and they are preferable to other DC-DC converters due to simplicity, size, and lack of switching noise. LDOs do not use large inductors or transformers and consist of a simple error amplifier and an output stage. On the contrary, these types of regulators have lower power efficiency than the switching type regulators. Ease of implementation of the low dropout regulator and the fact that its ability to supply a very

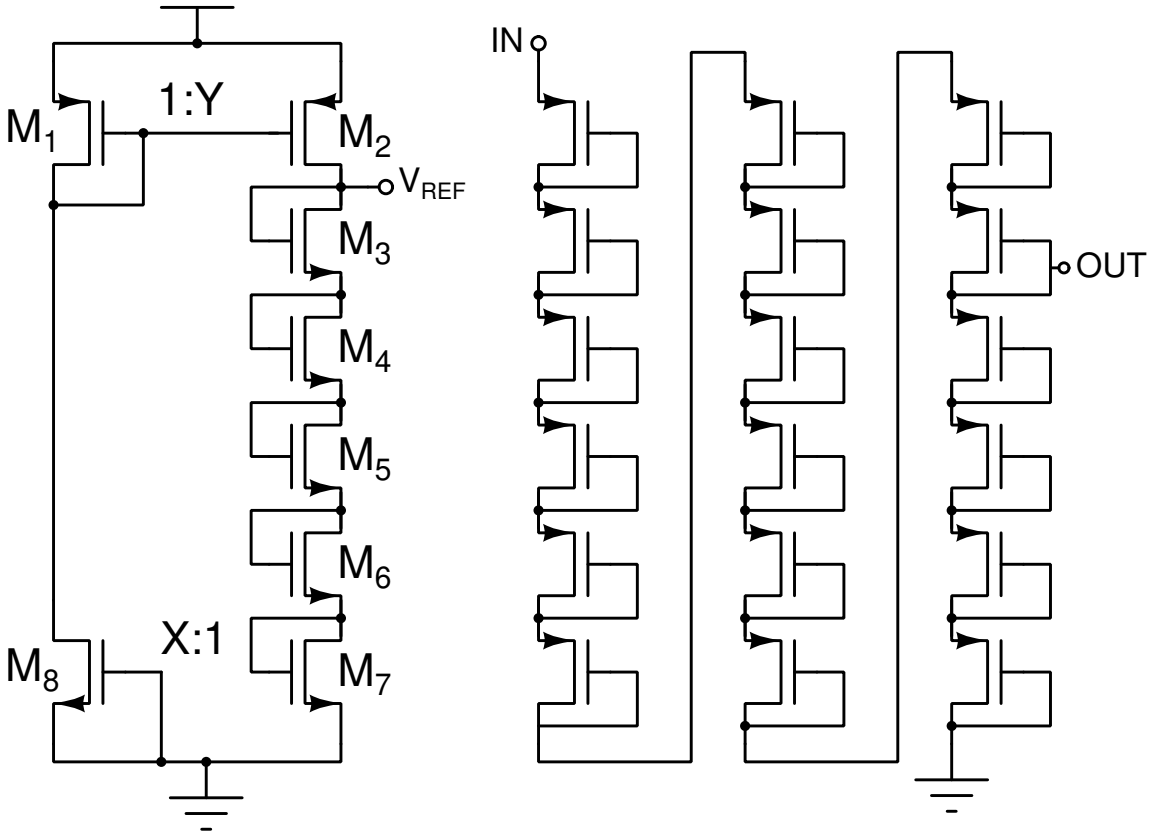

Figure 3.16. Voltage reference circuit (left) and voltage sense circuit (right).

low amount of power makes the low dropout regulator more suitable to be used here. The adopted version, shown in Figure 3.15, has unique differences from what is in the literature. The switch, M_1, is a high voltage transistor, and its allowed gate-source voltage is limited to only 5 V. Therefore, a level shifter is required to turn on and off this transistor. Instead of conventional power-hungry and large area level shifters, a high voltage metal-on-metal capacitor, C_1, and long length, diode-connected high voltage transistor, M_2, are used as a level shifter. M_2 transistor slowly charges the C_1 capacitor at the gate to the source voltage of the switch transistor,M_1. The digital output of the system connected to the bottom plate of the capacitor is 5 V as default. When the voltage on the off-chip thin film high voltage output capacitor falls below a specific value determined by a reference circuit, the comparator's output toggles high. This causes a 0 V pulse to be generated at the bottom plate of the capacitor since the output of the comparator is NANDed with a delayed version of itself. This leads

to the capacitor's top plate dropping 5 V due to capacitive coupling and turning on the switch transistor, which charges the output capacitor to the desired value. The maximum value of the output voltage is controlled with a 6-bit delay block by adjusting the generated pulse width. Additionally, an on-chip zener diode, D_1, which limits the maximum attainable voltage, is placed in shunt with the output to ensure that the devices are protected against breakdown even if the required delay is set wrong. Moreover, it does not play any role in voltage regulation.

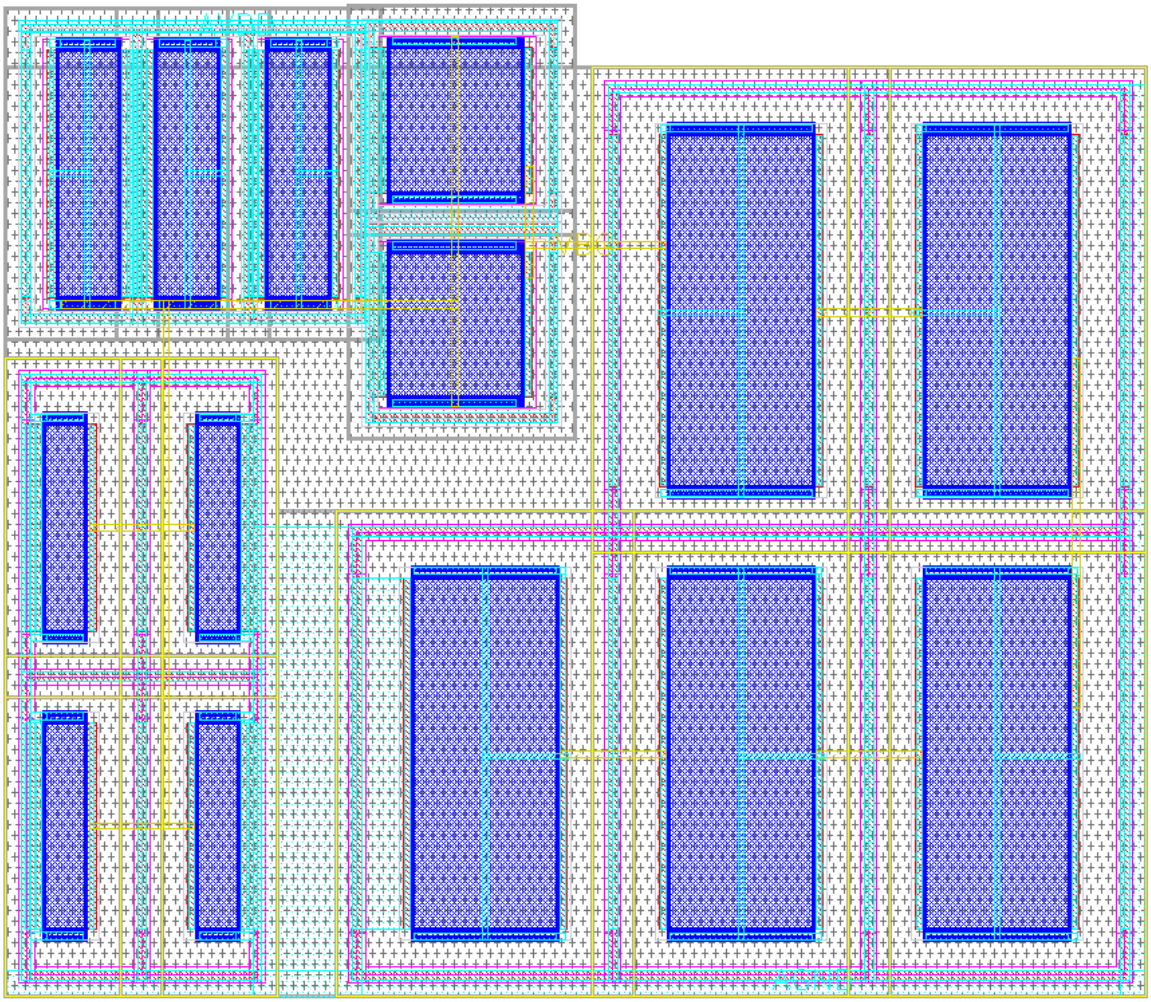

Figure 3.17. Layout of the voltage reference circuit.

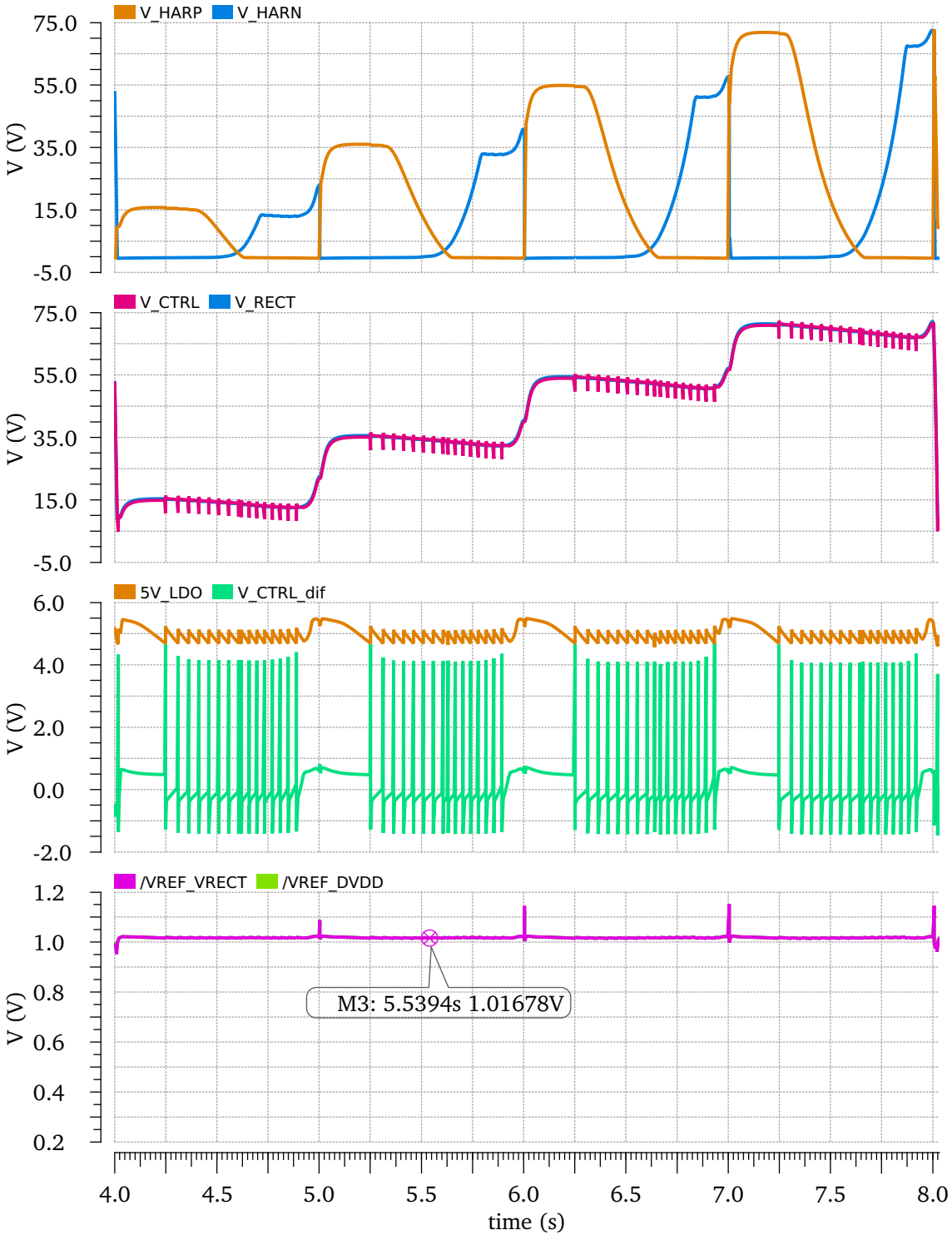

Figure 3.18. Simulation of the low dropout (LDO) circuit.

The operation of the low dropout regulation is validated with the post-layout simulations, as shown in Figure 3.18. V_{CTRL} and $V_{CTRL,diff}$ signals are the voltage level of the upper plate of the high voltage metal-on-metal capacitor, C_1, and the difference between the gate-source voltage of the switch transistor, M_1, respectively. As it is shown in the simulation results, V_{CTRL} signal follows the V_{RECT} signal. When the voltage on the external capacitance, C_2, drops a pre-defined voltage, the comparator sends a switch 'ON' signal to enable charging of the external capacitance. The voltage on the external capacitance is shown as $V_{LDO_{5V}}$ in Figure 3.18. The upper limit of the regulator output voltage is adjusted by switch 'ON' time, set by the 6-bit delay block to keep the voltage on the external capacitance acceptable voltage range, bounded to 4.8 V and 5.2 V on lower and upper boundaries, respectively. This limit can be changed by programming the 6-bit delay block externally through the I2C interface for optimization.

Another point in the above simulation result is the excessive rises in the V_{LDO_5V}. If it is followed from the Figure 3.18, it can be seen that just before and after the switching activity on the bias-flip switches, the voltage level increases in the V_{RECT} due to the charging of the external capacitance where TENG plates are. Therefore, the stress on the switch transistor, M_1, increases and leaks current to the external capacitance, C_2. This leakage cause the voltage level of V_{LDO_5V}, which is determined by the 6-bit delay block, to exceed 5.2 V. If this voltage level increases further as seen from the simulation results, it can reach breakdown levels, which can harm all the transistors. To prevent this from happening, the zener diode D_1 clamps the voltage around 5.6 V at the cost of excessive power loss. This power loss is one of the most critical losses in the overall system.

The 6-bit delay block used in the low dropout regulator design is the 2-bit reduced form of the 8-bit delay block previously detailed in Section 3.1 since the delay requirement here is similar. Also, the comparator is a modified version of the one used in zero-cross detection circuitry. The inputs, though, are at different DC voltage levels, which are around 1.05 V. These voltage levels in the inputs ease the design process and allow us to use less power from the 5 V supply coming from the regulated

voltage on the external capacitor C_2. Although it uses less power compared to the one in Figure 3.4, it operates faster and is smaller in area. It consumes only 9 nA of current from the 5 V coming from the LDO, which is 43 % lower than the comparator used in zero-cross detection circuitry.

Inputs to the comparator are from a fixed reference voltage and a sense circuit whose output changes as a function of the voltage on the output capacitor. Reference voltage generator, as shown on the right side of Figure 3.16, is adopted from [43]. Its output value, set to 1.05 V in post-layout simulations, can be calculated using the following equation:

$$V_{REF} \approx 5nV_{GS,n} = 5nV_T \ln(XY) \tag{3.1}$$

where n is equal to $1 + C_{dm}/C_{ox}$, and C_{dm} is depletion-layer capacitance per unit area, C_{ox} is the gate-oxide capacitance per unit area, V_T is the thermal voltage, X and Y are W/L ratios of the M_8 and M_2 transistors, shown in Figure 3.16, respectively. On the other hand, there is another factor that should be taken into consideration. The threshold differences on the transistors $M_3 - M_7$ adds additional voltage value to the output of the reference voltage generator. This is due to the layout restriction on the design-kit. The bulks of the transistors are connected to the ground, which leads to a non-zero bulk-source difference. Hence, although $M_3 - M_7$ transistors are equivalent in terms of size, their threshold voltages are different. Therefore, the above equation should be updated as follows:

$$\begin{aligned} V_{REF} \approx 5nV_T \ln(XY) + (V_{th,M_3} - V_{th,M_7}) + (V_{th,M_4} - V_{th,M_7}) \\ + (V_{th,M_5} - V_{th,M_7}) + (V_{th,M_6} - V_{th,M_7}) \end{aligned} \tag{3.2}$$

where $V_{th,M_3} - V_{th,M_7}$ values are threshold voltages of the $M_3 - M_7$ transistors. The post-layout simulation shown in Figure 3.18 proves that the obtainable voltage reference value is around 1.05 V, and it is vitally important to have this value since the lower bound is adjusted according to this value. The current consumption of the voltage

reference circuit is around 380 pA, which is an indication of why this architecture is chosen in the first place. Its area is also very small since it only consists of eight transistors, where it can be seen from Figure 3.17.

Another significant block in the low dropout regulation circuit is the voltage sense circuit, which consists of 18 diode-connected PMOS transistors. These series PMOS transistors act as a voltage divider, as shown in Figure 3.16. The output node of the voltage sense circuit is set to 1.05 V. It ensures together with voltage reference circuit that the voltage on the output capacitance of the regulator does not fall below 4.8 V. Upper limit of the regulator output voltage is controlled with the 6-bit delay-block as mentioned above and is set to 5.2 V. This circuit also consumes very low power since it consists of the only diode-connected transistors which act as a series of resistors. Its layout is given in Figure 3.19, which has almost the same dimensions as the voltage reference circuit. The current consumption of the voltage sense is also comparable to the voltage reference circuit, and is around 120 pA. It should also be noted that all the parasitics are taken into account, and sensitivity is adjusted so that it is fast enough to allow proper voltage regulation.

Moreover, the low dropout circuitry's overall power consumption is the biggest among the parallel-SSHI interface circuits with a current consumption of 65 nA from the external voltage, V_{RECT}. This vast power consumption stems from the losses due to the high voltage switch, clamping zener diode, and level shifters on the capacitors. The most significant contribution to the power loss is from the zener clamping, and it can not be eliminated since it is due to the TENG characteristic, where it pushes current to the output around the bias-flipping activity. The overall layout of the low dropout circuitry is given in Figure 3.20. The high voltage switch transistor and diode-connected charging transistor are separated by a certain distance, which is restricted by the design rule check due to the latch-up precautions.

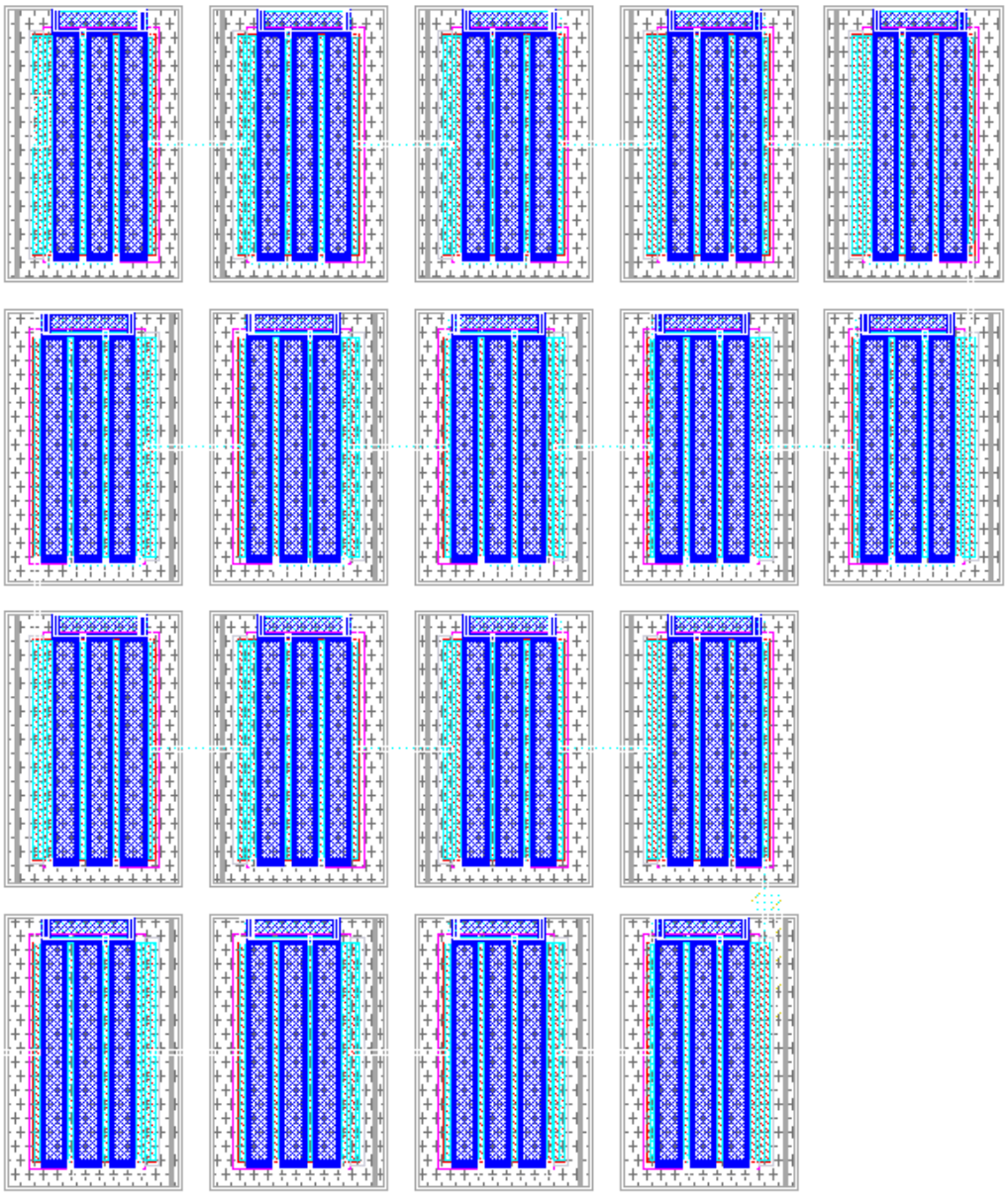

Figure 3.19. Layout of the voltage sense circuit.

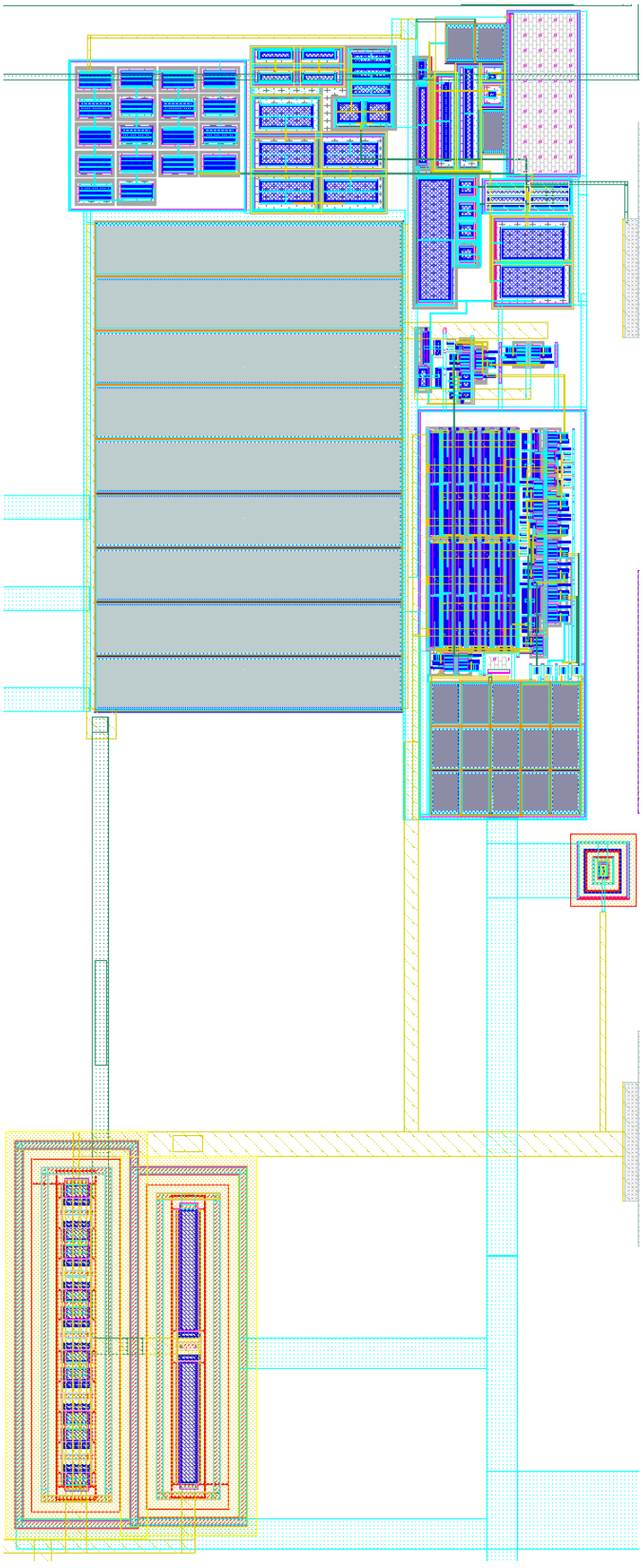

Figure 3.20. Layout of the low dropout (LDO) circuit.

3.3. 70 V Sense and Buck Start Signal Generation

As previously mentioned, the in-house fabricated TENG does not continuously deliver power to the buck DC-DC converter. The energy is stored first, and when it reaches a specific level, it is transferred to the buck DC-DC converter whose output is connected to a switched-capacitor DC-DC converter for further down-conversion. The energy is stored on an external high voltage capable thin-film capacitor that is charged up to 70 V, which is the breakdown voltage of the high voltage transistors in 0.18 μm HV BCD process.

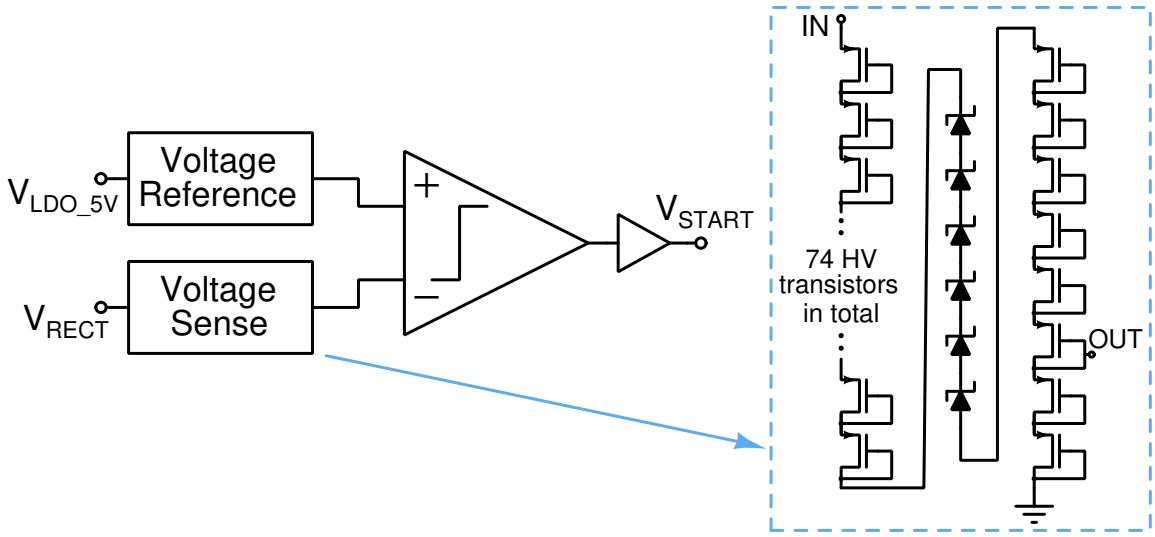

Figure 3.21. 70 V sense and start signal generation circuit.

In Figure 3.21, the 70 V sense and the start signal generation circuit are shown. The voltage sense part of the circuit is an optimized voltage divider similar to the circuit shown in Figure 3.16. When its output value is above the reference, the comparator output is set high, which is the required start signal for the DC-DC conversion. This start signal is the triggering mechanism for the buck converter to start the 70-to-10 V down-conversion process.

The 70 V sense circuit consists of 6 on-chip zener diodes and 74 high voltage diode-connected PMOS transistors connected in series. To achieve a low power consumption, more than one hundred of these diode-connected transistors would be needed, resulting in a very large area and uncertainty in the output voltage if zener diodes were not used. Six zener diodes are introduced in between the diode-connected high voltage PMOS transistors since zener well-layer breakdown voltage is around 35 V, which saves tens of PMOS transistors to be used in the design. Thus, the input, which is the voltage on the external storage capacitor, could be sensed with reasonable accuracy, low power, and relatively less area.

By considering the area, the voltage sense circuitry is the largest circuit block in the parallel-SSHI interface circuitry. This is due to the extra well layers for the isolation of the high voltage PMOS transistors. The large size of the overall layout can be seen in Figure 3.22, where the total area of the comparator and voltage reference generator is only around one-tenth of the voltage sense circuit area.

The comparator and the voltage reference circuits are the same circuits used in zero-current detector circuitry. These two circuits are also powered by the V_{LDO_5V}, which is generated by the low dropout regulator circuitry. The power consumptions of these two blocks are very small compared to the power consumed by the voltage sense circuitry. The total power consumption of these two blocks is 10 nA from the V_{LDO_5V}, whereas the power consumption of the voltage sense circuitry is 6 nA from the V_{RECT} value, which averages around 36 V. Therefore, its power consumption is four times more than the total power consumption of the comparator and the voltage reference circuits.

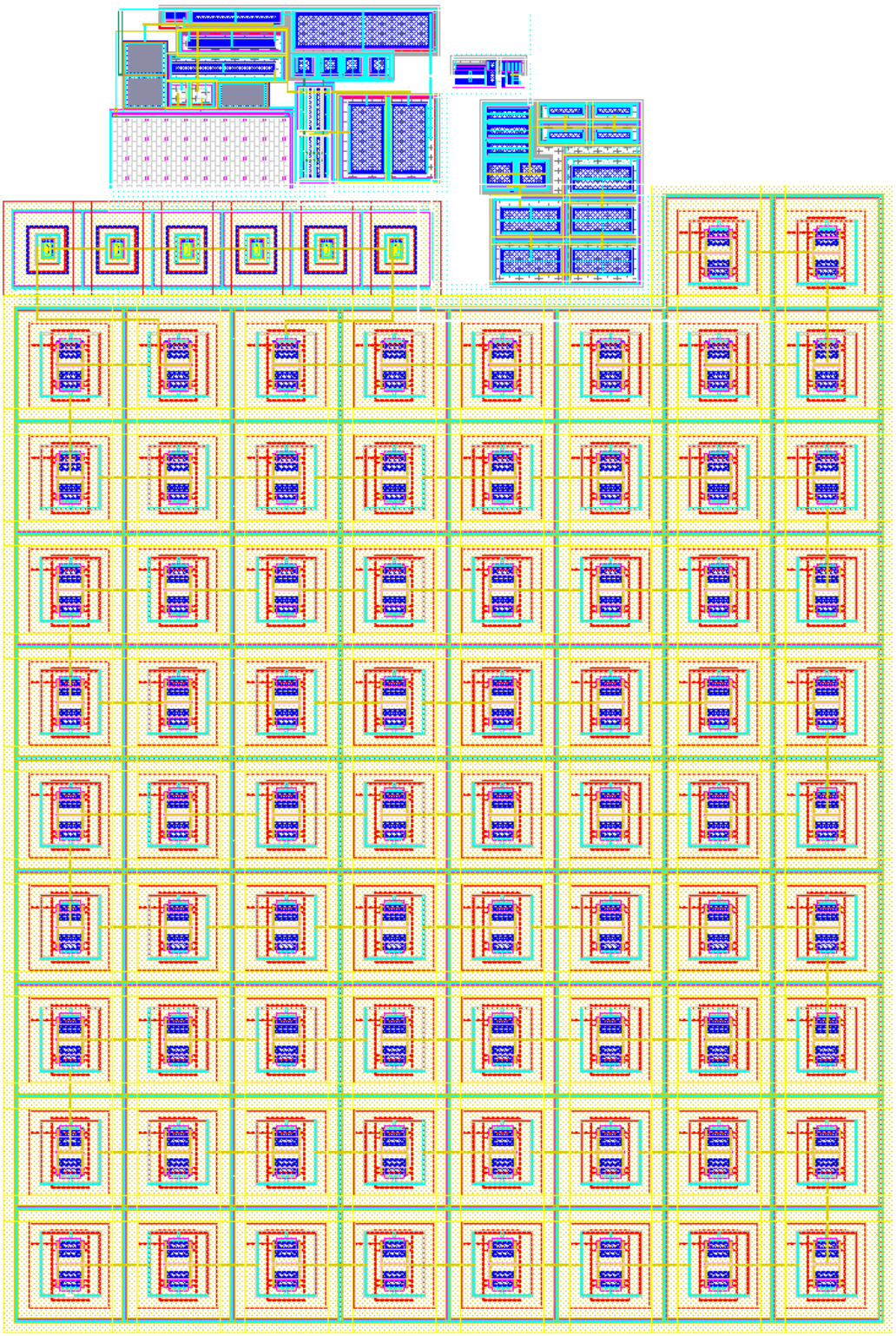

Figure 3.22. Layout of the 70 V sense and start signal generation circuits.

3.4. Area and Performance Evaluation

For the justification of the functionality, each block is simulated with the parasitics from the layouts. The post-layout simulations are iterated until achieving the schematic results by optimizing the schematics and layouts. The simulation results were as expected and detailed in Table 3.1 in terms of power and area. The simulation results cover the TENG operation for various frequencies. In Figure 3.23, 1 Hz, 2 Hz, and 5 Hz simulation results are shown. Their characteristics are almost the same except in 5 Hz simulation; the circuits consume less power due to shorter time intervals, which results in reaching buck start level in the third clock instead of forth. The layout of the whole bias-flip interface, including the pads, is shown in Figure 3.24.

Table 3.1. Power and area information when TENG is operated at 1 Hz.

Block	**Power**	**Area**
Zero Current Detector	22nA x 4.88V	190um x 215um
Comparator	16nA x 4.88V	65um x 115um
Delaybox and Digital blocks	6nA x 4.88V	125um x 200um
Low Dropout Regulator		195um x 500um
Comparator	9nA x 4.88V	55um x 100um
Voltage Reference	380pA x 4.88V	48um x 55um
Voltage Sense	120pA x 4.88V	59um x 50um
Delaybox and Digital Blocks	4nA x 4.88V	55um x 150um
Switch, Level Shifting Capacitors and Zener	65nA x 36V	150um x 230um
70V Sense and Start Signal Generation		265um x 395um
Comparator	9nA x 4.88V	55um x 100um
Voltage Reference	380pA x 4.88V	48um x 55um
70V Voltage Sense	6nA x 36V	265um x 345um
Rectifier Diodes		280um x 400um
Switch Transistors		475um x 375um
Overall		850um x 1850um

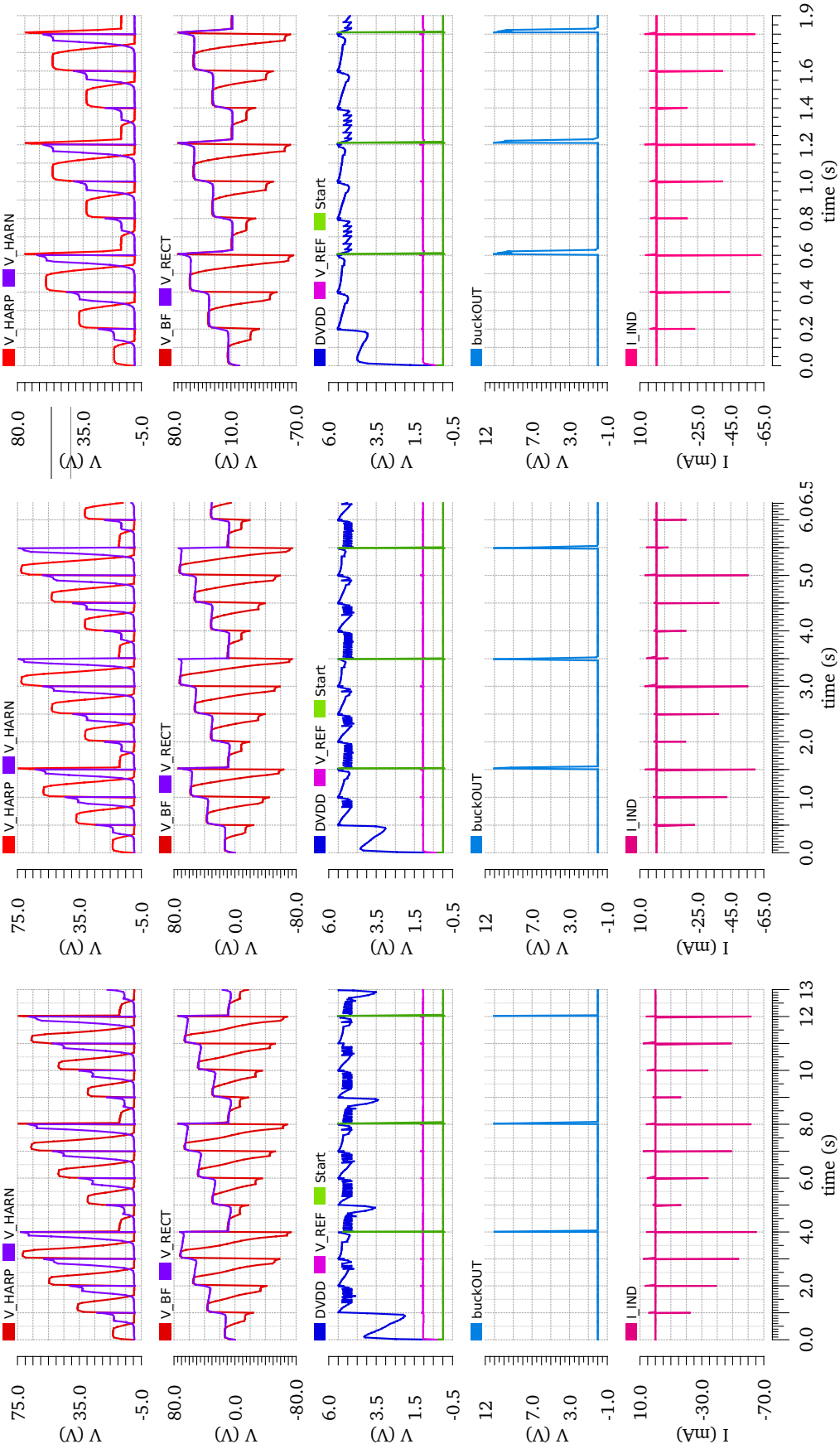

Figure 3.23. Simulation results for TENG operated at 1Hz, 2Hz,and 5Hz, respectively.

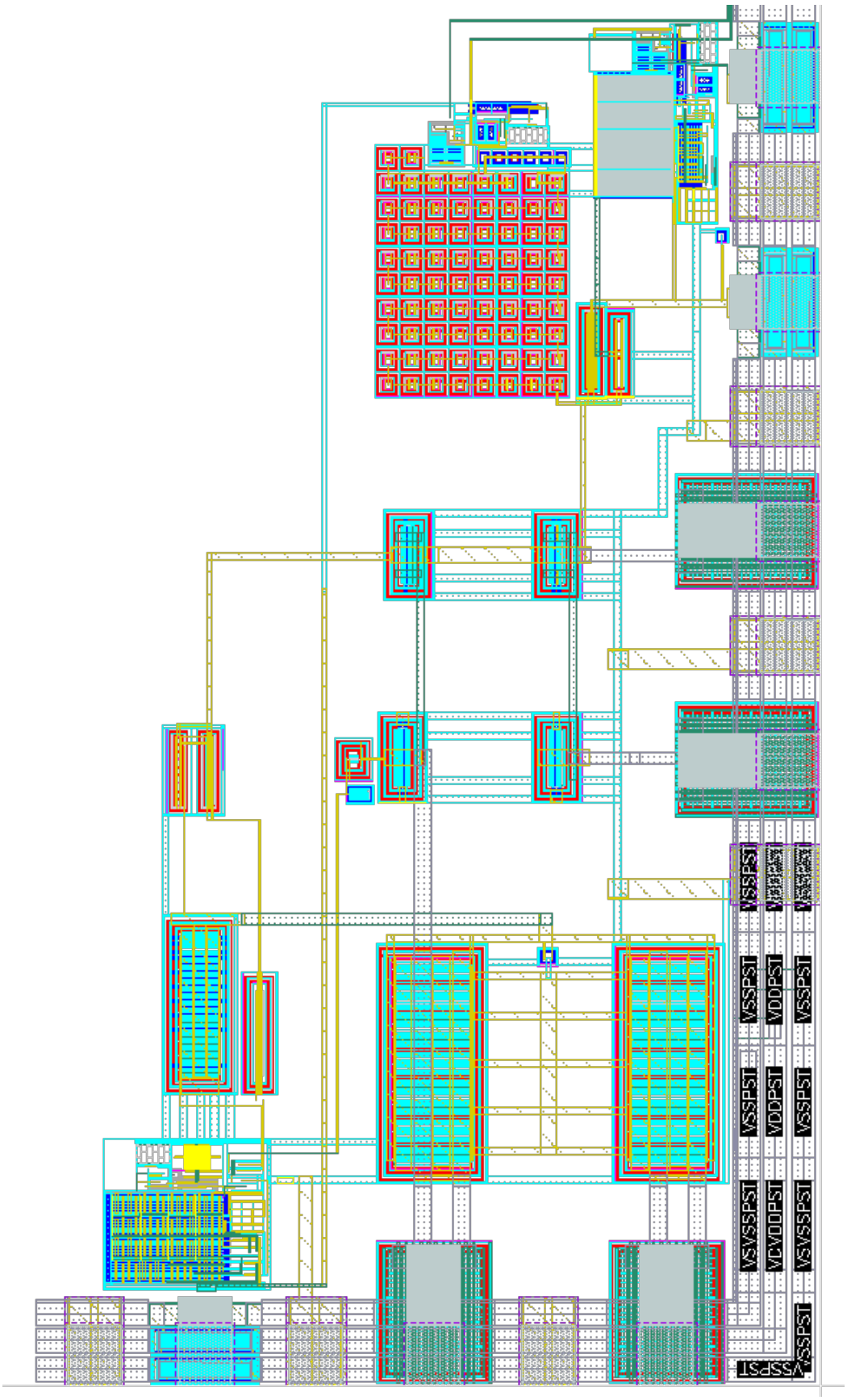

Figure 3.24. Layout of the whole parallel-SSHI interface including pads.

4. 70-TO-10 V BUCK DC-DC CONVERTER

4.1. Introduction

Once the harvested energy causes the voltage on the external capacitor C_{TENG} to reach 70 V and the sense circuitry detects this voltage level, a pulse is generated for the buck converter to start the energy conversion as explained in the previous chapter. Since the buck converter is the intermediate step of the 70-to-2 V down-conversion, it generates a 10 V from the 70 V and delivers it to the switched-capacitor DC-DC converter. This block is designed and realized by a Master's student as a Master's thesis [44].

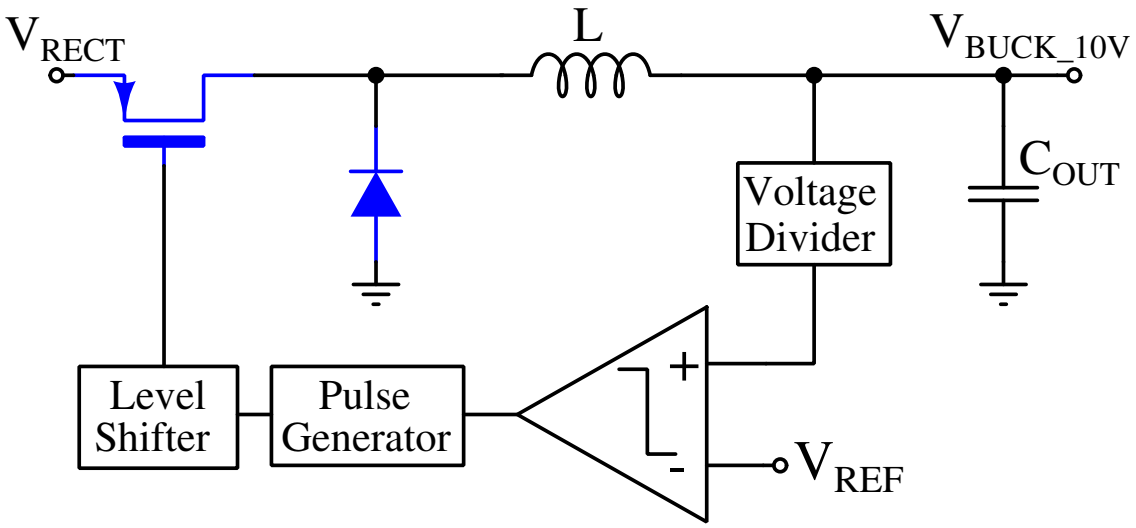

Figure 4.1. Proposed buck converter architecture.

Figure 4.1 shows the proposed buck converter. Since the input of the buck converter is connected to 70 V, a high-voltage PMOS transistor is used as the control switch, also known as high side switch (HSS). In buck converter architectures, a free-wheeling diode or an NMOS is used as the low side switch (LSS). Using an NMOS as the LSS requires the usage of a zero current detector and some other circuitry, which

adds to both complexity and power consumption. Thus, a high-voltage freewheeling diode, which makes this type of buck converters asynchronous, is used in this implementation. The HSS is controlled with a pulse frequency modulated (PFM) signal to achieve low power consumption. The PFM generation circuitry in Figure 4.1 consists of a comparator, a pulse generator, a level shifter, and a voltage sense block. The level shifter block, detailed in Figure 4.2, is used to control the high side switch and is designed to be compatible with high-voltage levels.

The buck converter's operation is as follows: The buck start signal, generated on the parallel-SSHI part of the system, triggers the level shifter to short the HSS switch. All the buck converter circuits are powered with the 5 V coming from the first stage of the switched-capacitor DC-DC converter since the low dropout regulator is designed for the intention of giving current in nano-ampere levels. Moreover, the switched-capacitor DC-DC converter is supplied from the buck converter. Initially, an ultra-low-power start-up circuit powered by the low dropout regulator lowers the gate voltage of the PMOS (HSS) and keeps the HSS shorted. Shorting the HSS leads to current flow through the inductor L that charges up the output capacitor C_{OUT}. HSS stays shorted until the output capacitor of the buck reaches 10V, and switched-capacitor DC-DC converter generates 5 V.

The output voltage is monitored by a sense circuit, which is a much faster version of the one in Figure 3.15, and its output is compared with a reference voltage generated by a band-gap reference circuit. When the sensed voltage from the output is smaller than the reference voltage, a fixed-duration pulse is generated by the pulse generator. If the sensed voltage is still smaller, another fixed-duration pulse is generated. This operation continues until the sensed voltage is larger than the reference voltage. Fixed-duration pulse is programmable via a 4-bit delay block, which can be programmed externally via the I2C interface. When the sensed voltage is larger than the reference, the HSS is opened. Once the HSS is off, a current flows from the ground over the high-voltage diode and passes through the inductor to the output capacitor C_{OUT} until the current in the inductor is dissipated. Consequently, energy transfer from C_{RECT} to C_{OUT} is completed for a cycle.

4.2. Buck Converter Sub-blocks

Level shifter block, as shown in Figure 4.2, plays a critical role in dealing with high voltage problems. The voltage levels that are required to turn on and off high side switch (HSS) are 5 V below of the input voltage, which is $V_{RECT} - 5V$, and the input voltage itself, V_{RECT}, respectively. As previously mentioned, the buck conversion process is initiated with a buck start signal generated when V_{RECT} reaches 70 V. This 70 V level is difficult to manage. First, 70 V V_{RECT} input can be bearable for the HSS. Then, this switch can be turned on and off when it is necessary. So, the aforementioned level shifter is designed, which is fast enough to respond to changes in its input.

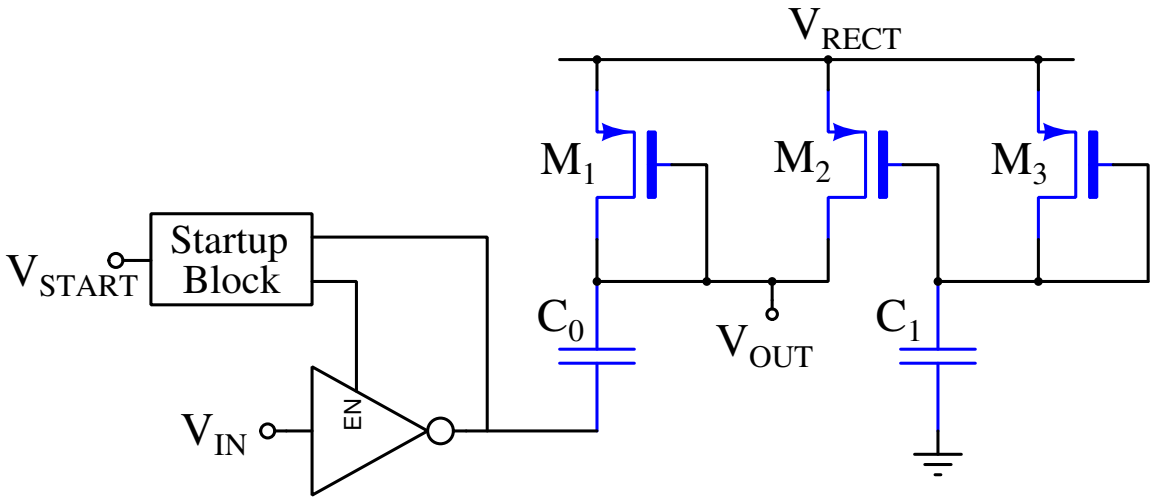

Figure 4.2. The proposed level shifter for buck converter.

V_{RECT} charges to 70 V in three seconds, which is very slow and makes it easily operable for the level shifter with small power consumption. The level shifter transistors M_1, M_2, and M_3 are high voltage transistors that are tolerable to 70 V drain-source voltages, and C_0, C_1 capacitors are metal-on-metal capacitors that are also tolerable to very high voltages. M_2 transistor is very large compared to the two other same-sized transistors, and the capacitors are also in similar size. When V_{RECT} charges, M_2 transistor rapidly charges the C_0 capacitor to V_{RECT}, which keeps HSS opened. Meanwhile, M_3 also charges the C_1 capacitor to V_{RECT}, which will prevent the output

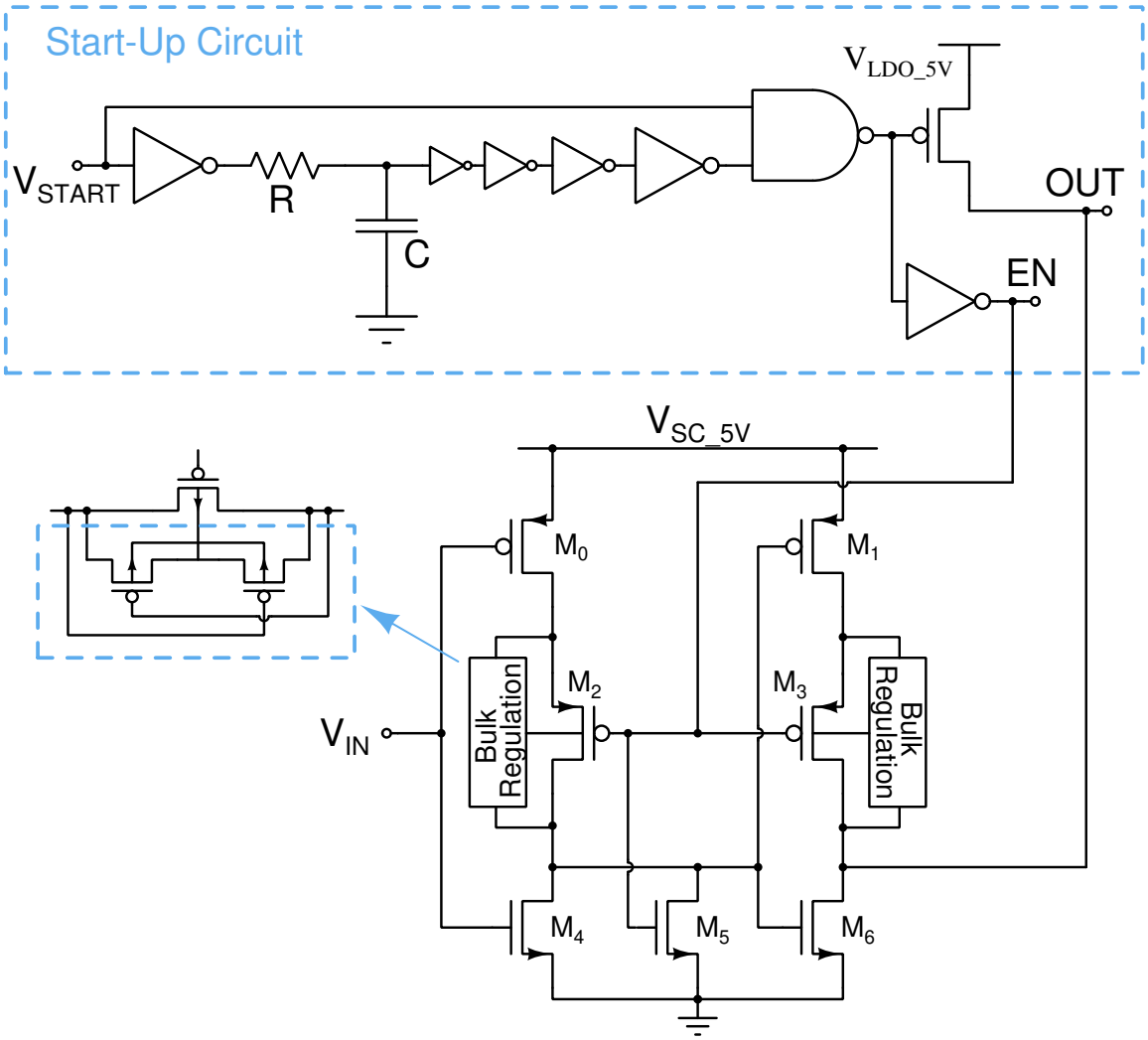

Figure 4.3. The start-up circuity, digital block, and bulk regulation circuit for the level shifter.

of the level shifter from changing while ensuring M_2 transistor is turned off during the down-conversion process. This is only possible if V_{RECT} does not increase where the opposite happens since the charges are delivered to C_{OUT} via HSS and inductor.

The level shifter block is triggered by the start signal coming from the start signal generation block, shown in Figure 3.21. This signal is processed in the start-up block of the level shifter, as shown in Figure 4.3. This circuit initially powered-up by the voltage coming from the low dropout regulator to start the down-conversion. The start signal is NANDed with its delayed form to generate a logic '0' pulse, which

lowers the output of the level shifter by a 5 V, hence the gate of the HSS is lowered by 5 V. Thus, the HSS is turned on, and a current flows through HSS and inductor to the output capacitor to charge it up to 10 V.

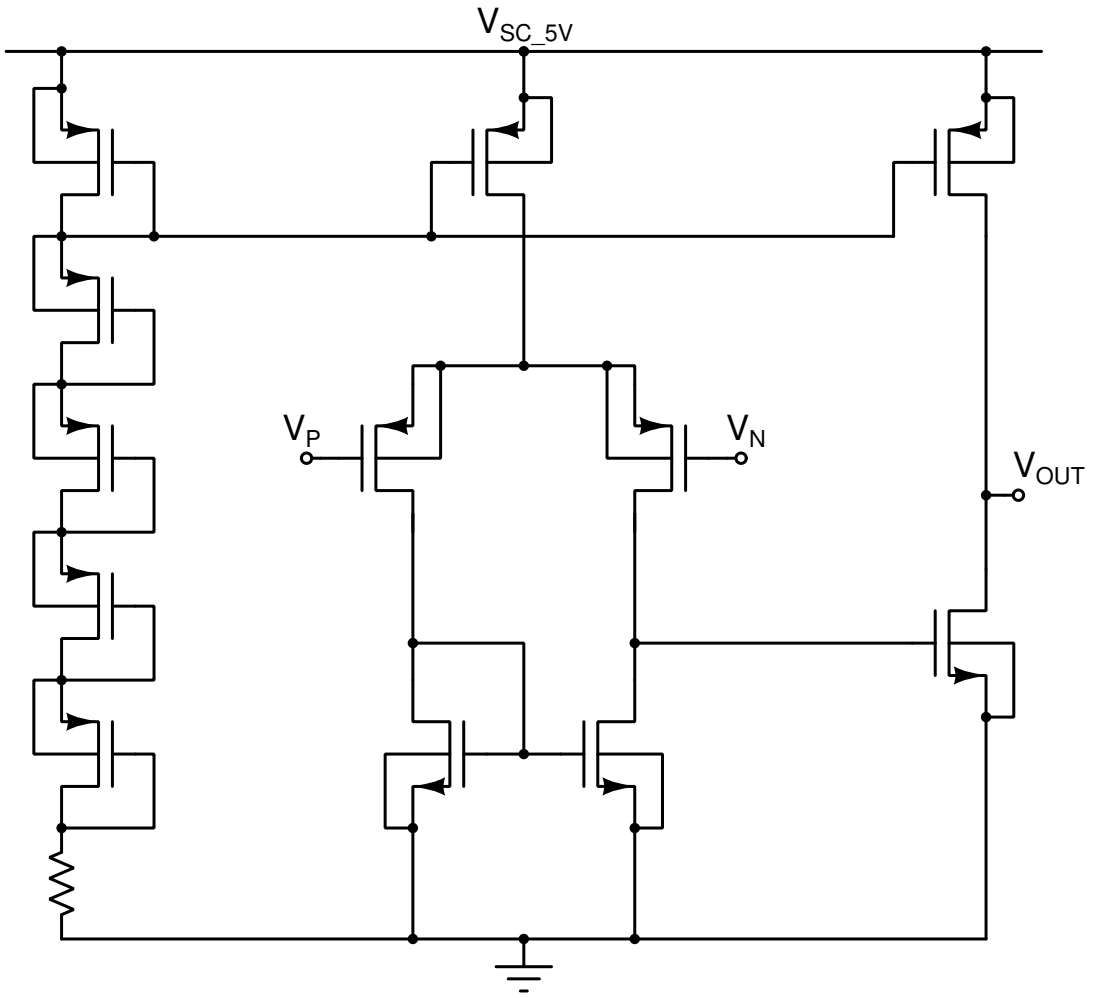

Figure 4.4. Proposed comparator circuit for the buck converter.

However, the RC delay element slowly changes its state, which causes a short path in the inverter connected to the C_0 capacitor of the level shifter. Thus, a modified tristate inverter is used in this block, as shown in Figure 4.3. This modified digital circuit separates the regular operation of the buck converter from the start-up operation by using the power from the 5 V coming from the switched-capacitor DC-DC converter. This separation process is needed since power coming from the LDO is not

enough. This circuit modifies the current path on a chain of inverters with the help of bulk regulation circuits, which utilizes body diodes to connect bulk to the highest potential when switching from start-up operation to regular operation.

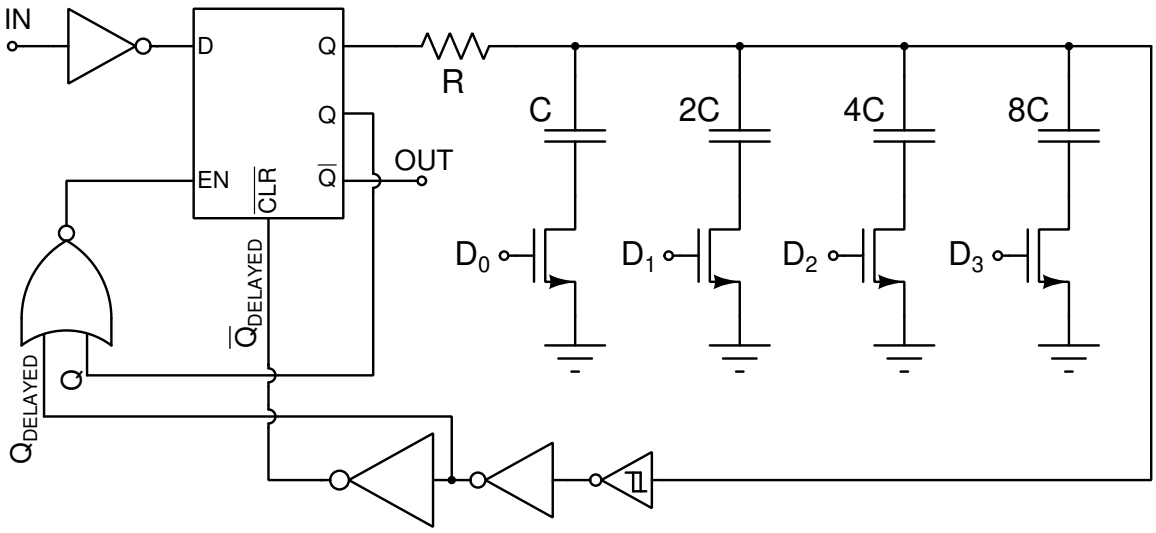

Figure 4.5. Pulse generation circuit for buck converter.

Another critical job is sensing the output voltage in a fast and accurate manner. Thus, the output voltage is monitored by a sense circuit, which is a much faster version of the one in Figure 3.15. On the other hand, there are some changes in this circuit. First, the aspect ratios of the PMOS transistors are very big compared to those in parallel-SSHI interface since the sense speed is critical. Then, in the parallel-SSHI interface, the 5 V level is sensed on the low dropout regulator compared to the 10 V level, which is sensed on the buck converter's output capacitor. Moreover, high voltage transistors are not suitable for this circuit since they cover a large area, which adds lots of parasitics and makes it difficult to operate at high speeds. However, there are low-threshold PMOS transistors in the technology design-kit, and they have high voltage n-wells compared to the normal-threshold PMOS transistors, which are the most common ones used in this thesis. These high voltage n-wells can bear 10 V substrate-bulk voltage difference, which is very likely to happen, and they have small parasitics compared to the other high voltage transistors.

The other two blocks from Figure 4.1 are comparator and pulse generator, which are shown in Figure 4.4 and Figure 4.5, respectively. The comparator is a very common architecture from the literature and fast enough to respond to the changes in its inputs. It is self-biased, hence a start-up circuit is not needed.

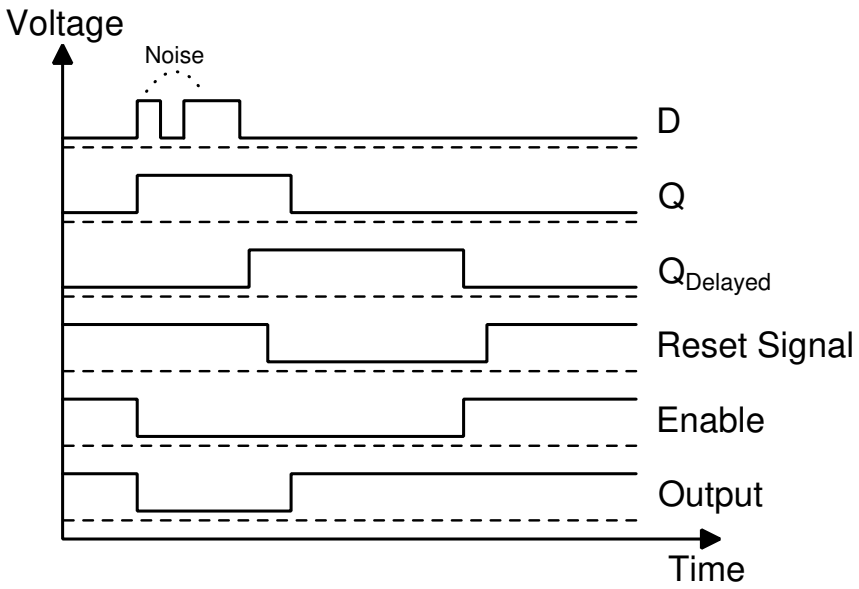

Figure 4.6. Generated signals in the pulse generator.

The pulse generator is used to control the time interval for HSS to be turned on. The output of the comparator is fed to the pulse generator's 'D' input. When the logic '1' changes to logic '0' in the 'D' input of the latch, the pulse generator resets the latch. The timing of the generated pulse is given in Figure 4.6. The pulse duration is set by a 4-bit control coming from the I2C interface circuit, which is externally controlled by the user.

The output of the RC delay line of the pulse generator is connected to a Schmitt trigger gate, which prevents false pulses from being transmitted to the latch. When $Q_{Delayed}$ is logic '1', Schmitt trigger holds it for a while after the reset, and then it becomes logic '0'. Schmitt trigger also holds $Q_{Delayed}$ at logic '1' for a while, following the arrival of the reset signal. This leads D-latch to be disabled longer than expected. If Schmitt trigger is not used, D-latch will turn to logic '1' just after the resetting.

This would cause the kickback or coupling in the comparator that would create false pulses, as shown in Figure 4.6.

4.3. Area and Performance Evaluation

The buck converter functionality is realized after several post-layout simulations since the parasitics affect the system operation significantly. Typically, the output of the buck converter is the switched-capacitor DC-DC converter. For calculation and ease of design, the switched-capacitor DC-DC capacitor is modeled as a load of 67 $k\Omega$ with a 150 μA current on it.

The simulation result is given in Figure 4.7. The buck start signal initiates the down-conversion and a large amount of current flows to the output until the inductor current stabilizes. Then, the switched-capacitor DC-DC converter supplies 5 V to the buck converter's internal blocks for the rest of the operation. The initially set pulse width leads to less voltage variation on the output since the input voltage, V_{RECT}, gradually decreases. The current on the inductor also decreases until the end of the operation with the very same reason as specified. As the operation continues, the switching frequency and power loss increase due to fewer output variations.

The inductor used in the simulations is the model of a commercially available 1 mH inductor with a DC resistance of 13 Ω, which causes a lot of losses on the inductor. This also causes more power dissipation on HSS since this resistance leads to more switching activity. The overall efficiency is calculated as 71.4%, and the rest of the energy is dissipated as the losses on the other blocks of the buck converter. The losses are distributed as follows: 12.5% on HSS, 12.6% on inductor, 2.2% on freewheeling diode, 0.5% on voltage sense, 0.4% on comparator, 0.3% on level shifter, 0.1% on pulse generator, and <0.1% on ESR. Additionally, the layout of the buck converter is given in Figure 4.8.

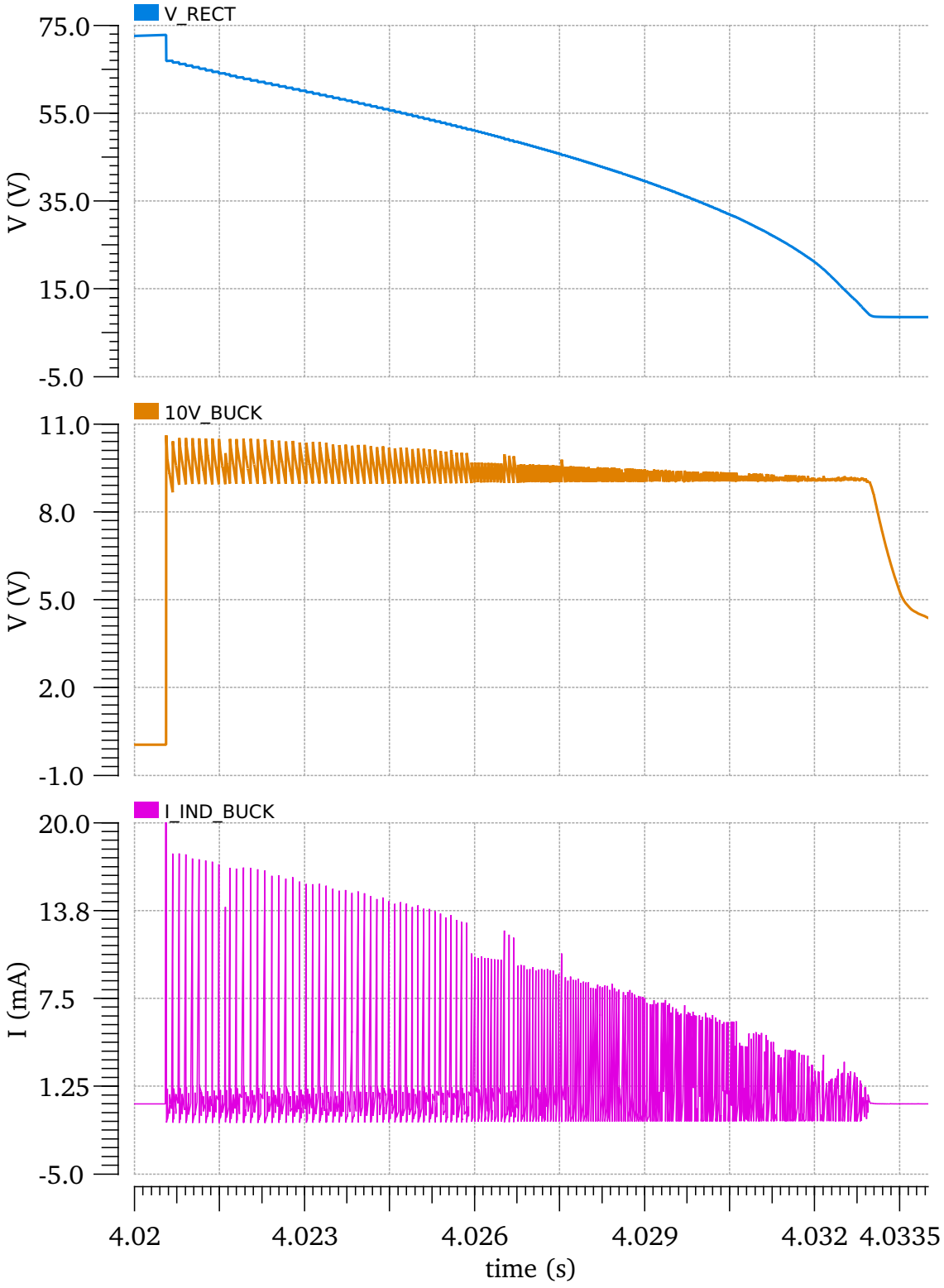

Figure 4.7. Simulation results for buck converter.

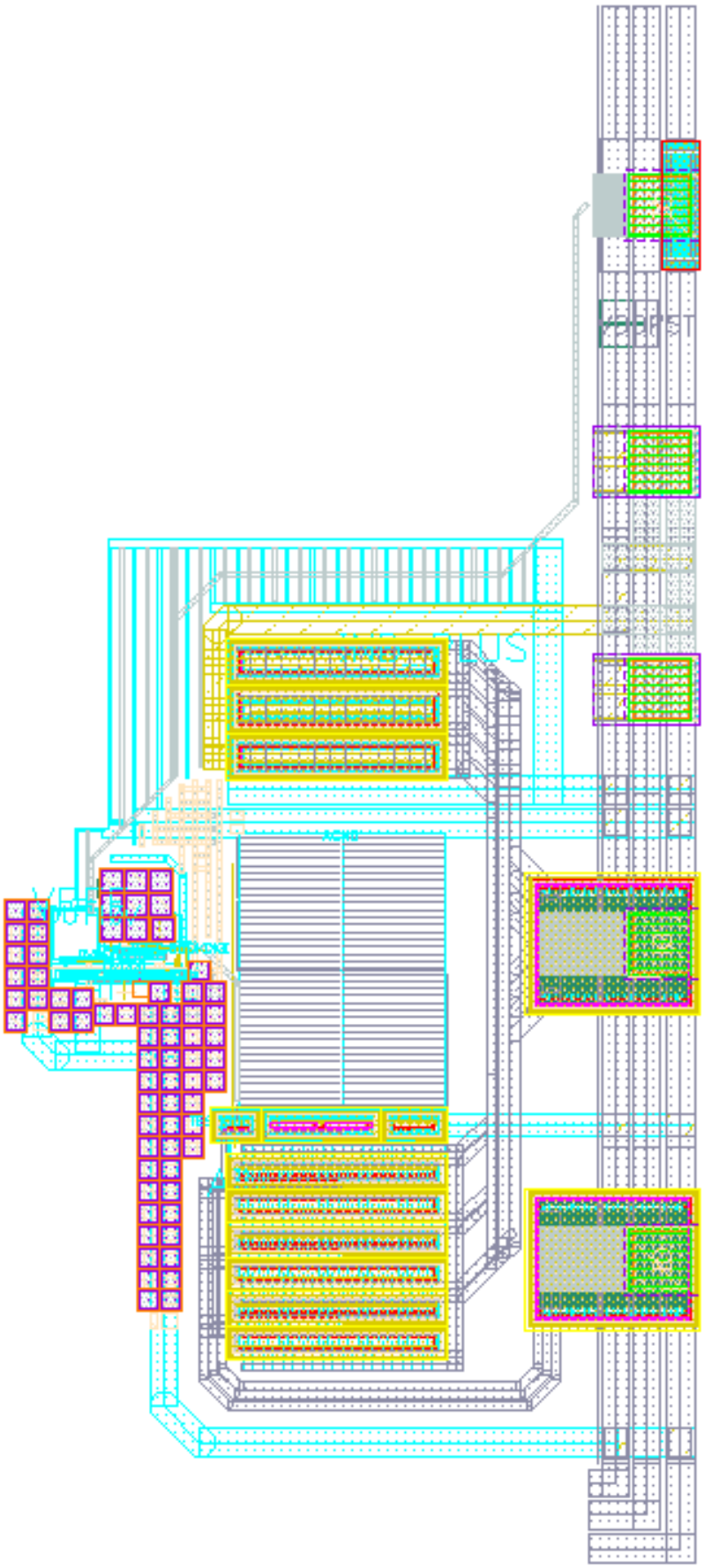

Figure 4.8. Layout of the buck converter.

5. 10-TO-2 V SWITCHED-CAPACITOR DC-DC CONVERTER

5.1. Introduction

Once the rectified voltage is down-converted to the 10 V level by the buck DC-DC converter, it is fed into the switched-capacitor DC-DC converter, shown in Figure 5.1, to obtain a voltage level that is suitable for modern integrated circuit nodes. Since the conversion ratio required is 10-to-2 V, it is challenging for the DC-DC converters to achieve high efficiency, especially for low load current levels (~500 μA in our case). Another issue to watch for in the design is that the supply is 10 V for the block while the devices that are used have a maximum rating of 5 V. To this end, two 2-to-1 cascaded stages are used to keep the voltage difference across all the capacitors and switches below 5 V, which is the CMOS technology limitation. The schematics of this block are initially designed by a PhD student, then significantly modified and optimized by the author of this thesis.

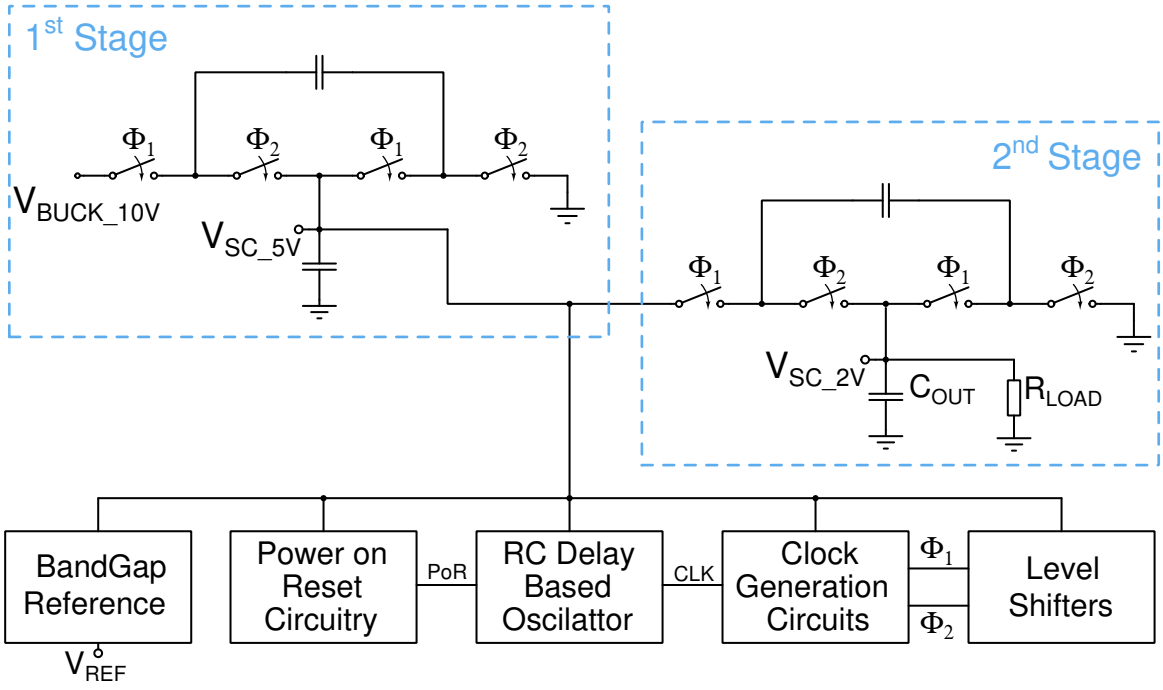

Figure 5.1. Proposed switched-capacitor DC-DC converter architecture.

The output voltage settles down to around 2 V rather than the ideal 2.5 V due to the losses in the converter. The internal circuits used for clock generation and other purposes are supplied from the first stage's output. During start-up, the outputs from the clocking circuitry are logic '0' since the output of the first stage is zero. By using PMOS switches for this converter, as shown in Figure 5.2, the output is passively charged from the 10 V supply until it reaches the normal operation. A power-on-reset circuit similar to the circuit designed in [45] is used to generate a pulse to start the internal RC based oscillator operation.

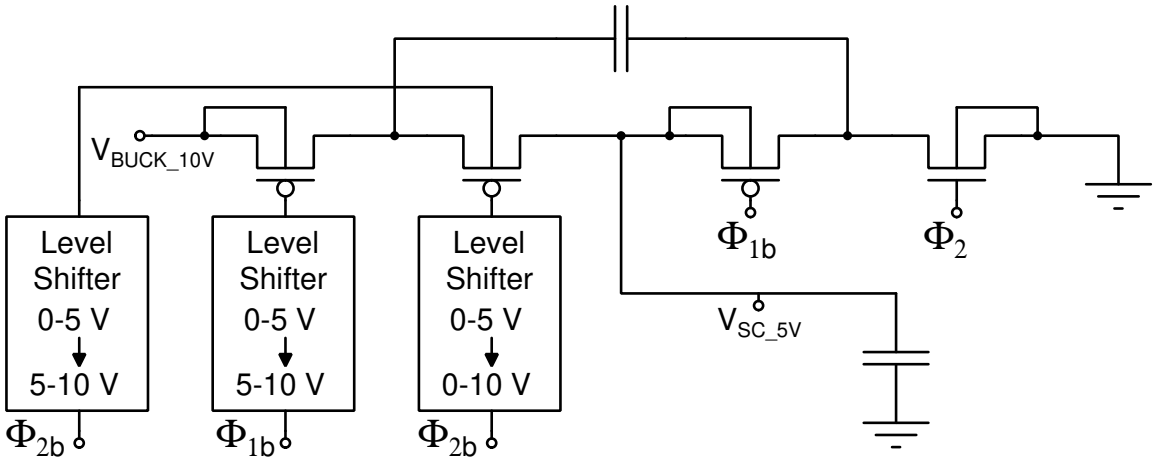

Figure 5.2. 1st stage of the switched-capacitor DC-DC converter.

The first stage of the switched capacitor DC-DC converter, as shown in Figure 5.2, performs a down-conversion from 10 V to 5 V. In order to keep switch transistors within the technology breakdown limits, two different level shifters, which are shown in Figure 5.6 and Figure 5.7, are used. The first one converts 0-5 V range to 5-10 V range and is used to bias one of the PMOS switch's base and control one PMOS switch's gate, as shown in Figure 5.2. The second type converts 0-5 V range to 0-10 V range and is used to control other PMOS switch's gate.

An RC based oscillator architecture similar to [46] is used to achieve lower variation in terms of output frequency across different process-voltage-temperature (PVT) conditions. The different resistors in the RC sections used to determine the output

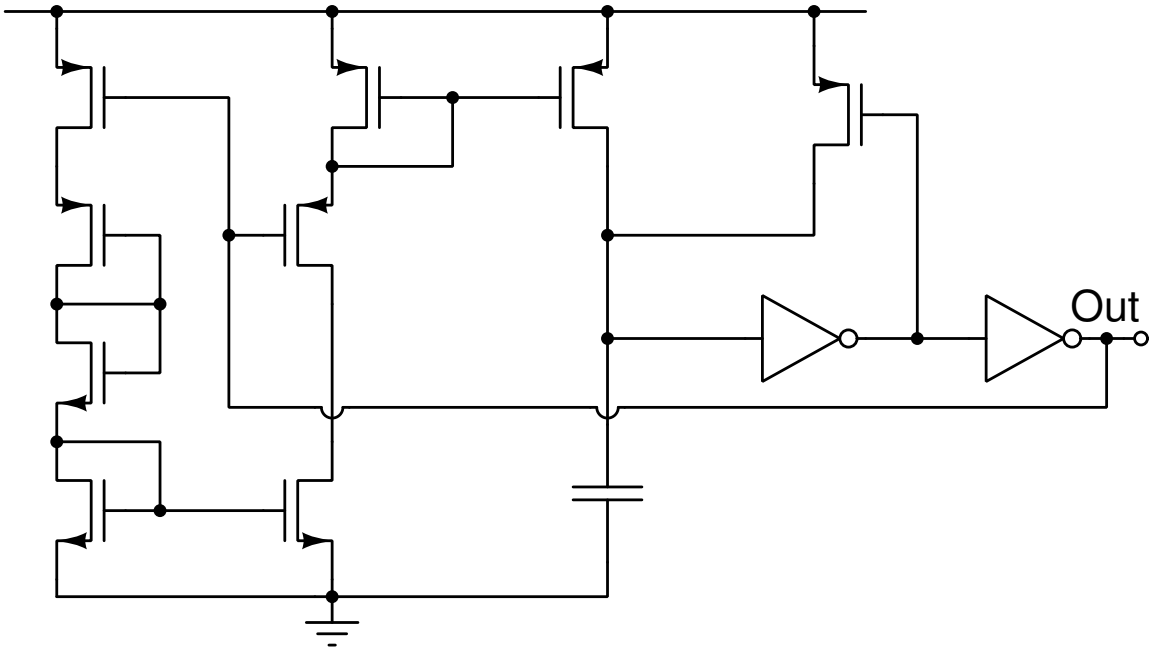

Figure 5.3. Power-on-Reset circuitry used in switched-capacitor DC-DC converter.

frequency are controlled through an internal control circuit to have a sort of negative feedback on the DC-DC converter output voltage to maintain this voltage within a certain range across different PVT conditions. The output voltage is compared with two voltage references, which are generated in band-gap reference [47], and the outputs of these comparators control an up/down counter. The up/down counter output bits are used to control the RC oscillator resistors.

5.2. Switched-Capacitor DC-DC Converter Sub-blocks

In this section, more detailed operation schemes of the sub-blocks are covered. As previously mentioned, the buck converter sends its output to a capacitor, which is the input of the switched-capacitor DC-DC converter. The conversion process does not start with the availability of the voltage at the input. It starts after the kickoff of a chain of circuit operations. However, these operations require power, which is passively provided by the first stage of the switched-capacitor DC-DC converter. The switches in the first stage are chosen as PMOS type transistors, and their gates are

connected to logic '0' since the level shifters are not powered yet, and their outputs are equal to 0 V. As the voltage starts to increase on the output capacitor, the first block that is triggered is the power-on-reset circuit.

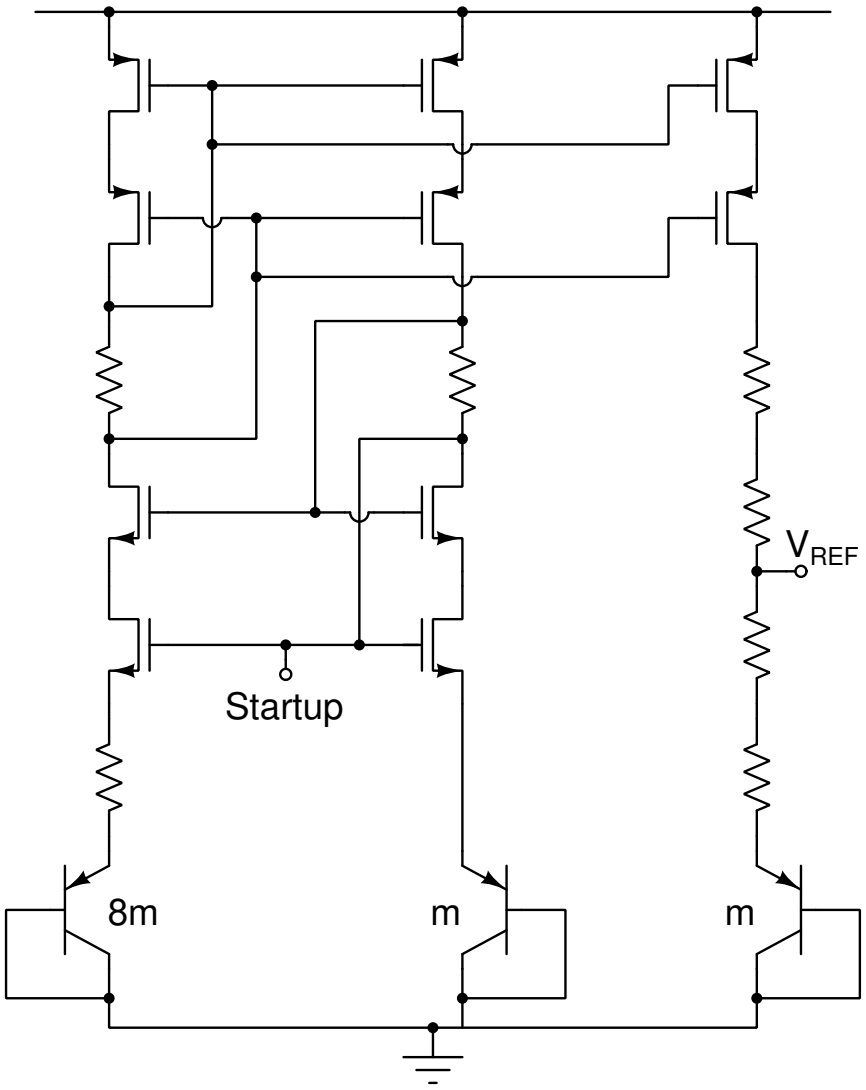

Figure 5.4. Bandgap reference circuit used in buck converter and oscillator clock frequency adjustment.

The power-on-reset circuits are very common among the architectures that use cold start-up to initialize their systems. These circuits are very simple and consume very low amounts of currents, usually in pA levels. Also, these circuits usually can not be altered after production, which puts a strain on the triggering point of the circuit.

The power-on-reset circuitry used in this architecture starts right after the voltage on the input capacitor reaches a certain level. The schematic of the power-on-reset circuit is illustrated in Figure 5.3. This circuit generates a logic '1', which resets the process-variation-temperature configuration of the RC delay-based oscillator when the first stage provides a stable 5 V to the system.

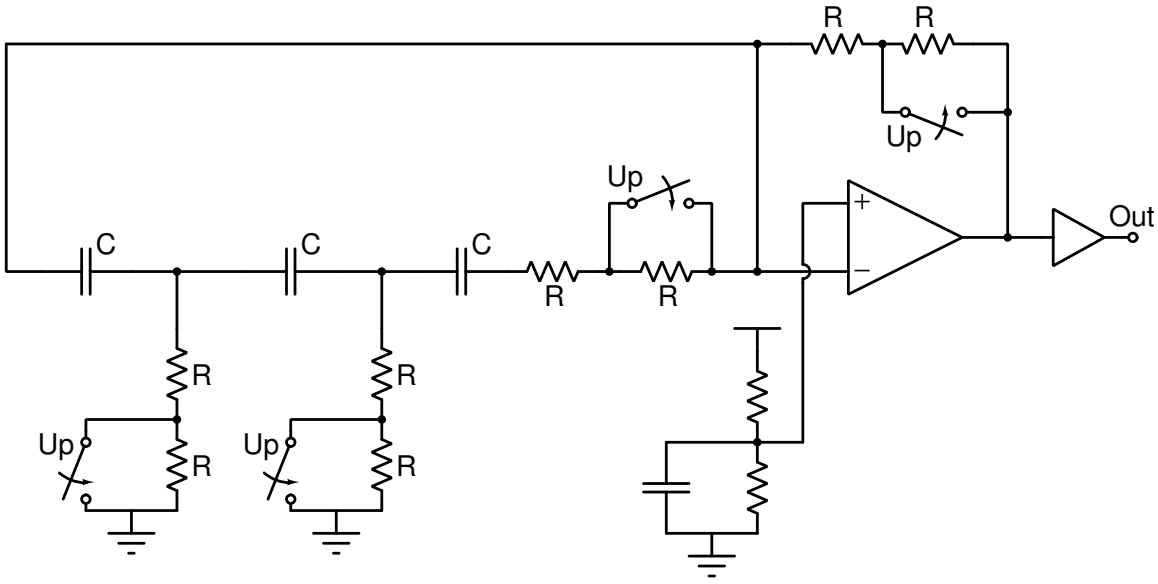

Figure 5.5. RC delay based oscillator used to create clock signals.

The overall system architecture of this thesis requires many reference voltages to be used for various needs. The parallel-SSHI needs two reference voltages, which are used for 5 V generation on low dropout regulator and 70 V sense circuit. However, they use their own low power, small area reference circuits since the operation interval of parallel SSHI is much broader than those of the buck converter and the switch-capacitor DC-DC circuits. The buck converter needs a very persistent reference circuit to compare the sensed voltage from its output. And finally, some sub-blocks of the switched-capacitor DC-DC converter requires different references for diverse purposes such as bias voltage generation, and reference for decreasing process-voltage-temperature variations of the oscillator. Thus, a band-gap reference circuit is designed for both the buck converter and the switched-capacitor DC-DC converter requirements.

The designed band-gap reference is depicted in Figure 5.4. This circuit is an improved version of the conventional band-gap reference circuits in the literature [47]. It provides two bias voltages, a reference that is used for the buck converter requirement, and a reference for the oscillator PVT variation reducing process.

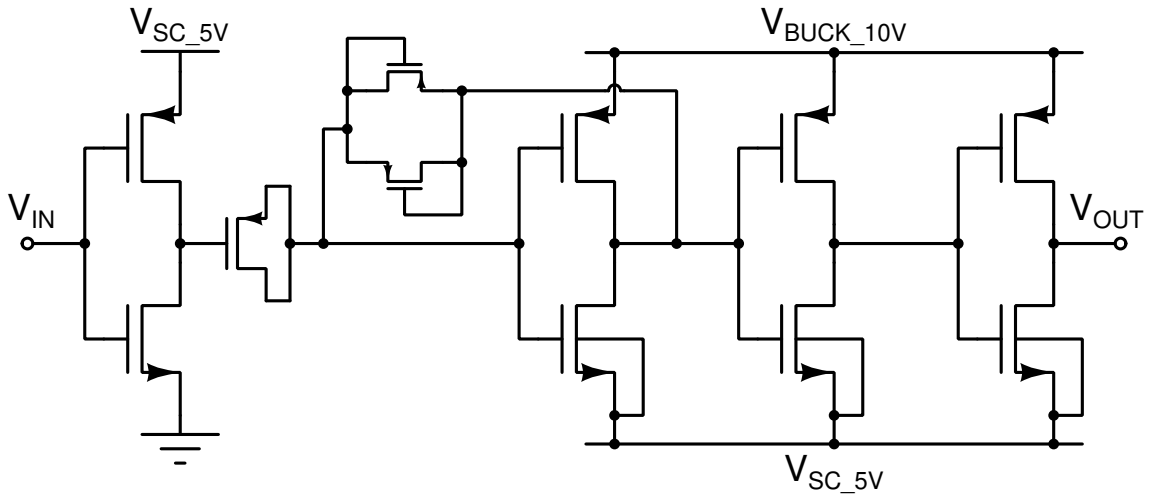

Figure 5.6. 1st level shifter that shifts 0-5 V level to 5-10 V level.

One of the main requirements of the switched-capacitor DC-DC buck converters is a clock generation circuit for all the switching activities. For an internal clocking circuitry, an oscillator that generates accurate and stable waveform is needed. In literature, there are many types of oscillators. One of the most commonly used oscillators is a quartz crystal oscillator, an off-chip component that can not be used in this study. Among other oscillator architectures, RC based oscillators are also very extensively used since they are very easy to implement. However, they are very prone to variations such as process, voltage, and temperature. Thus, several methods are applied to the RC delay-based oscillators to make them more stable and robust against the above variations. One of them is controlling the frequency with an implemented negative feedback scheme. As shown in the schematic of the proposed oscillator, which is illustrated in Figure 5.5, redundant resistors are switched with a control signal to change the RC time constant and reduce the variation on the frequency. The switched-capacitor's output is compared with the references generated by the band-gap reference

circuit, and the outputs are fed to an up/down counter to control the RC oscillator resistors. Thus, the oscillator provides a stable frequency waveform for the switching activity. The output of the oscillator is a sine wave, as shown in the simulation results, which is given in Figure 5.8. This sine wave is converted into a square wave with the help of a series of buffers. Then, this square waveform is used to generate non-overlapping signals by a well-known NAND-flipflop based inverter chain [48]. The square waveform and non-overlapping clock signals are also shown in Figure 5.8.

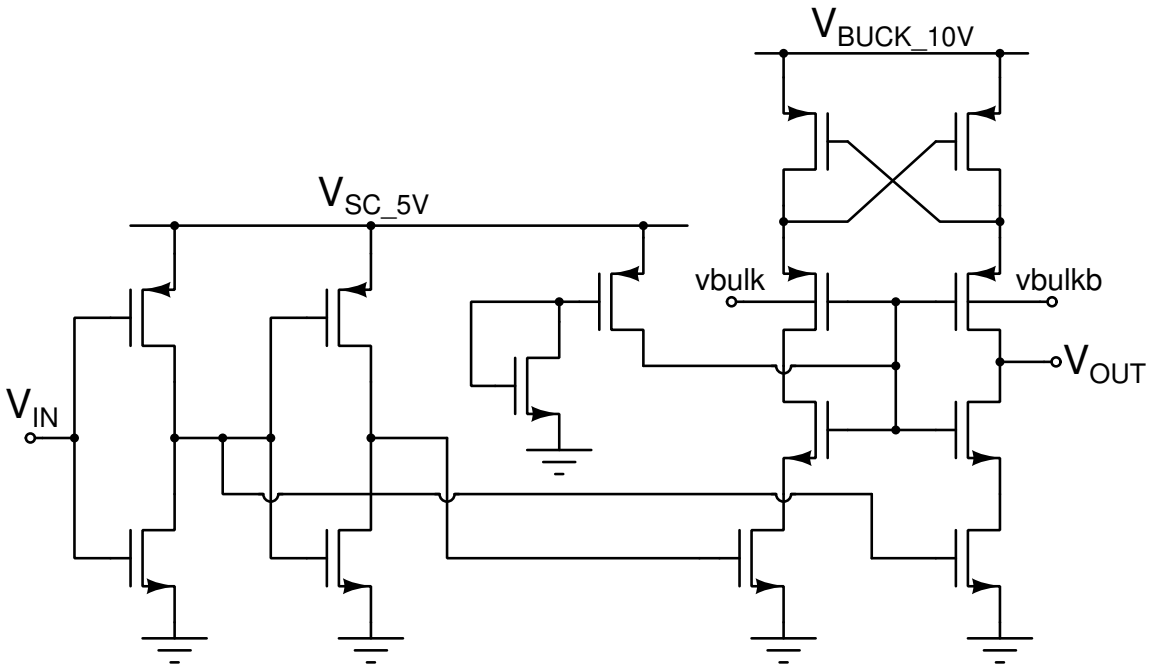

Figure 5.7. 2nd level shifter that shifts 0-5 V level to 0-10 V level.

The generated non-overlapping signals are used for the switching activities of the switched-capacitor DC-DC converter. On the other hand, these generated non-overlapping signals are not directly applied to the switches of the first stage of the switched-capacitor DC-DC converter. The first stage of the switched-capacitor DC-DC converter, as shown in Figure 5.2, down-converts the input coming from the buck converter to 5 V, which is used to power up all the internal circuits of the buck converter and the switched-capacitor DC-DC converter. Since the input is 10 V and the technology breakdown limit is 5 V, particular measures are taken to keep voltage

levels within the technology limits. For this purpose, two different level shifters are needed as shown in Figure 5.6 and Figure 5.7.

As previously mentioned, the outputs of the level shifters are logic '0' since the output of the first stage is zero. Using PMOS switches in the first stage and letting the output capacitor passively charging through the switches supply initial power to all the circuits described earlier. However, the technology limit puts stress during the passive charging operation since the drain-source voltage over the first two switches is 10 V. Therefore, the gate-source voltage is under stress and should be returned to the nominal values as soon as the operation of the down-conversion starts. One of the critical components here is the capacitance value used in the first level shifter, which is sized very carefully to decrease the initialization interval. Then, the switches in the first stage are controlled between 5-10 V levels with the signals coming from the first level shifter.

Moreover, the second switch in the first stage faces a more extreme case. During the switching activity, source and drain terminals of the second switch either bear 5 V or 10 V and the switch should be 'ON' when the drain is 5 V which requires the gate to be 0 V and should be 'OFF' when the source is 10 V which requires the gate to be 10 V. Therefore, a second level shifter is used to convert 0-5 V levels to 0-10 V levels. Also, the base of the second switch should be leveled up or down according to the signal on the gate, which will be ensured by using another first type of level shifter. These level shifting operations are simulated and shown in Figure 5.8.

5.3. Area and Performance Evaluation

The switched-capacitor DC-DC converter functionality is realized after several post-layout simulations since the parasitics significantly affect the system operation. The overall system load is modeled as 5 $k\Omega$ with a 500 μA current on it.

The simulation result is given in Figure 5.9. The frequency of the switching activity is consistent with the initial design goals. The simulation result provided in

Figure 5.9 shows the voltages that have connections to the outside of the chip. The output of the first stage is expected to be around 5 V and which is met according to the post-layout simulation results. The ripple on 5 V output is 76 mV. The system output, which will drive the 5 $k\Omega$ load, is expected to be around 2 V due to the losses in the first stage. The simulation result shows that it is around 2.3 V with an 18 mV ripple on it.

Moreover, the reference voltage generated by the band-gap reference circuit is simulated as 1.06 V with a ripple of 19 mV, which is very big for a reference circuit. However, this ripple does not affect the efficiencies of the buck converter and the switched-capacitor DC-DC converter. Shielding the reference voltage's connection to the pad did not work in this design architecture since the path to the pad is very long, and the amount of the capacitance over the path is very large. As an overall performance evaluation, the overall efficiency of the switched-capacitor DC-DC converter is calculated as 69.8%, which is consistent with the initial design targets.

Finally, the layout of the switched-capacitor DC-DC converter is given in Figure 5.10. The layout of the switched-capacitor DC-DC converter covers more than half of the overall chip area. This is due to the amount of flying capacitors used to transfer charge from input to the output. Our initial designs were utilizing PMOS gate-bulk capacitance, so that metal layers would be free to use. Nonetheless, parasitic diode formed between bulk and substrate layers caused a significant loss on the efficiency due to the large leakage current to the substrate, which was due to the large amount of the capacitance used. Therefore, metal-insulator-metal (MiM) capacitors are used in the top layers, which also caused the switching noise on the reference voltage. To eliminate the switching noise, the underneath of the MiM capacitors are left empty, which resulted in larger area usage.

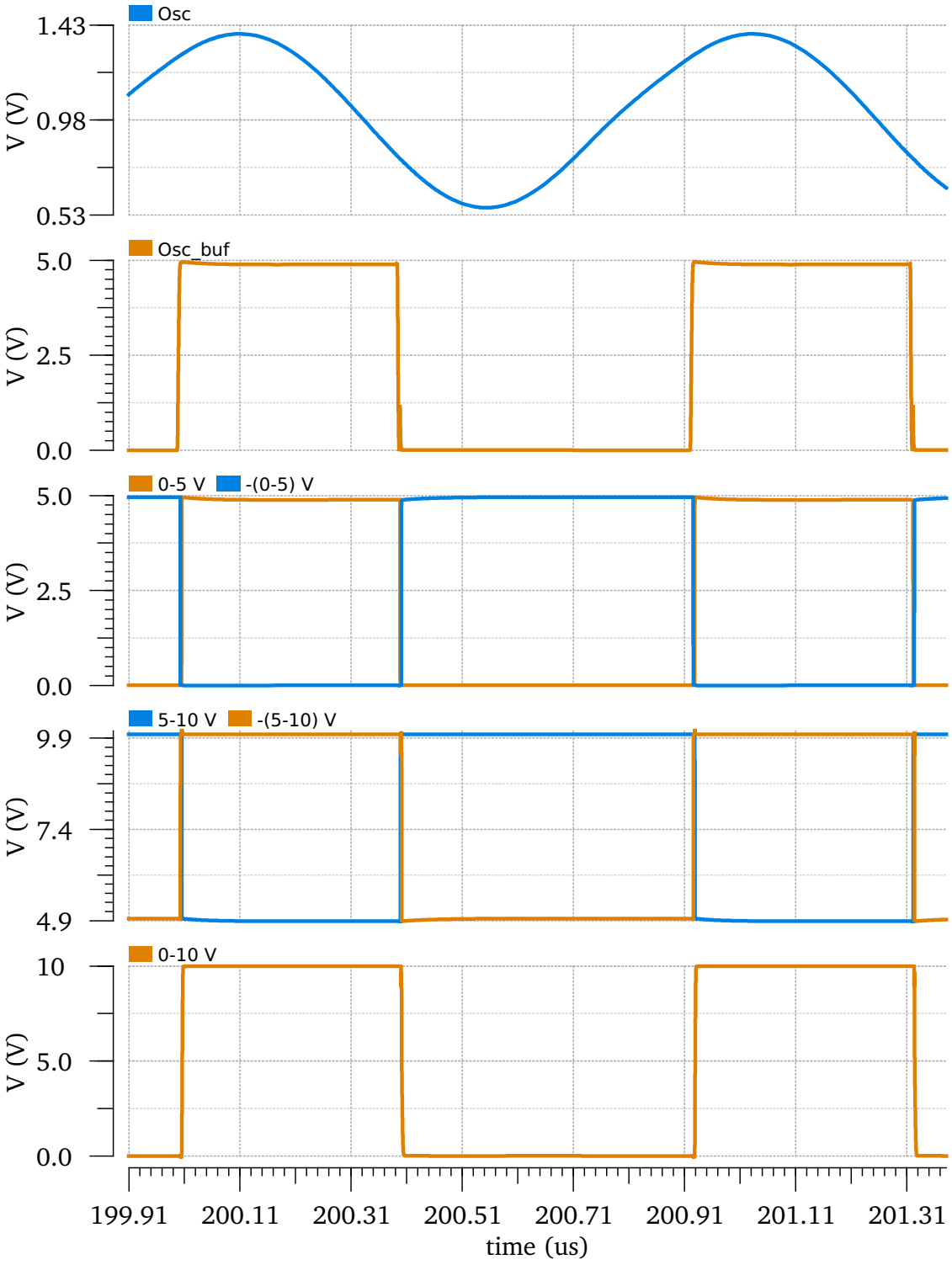

Figure 5.8. Simulation results of oscillator, non-overlapping clock signals, and level shifters.

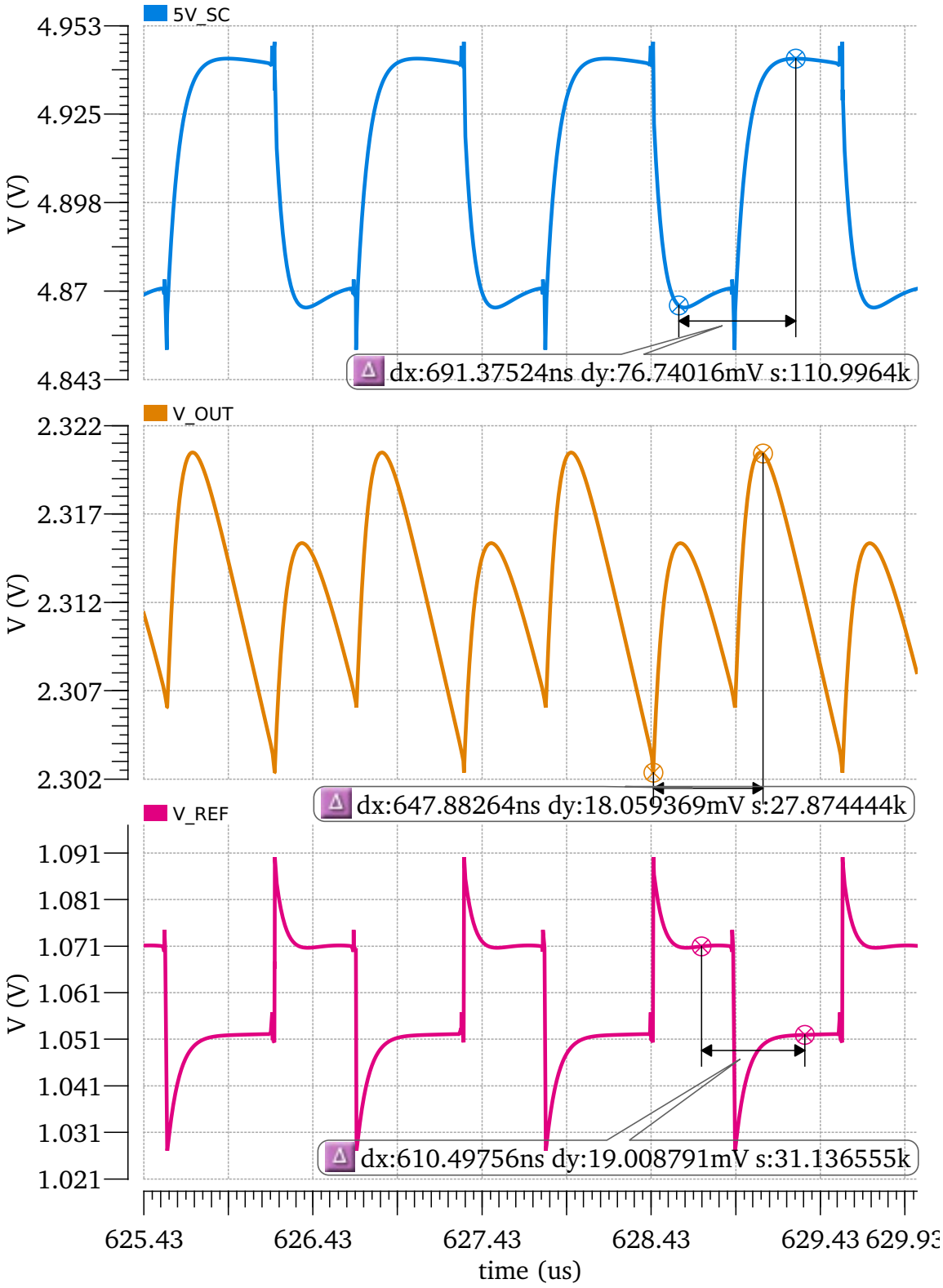

Figure 5.9. Simulation results of the switched-capacitor DC-DC converter.

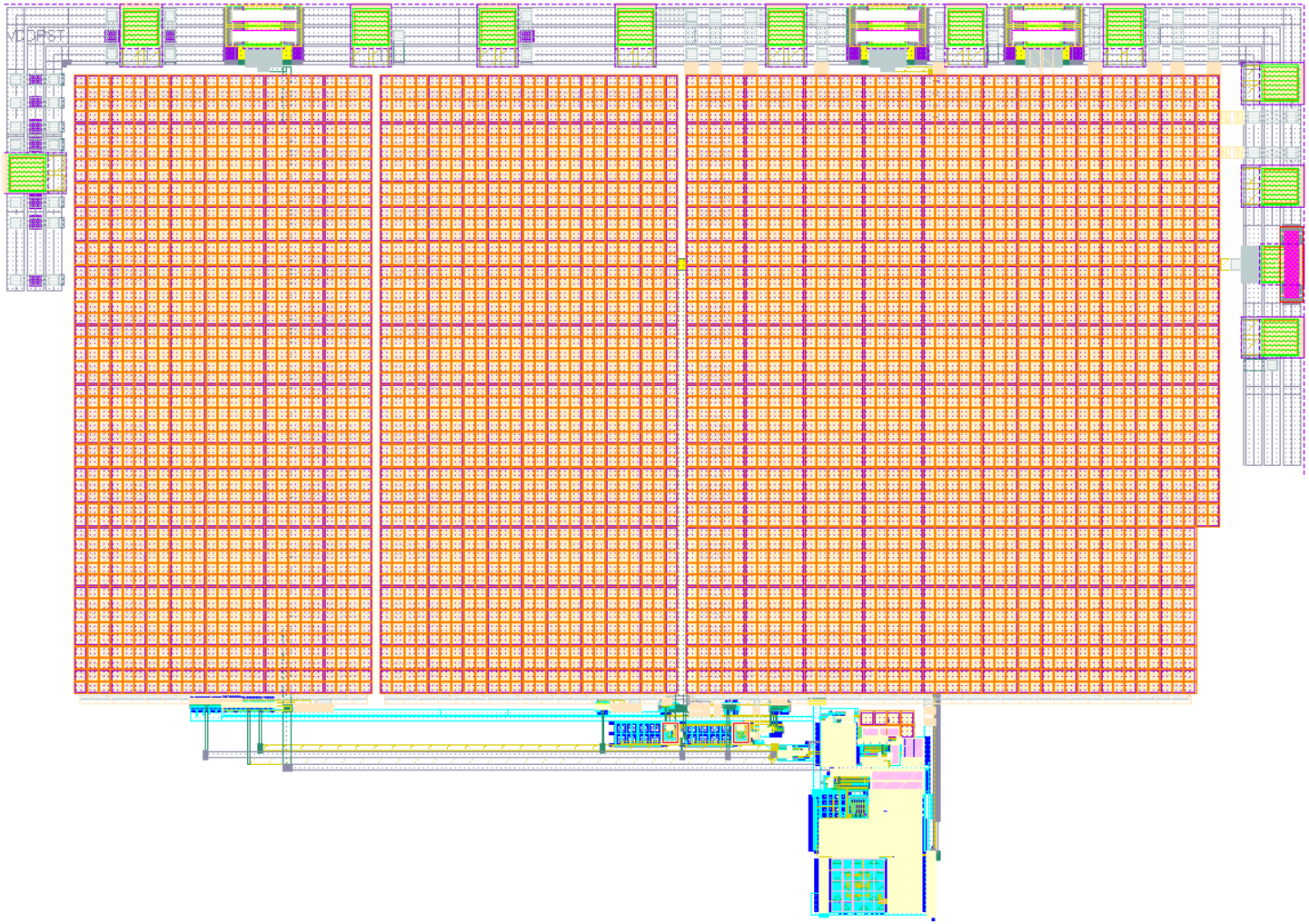

Figure 5.10. Layout of the switched-capacitor DC-DC converter.

6. MEASUREMENT RESULTS

6.1. PCB Design and Test Setup

The triboelectric harvester system is implemented in 0.18 μm HV BCD process with a-chip-area of 6.25 mm^2. Figure 6.1 shows the bonding diagram of the IC core to the quad-flat no-leads (QFN) package with 48 pins. The ground connections are bonded to the base of the package, and unused pads are left floating.

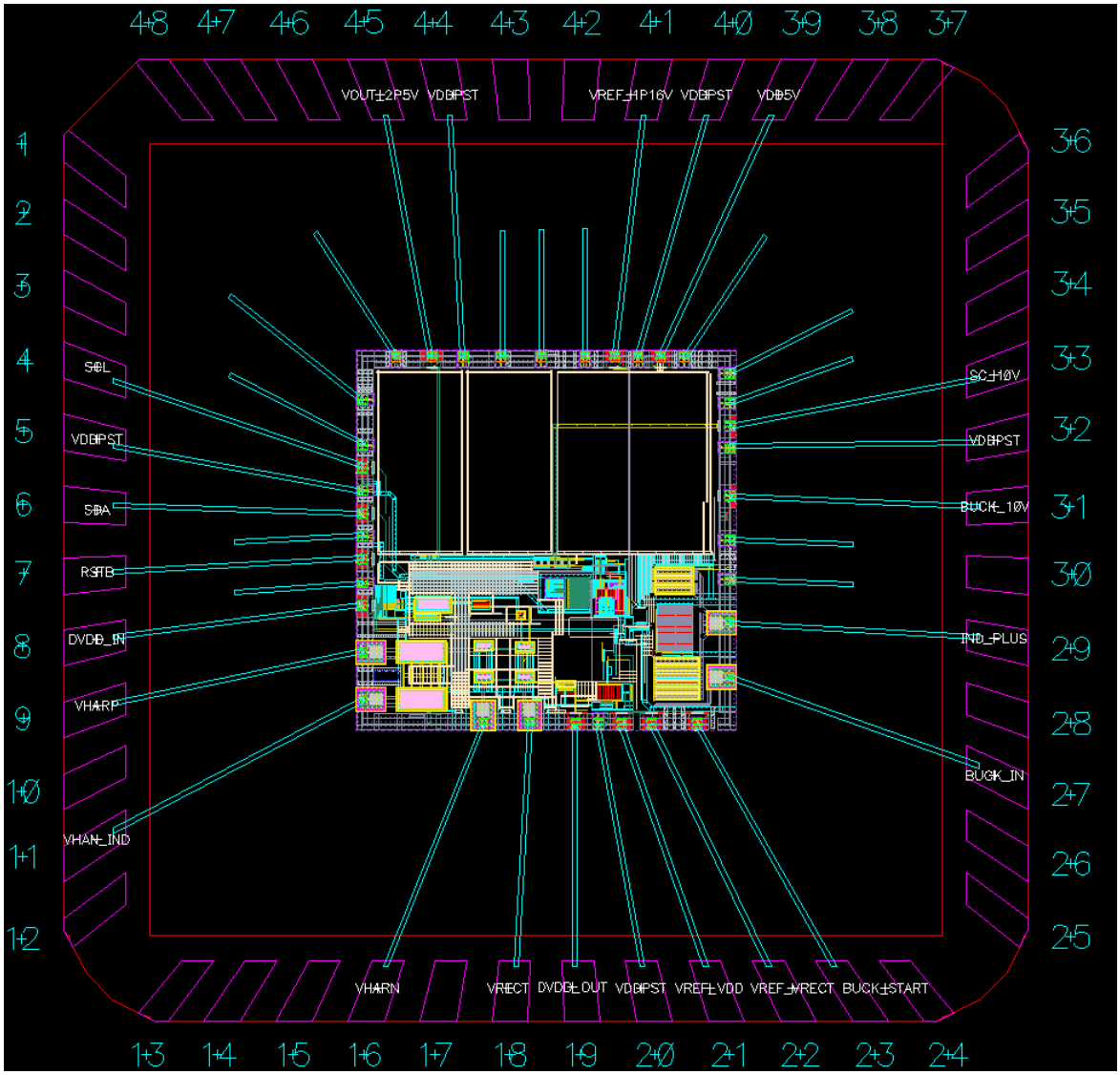

Figure 6.1. Bonding diagram of the overall layout in the QFN48/7mmx7mm package.

After sending the IC to the manufacturer, a printed-test-board is designed and sent for production. The schematic of the PCB with the component placement on it is shown in Figure 6.1. The majority of the PCB is occupied by optional inductor footprints. The PCB is designed with footprints for different inductors from different manufacturers for testing purposes. Thus, during the measurements, only one type of inductor is placed on the PCB. Also, as it can be seen from Figure 6.1, there are various different capacitor footprints on the PCB. These capacitors are selected according to their capacity and voltage ratings. The outputs with low voltages are stored on surface mount capacitors (SMDs). On the contrary, the outputs that are sensitive to leakages or require high-voltages are stored on the high-voltage capable external thin-film capacitors, which are rated up to 200 Volt levels.

In Figure 6.1, the produced PCB with some components, including the manufactured IC on its surface, is shown. The PCB also allows for multiple capacitors for each input/output node for testing purposes. Also, some switchable jumpers are used in the PCB. These jumpers allow each sub-block (parallel-SSHI interface, buck converter, and the switched-capacitor DC-DC converter) to be measured individually. Also, by configuring the jumpers, the blocks could be tested altogether. Therefore, the performance evaluation of each block could be done separately according to the measurement results.

Moreover, some test points are placed to make easy connections for the oscilloscope probes. Also, in the case of failures on the reference voltage generators, voltage dividers with potentiometers are connected to the 5 V supplies coming from the low dropout regulator and the switched-capacitor DC-DC converter. Thus, the references can be set to different values for different operating conditions. If the voltage generators are working as expected, those additional voltage reference generators are disconnected from the system by utilizing the jumpers added on their path. To sum up, the printed circuit board is designed for many cases, including the failure probabilities of the sub-blocks and some specific blocks, so that extensive coverage of measurements can be made and healthy performance evaluation can be done.

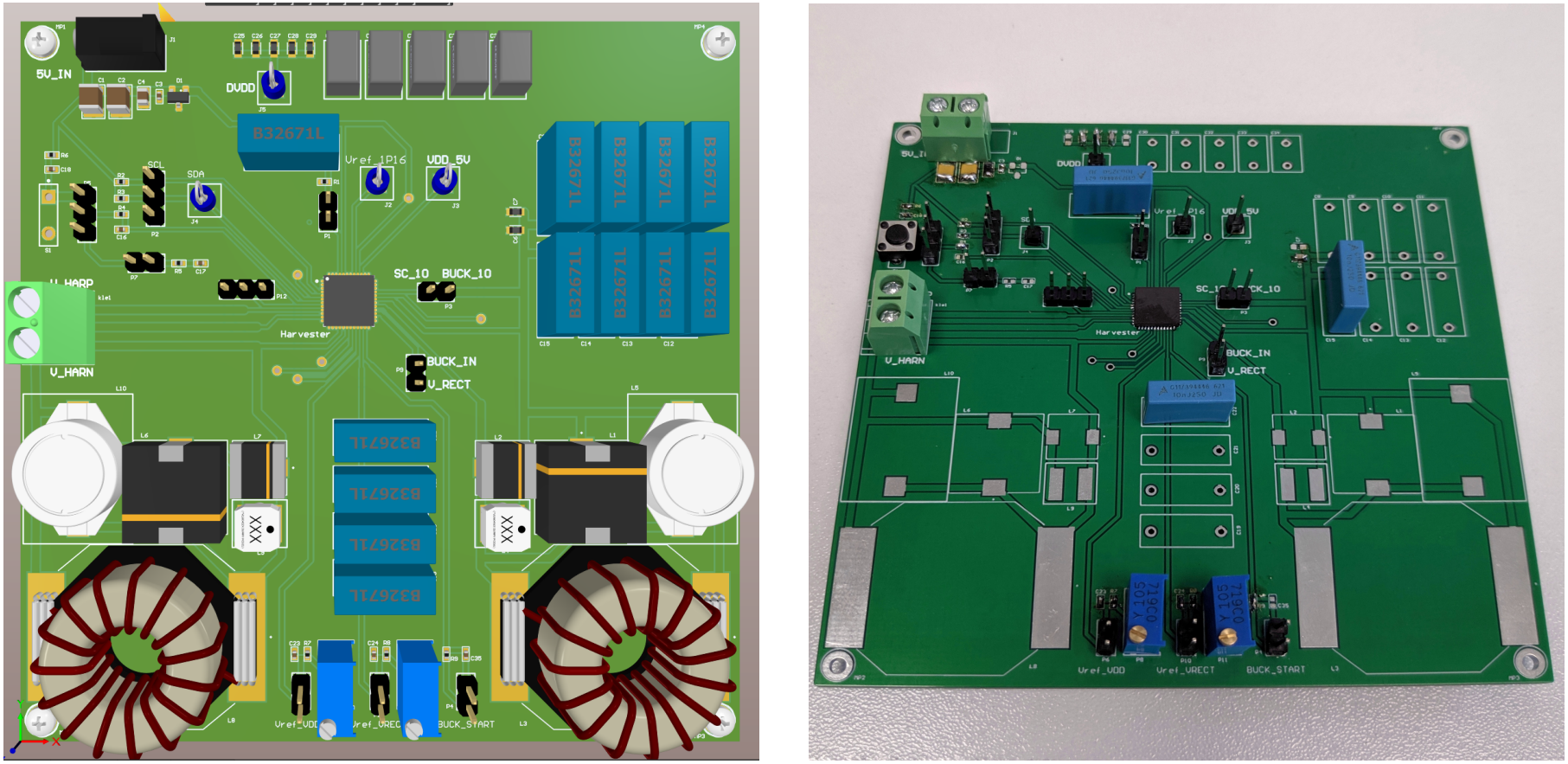

Figure 6.2. (a) 3D view of the PCB when all the components are placed on it. (b) Prepared test PCB of the whole architecture.

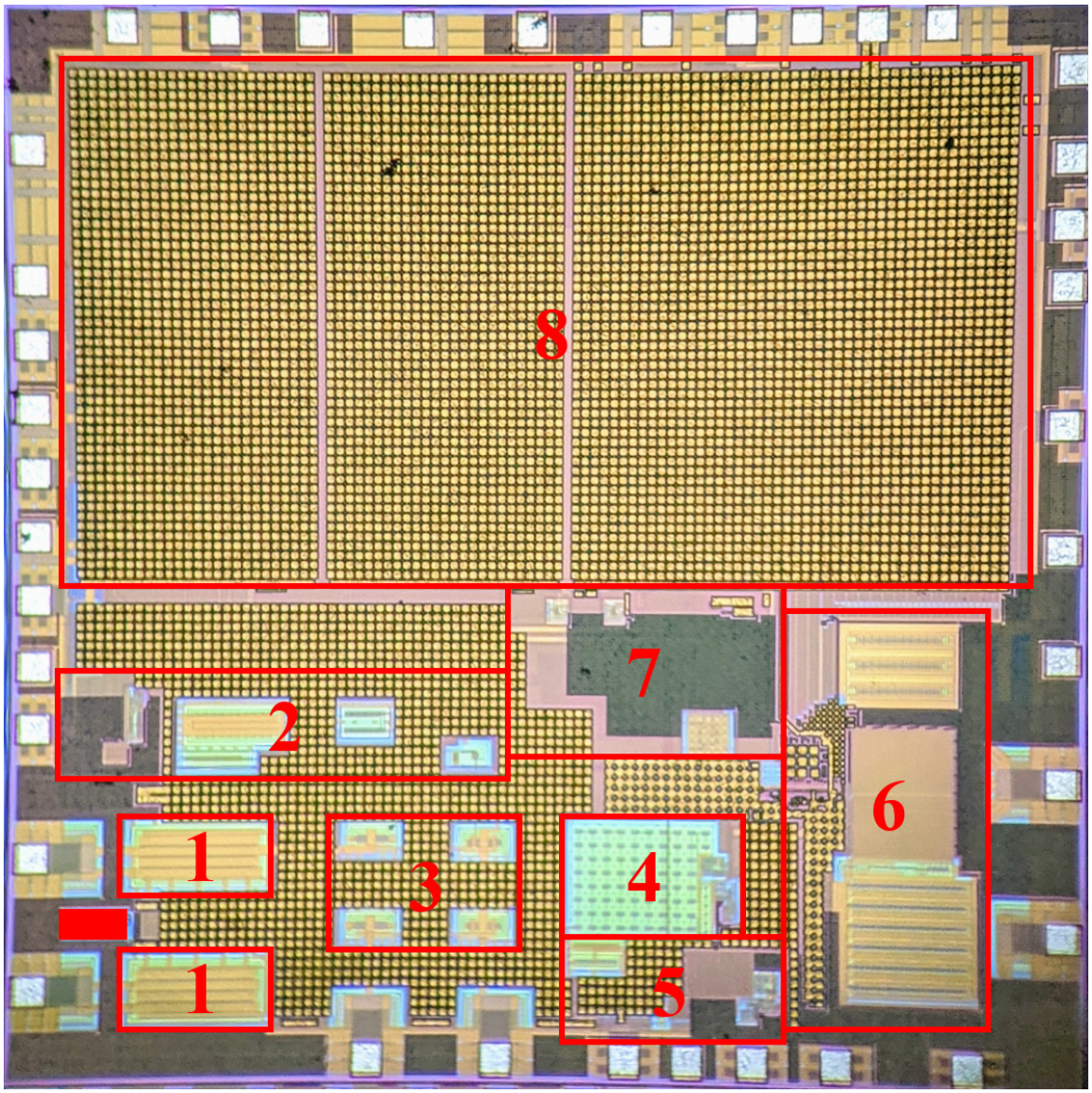

Figure 6.3. Chip micro-graph. (1) High-voltage switches (2) Zero-current detector circuitry (3) High-voltage transistors used as rectifier diodes (4) 70 V sense circuitry (5) Low-dropout regulator (6) Buck converter (7) Switched-capacitor DC-DC converter circuits (8) Capacitors used in down-conversion from 10 V to 5 V and 2 V.

Once the manufactured IC was delivered, and its die photo was taken with a high-resolution microscope in our MEMS laboratory. Figure 6.3 shows the die photo with the corresponding blocks stated in the caption. More than half of the area is occupied by the capacitors used for the switched-capacitor DC-DC converter. These capacitors are implemented in MiM capacitors since the voltages across some of them

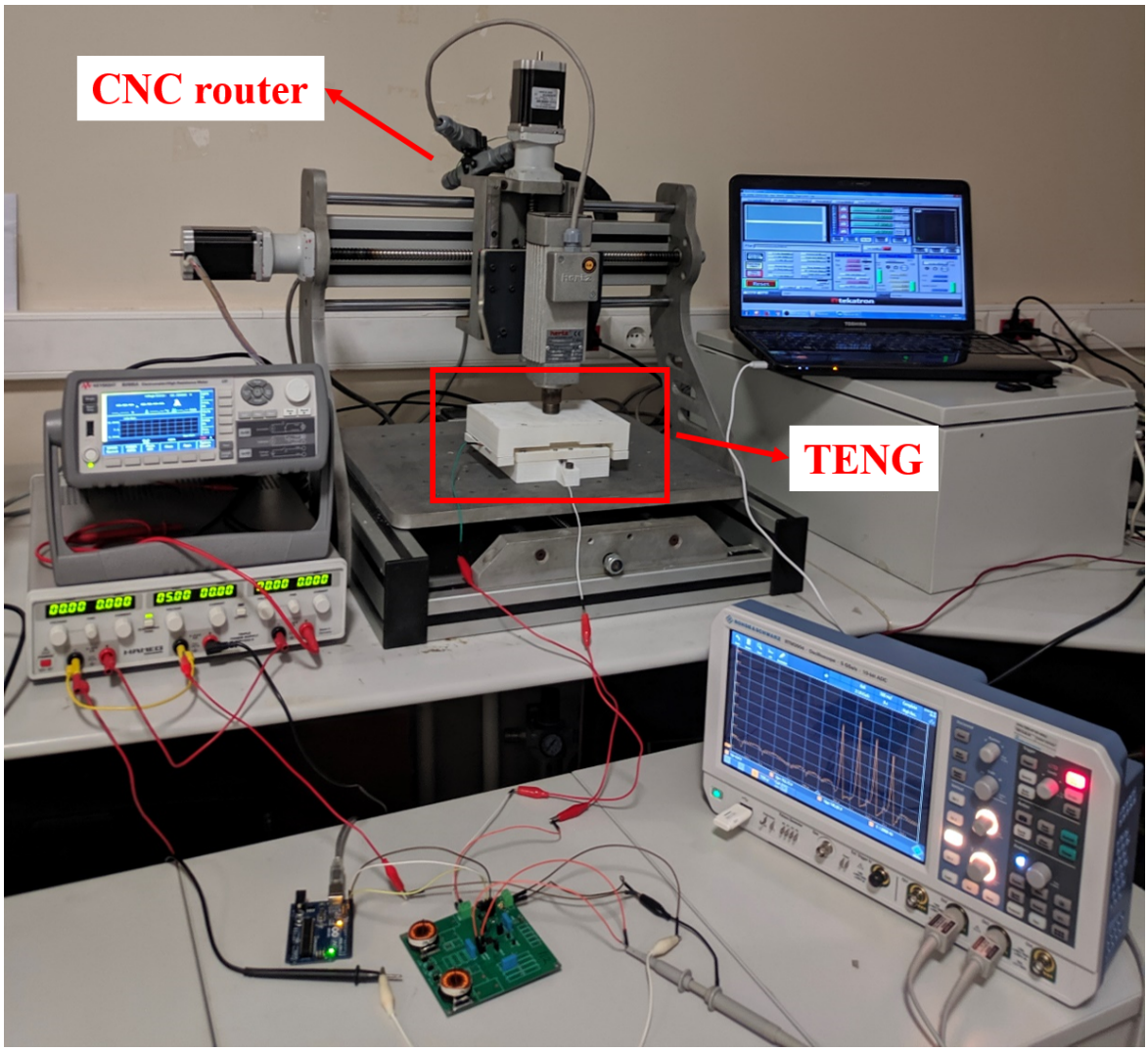

Figure 6.4. Measurement setup for testing and verification of the results.

exceed the gate breakdown voltage of the MOS capacitors. Furthermore, almost a quarter of the chip area is used by the high voltage switches and high voltage diodes.

The measurement setup is depicted in Figure 6.4. The in-house fabricated TENG and its 3D printed plastic holders are connected to a CNC router machine to achieve sine wave-like continuous movement. The movement type and speed are adjusted by software, which is run on a computer. The computer also controls an Arduino device that is used to write to the shift registers in the harvester chip to change the delays of the programmable delay blocks. An electrometer is used to measure nA levels of the

quiescent current consumption of the parallel-SSHI circuits. Since the design is not implemented to share the inductor between the parallel-SSHI and the buck converter due to the complexity of controlling the high voltage circuits, the test board contains two 1 mH low ESR inductors, one for each. Also, four low leakage, high-voltage capable external thin-film capacitors are used for each sub-block. A 10 nF is chosen for the switched-capacitor DC-DC converter in the design process for a <1% ripple at the output [49, 50]. A 4 nF capacitor is used by the low dropout regulator to ensure proper voltage regulation and power consumption. A 5 nF capacitor is used at the output of the parallel-SSHI circuitry to obtain the maximum power transfer according to [32]:

$$C_{RECT,opt} = 1.592k(C_{min} + C_{max}) \tag{6.1}$$

where k is the cycle count, C_{max} is equivalent value of the C_{TENG} when displacement distance *x(t)* is zero, and C_{min} is equivalent value of the C_{TENG} when displacement distance *x(t)* is at maximum of 8 mm.

6.2. Measurement Results and Performance Evaluation

To test the functionality of the parallel-SSHI interface circuitry, the setup shown in Figure 6.5 is used. The reason behind this setup is to make sure that the switching is working correctly, and the switch 'ON' time interval is adjustable by the I2C interface. The original setup, which is shown in Figure 1.1, can not be directly tested in this way. This results from the amount of the current injected to the system. The current injected to the system is not enough to allow measurements with an oscillator probe. The oscillator probe has an internal resistance of 10 $M\Omega$ and a few pF of internal capacitance. These internal parasitic values of the oscillator probe put a relatively large loading on the parallel-SSHI interface. As suggested later in this section, very large series resistance and a parallel connection to the probe still prevent parallel-SSHI interface operation with its loading effect. Therefore, the setup shown in Figure 6.5 is established by disconnecting the TENG from the input of the parallel-SSHI interface.

The load to the parallel-SSHI interface, which is the buck converter, is disconnected from the system. A transformer is then connected to the input and the probe to the output of the parallel-SSHI interface. The transformer has a gain of one if it is operated at 50 Hz frequency, and the gain goes to zero if the frequency is other than 50 Hz. Therefore, the signal generator frequency is set to 50 Hz. This transformer is used to isolate the signal generator that is used to observe the switching activity on the bias-flip rectifier interface. The signal generator can not be directly connected to the input of the parallel-SSHI interface, which forces the parallel-SSHI interface to be bypassed with its practically unlimited current supply.

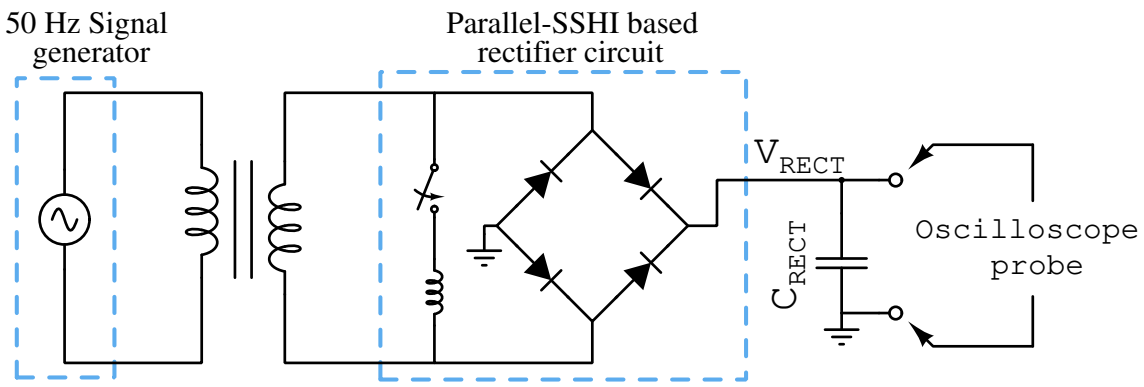

Figure 6.5. The measurement setup for the switching activity on p-SSHI interface.

To protect the parallel-SSHI interface, the output of the signal generator is set to $5V_{pp}$ as it can be seen in the upper left corner of Figure 6.6. This result is measured by the oscilloscope probe and saved as a comma-separated values (.csv) file to a flash memory, which is attached to the oscilloscope. Then, the result is plotted with the MATLAB software without doing any change in the measured values. This specific measurement shows that zero-crossing detection works as expected since the voltage spikes follow the minimum voltage 4 ms behind, which is the design specification. By changing the I2C defaults from a middle value of the 8-bit delay control, different switch on intervals can be measured as they are shown in Figure 6.6. These measurements are taken with the minimum, middle, and maximum values of the 8-bit delay control circuitry by changing the I2C defaults.

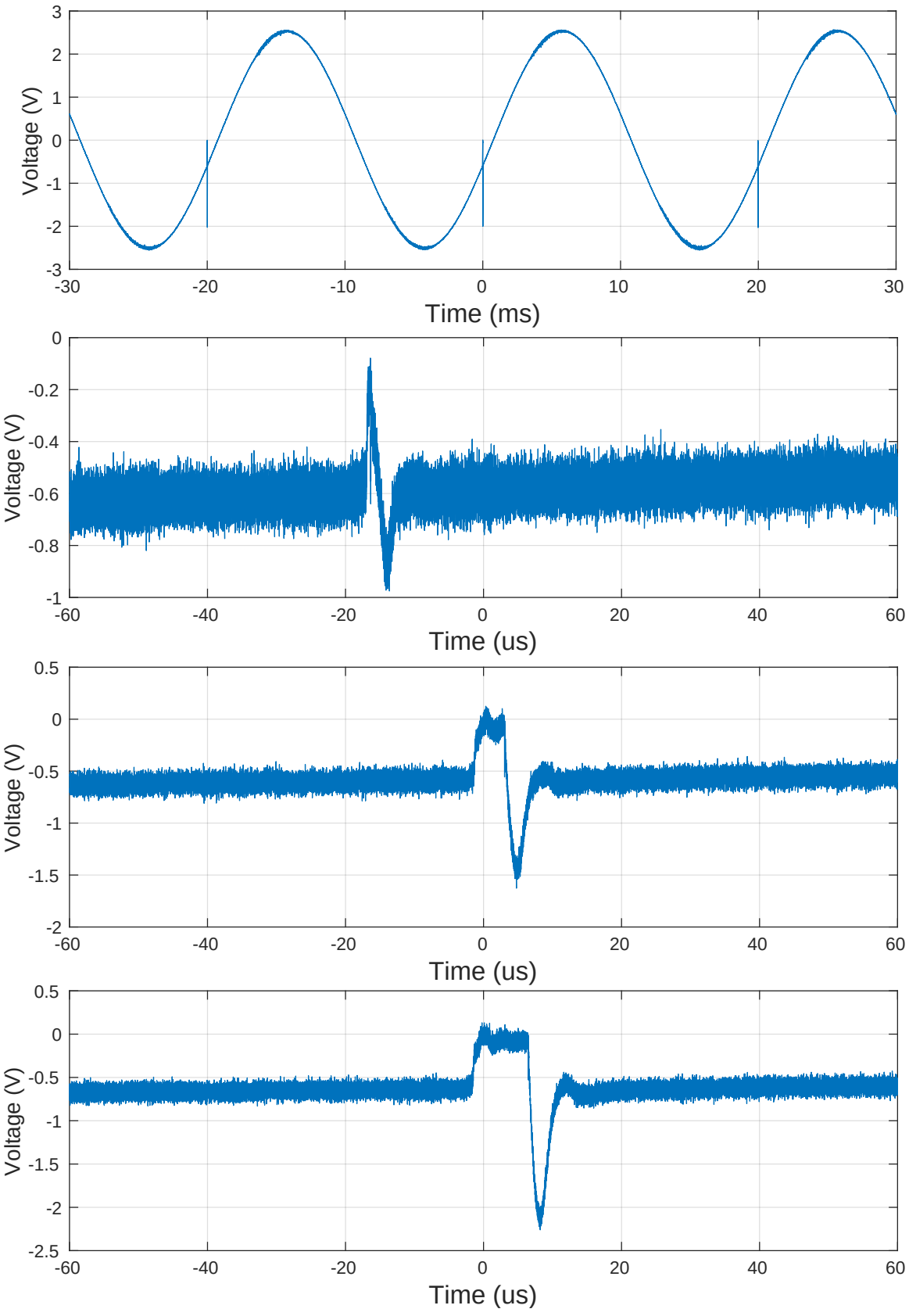

Figure 6.6. Measurement results of the switching activity on p-SSHI rectifier interface.

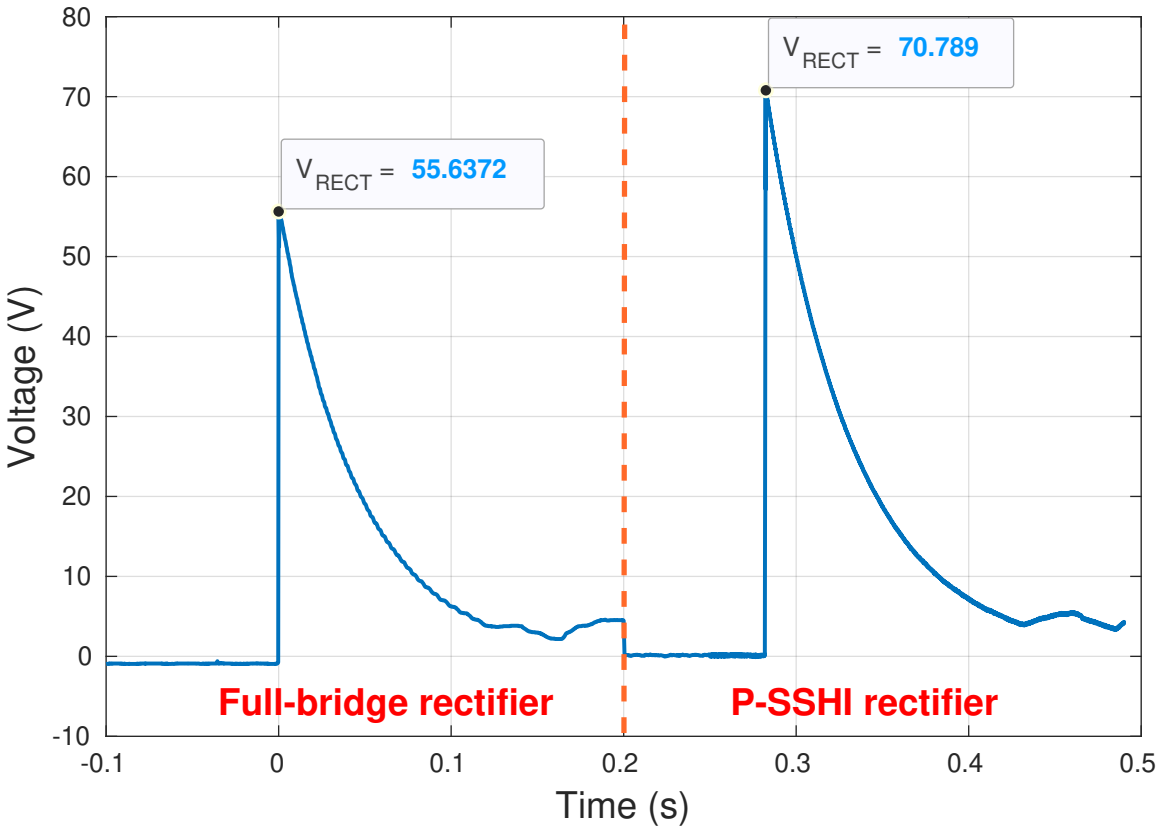

Figure 6.7. Measured waveforms of full-bridge rectifier and parallel-SSHI rectifier at the end of the third cycle.

A mechanical switch is connected between C_{RECT} and the oscilloscope probe to measure the voltage on the output without loading. If the probe is directly connected to the C_{RECT}, then the internal resistance of the probe consumes all the charges on C_{RECT}, which prevents the harvester from working. Thus, the mechanical switch is closed at the end of the third cycle, and V_{RECT} is measured as an RC decaying waveform. This measurement was done to compare the full-bridge rectifier with the parallel-SSHI rectifier shown in Figure 6.7. Compared to the full-bridge rectifier, the parallel-SSHI rectifier is 61.9% more efficient in terms of delivered power to the output. Since the TENG is designed for sub-5 Hz movements, V_{RECT} is measured for various frequencies up to 5 Hz, as shown in Figure 6.8. In order to deal with the previously mentioned measurement challenge of loading, a voltage divider is used to observe V_{RECT} when the triboelectric harvester system is operated. A series-connected

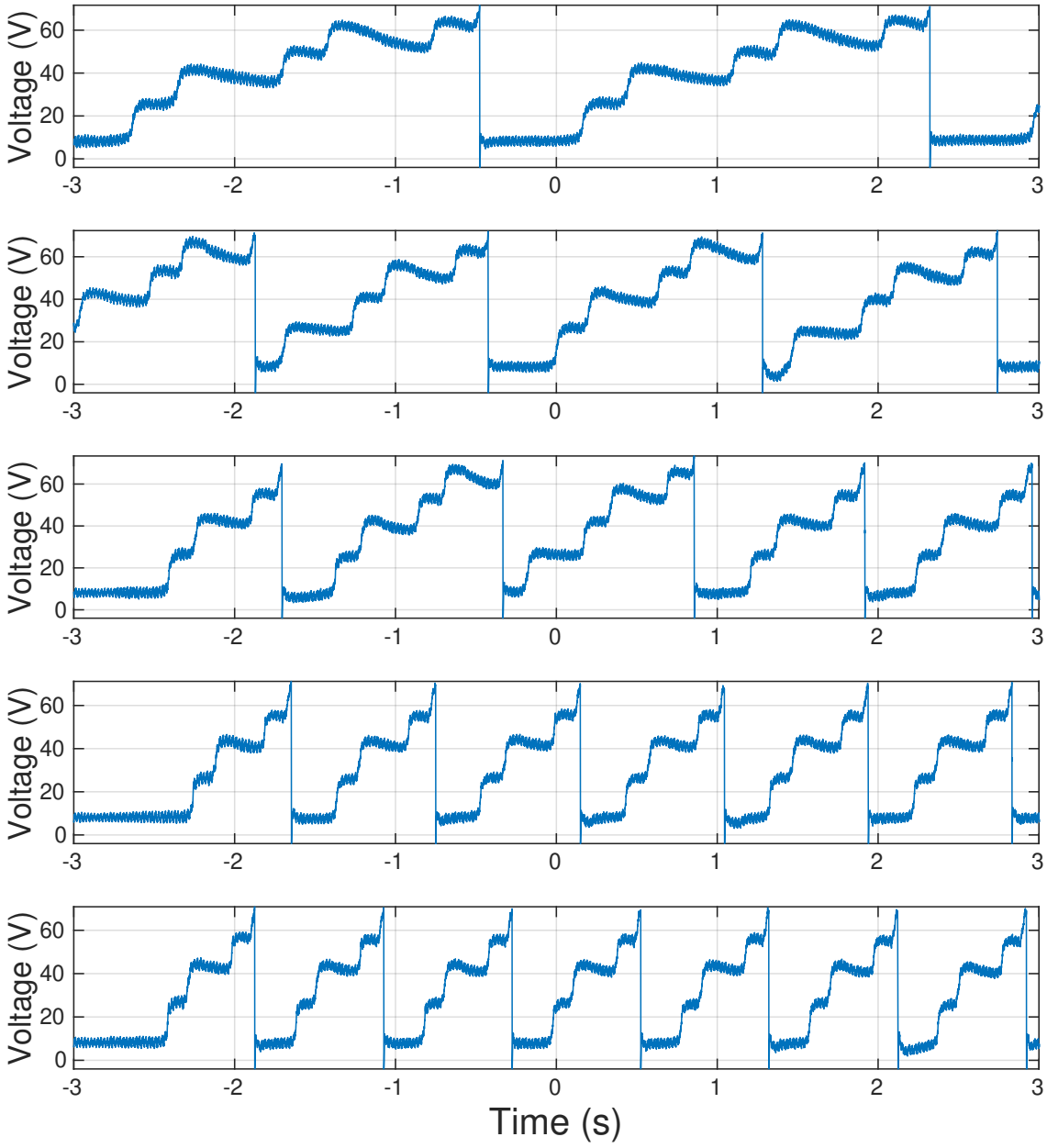

Figure 6.8. Measured waveforms of V_{RECT} at the output of the parallel-SSHI for various frequencies.

500 $M\Omega$ and 10 $M\Omega$ resistor pair is connected in parallel to C_{RECT}, with the latter resistor being terminated at the ground. The oscilloscope probe is connected across the 10 $M\Omega$ to observe the divided down version of V_{RECT}. Also, the oscilloscope probe is set to x100 magnification to observe the 70 V level since the voltage divider has a gain of 1/100.

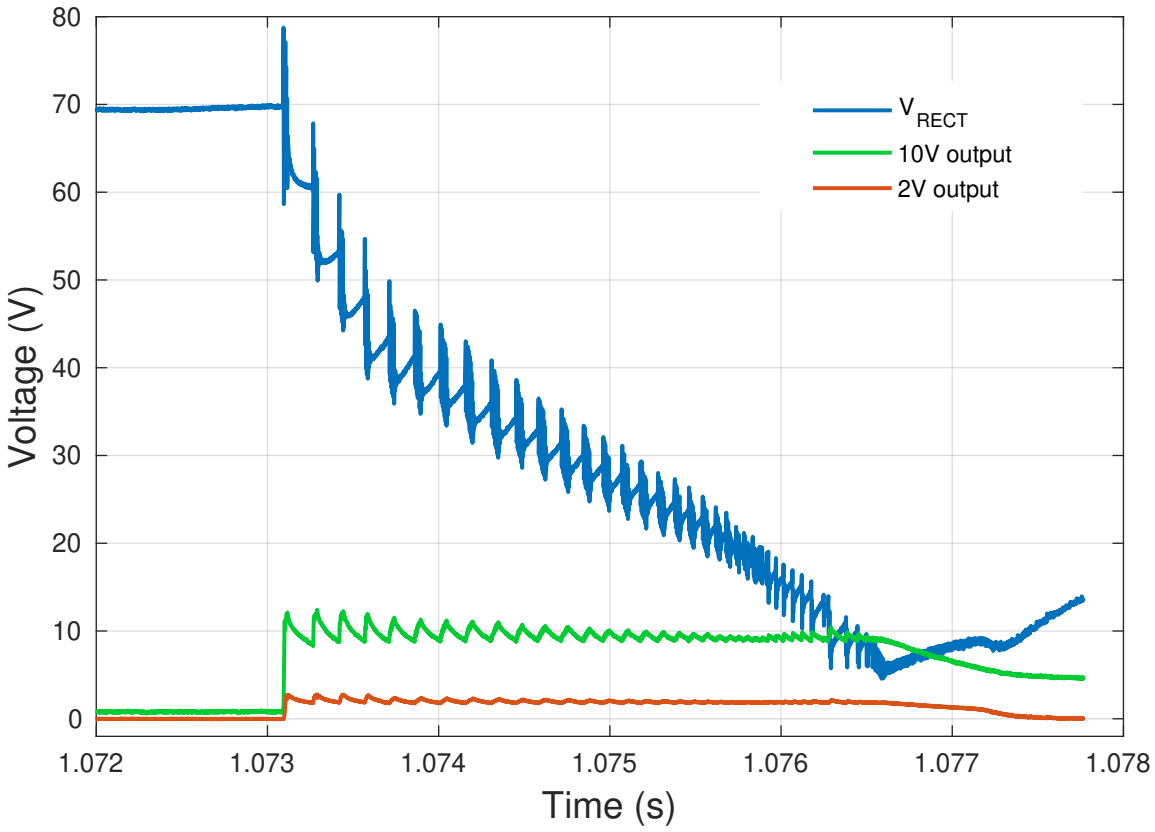

Figure 6.9. Measured waveforms of output voltages of each block during the 70-to-2 V conversion.

Upon the charging of C_{RECT} to 70 V and its detection by the 70 V sense circuit, a start signal is generated and sent to the buck converter to trigger the 70-to-2 V conversion. Figure 6.9 shows the measured outputs of each conversion block just after this triggering until the energy on C_{RECT} is drained. The 5 V output has a ripple of 180 mV and powers the buck converter internal circuitry as well as the internal circuitry of the SC DC-DC converter itself. The 2 V system output has a ripple of 24 mV and can power up a typical [51] sensor node for a duration of up to 4 ms. The 5 V and 2 V outputs measurements are shown in Figure 6.10. Since each sub-block was designed to be operable standalone, their efficiencies are measured individually. The parallel-SSHI circuitry extracts energy with an efficiency of 69.2% according to the measurements. Efficiency lost is due to the quiescent current of the parallel-SSHI circuits, which is measured as 53 nA by an electrometer, and current consumed during switching.

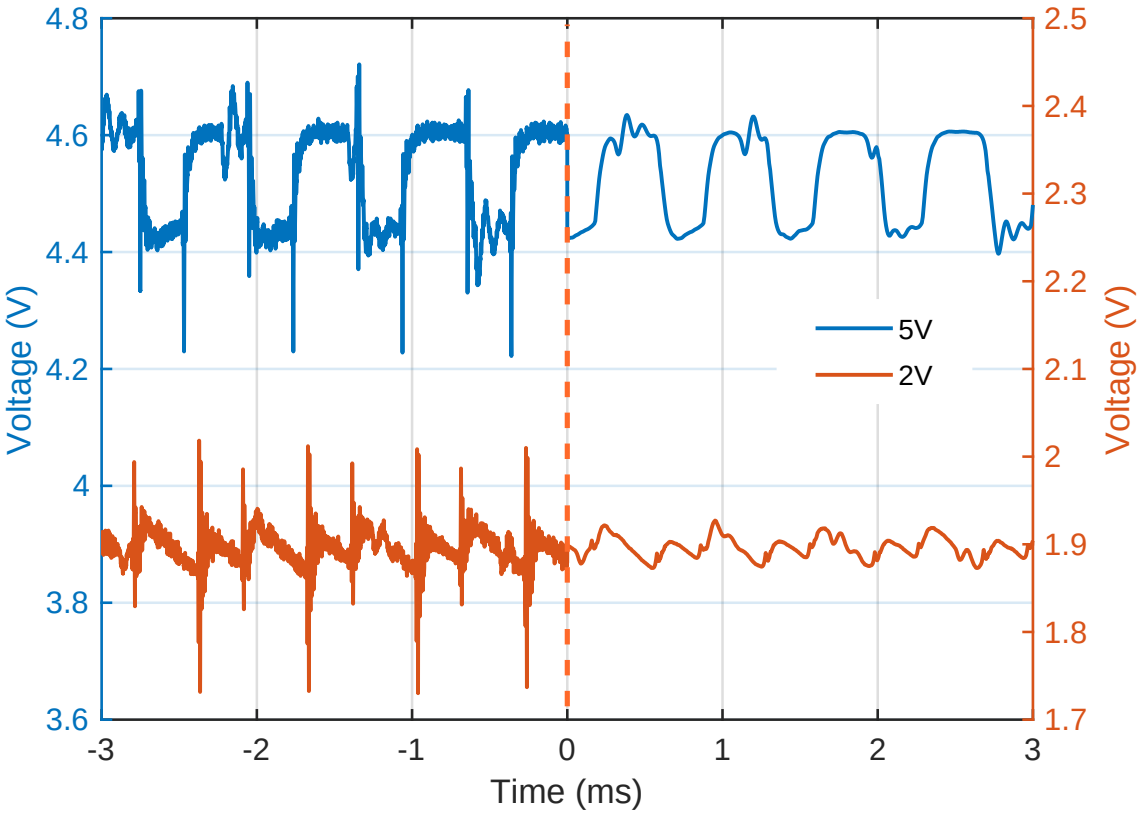

Figure 6.10. Measured waveforms of 5 V output used for powering buck converter and internal switched-capacitor DC-DC converter, and 2 V output of the switched-capacitor DC-DC converter (unfiltered form vs filtered form with the internal digital filter of the oscilloscope).

Buck converter average efficiency is measured as 41.53% as the input discharges from 70-to-10 V with a load of 23 $k\Omega$ resistance. The average efficiency of the switched-capacitor DC-DC converter is measured as 54.39% when the input discharges from 11.5-to-6 V with a load of 5 $k\Omega$ resistance. These efficiency measurements are shown in Figure 6.11 and Figure 6.12, respectively. When the switched-capacitor DC-DC converter is connected as a load to the buck converter for the conversion from 70-to-2 V, the average efficiency of the DC-DC converters is measured as 24.3%. In this case, the peak efficiency of the DC-DC converters is measured as 47.27%. Therefore, the end-to-end peak efficiency of the energy harvester system is measured as 32.71%. This efficiency is enough to power a wireless sensor chip by delivering an average power of 722 μW for 4 ms duration, which corresponds to total energy delivery of 2888 nJ to the load by the proposed triboelectric energy harvesting system.

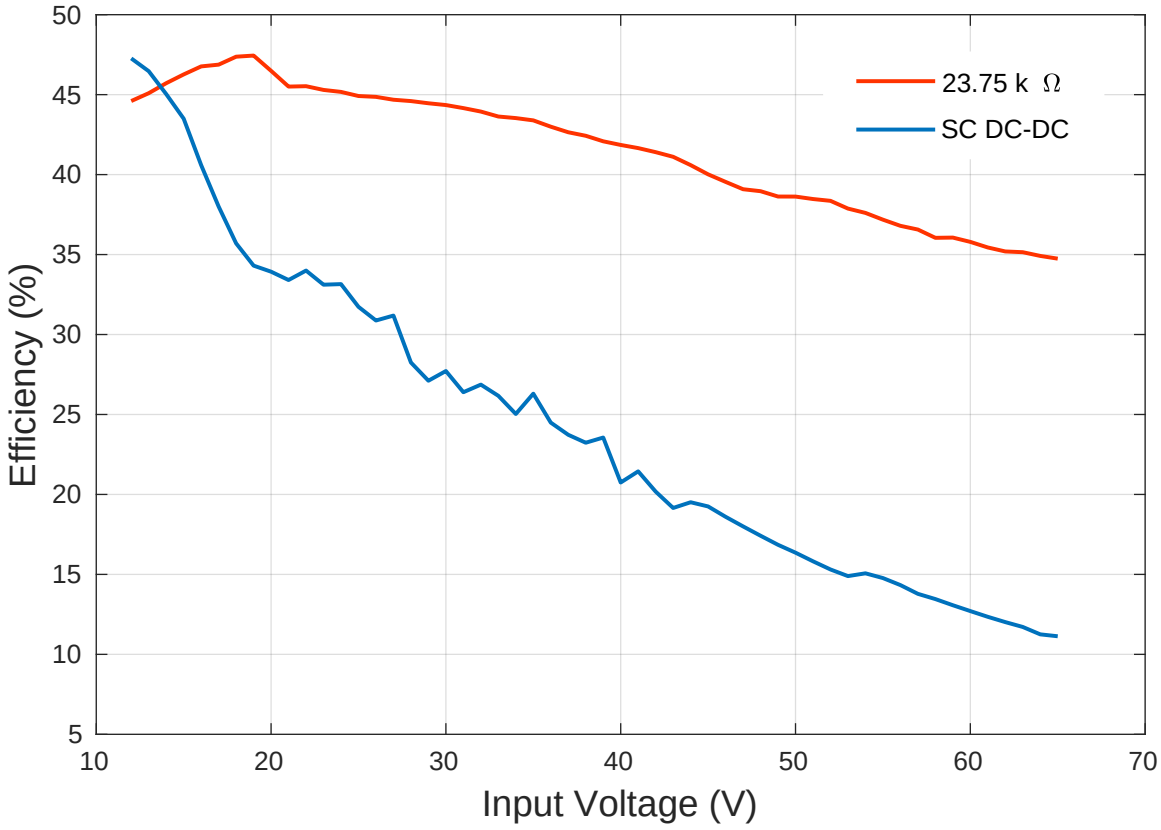

Figure 6.11. Measured efficiencies of the buck converter for different loads.

Table 6.1 summarizes the chip performance and compares it to previous studies in terms of the key properties. [19] and [23] utilize piezoelectric harvesters with the use of parallel-SSHI technique to extract energy. They both show substantial improvements (2x to 6.81x) compared to conventional full-bridge rectifiers. [19] provides only buck converter efficiency, which is 85%, and the system can provide 47 μW power to the load. The system proposed in [23] sends 36.8 μW power to the load when it is operated at resonance frequency with an end-to-end peak efficiency of 95.4%. However, they have significantly lower output power than our proposed design, where our system is capable of delivering 722 μW power to the load. In [39], a triboelectric energy harvester system is presented with an operating frequency from 20 Hz to 50 Hz. A fractional V_{OC}-based MPPT technique is implemented with a high voltage capable rectifier and a high voltage dual-input buck converter to achieve an end-to-end efficiency of 52.9%. This efficiency value significantly drops when it is operated at 20 Hz on human skin.

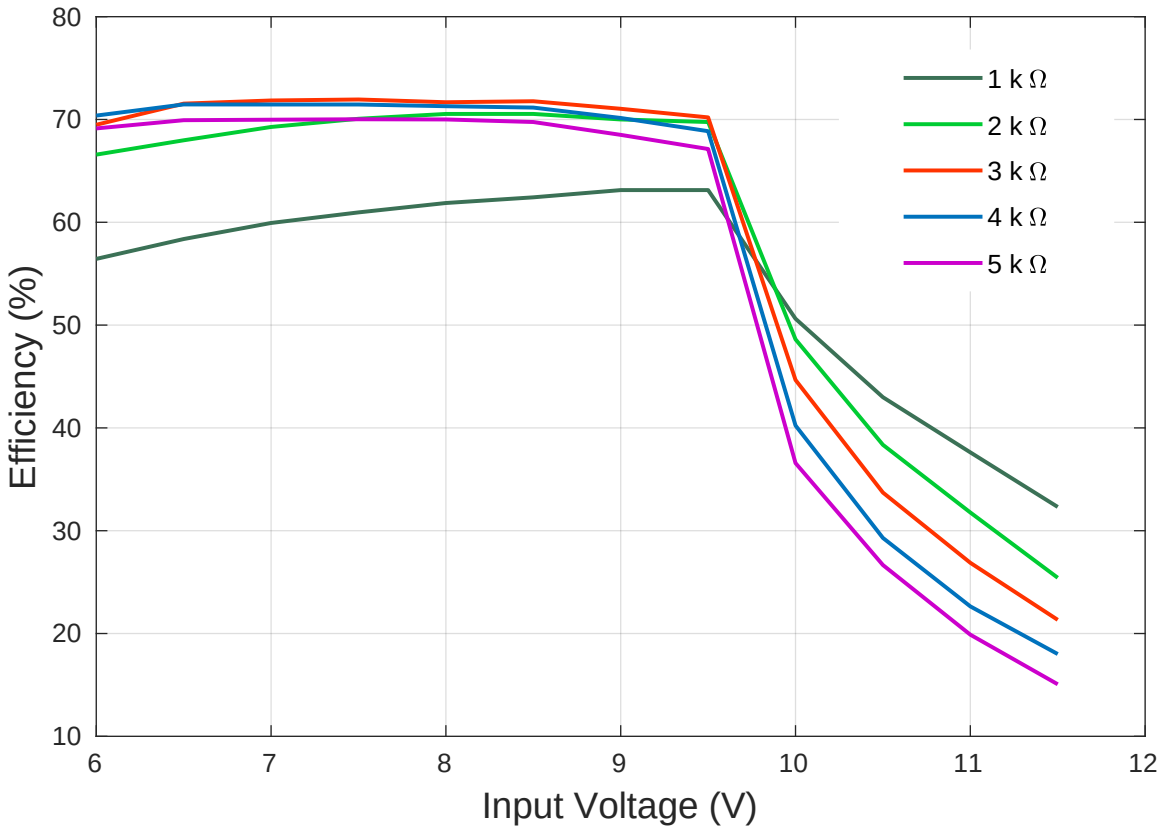

Figure 6.12. Measured efficiencies of the switched-capacitor DC-DC converter for different loads.

On the other hand, our proposed design can work for 1-to-5 Hz motions with adequate efficiency. In [41], the first adaption of parallel-SSHI to triboelectric energy harvesters can be seen. However, it is implemented with discrete components with deficient output power and not targeting the critical frequency range from 1 Hz to 5 Hz. In a nutshell, our system is superior to the above systems in terms of delivered power and ability to harvest energy from less than 5 Hz ambient motions. Also, our design does not require any external stimulus other than an ambient motion for operation, i.e., neither an external power supply nor a start-up circuitry is needed.

Table 6.1. Comparison with other energy harvesters from the literature.

Reference	**JSSC 2010 [19]**	**JSSC 2016 [23]**	**JSSC 2019 [39]**	**TPEL 2019 [41]**	**This thesis**
Technology	$0.35\mu m$ CMOS	$0.35\mu m$ CMOS	$0.18\mu m$ HV BCD	Discrete	$0.18\mu m$ HV BCD
Harvester Type	Piezoelectric	Piezoelectric	Triboelectric	Triboelectric	Triboelectric
Extraction Technique	p-SSHI	p-SSHI with AR	Fractional V_{OC}	p-SSHI	p-SSHI
Regulator Architecture	Buck + SC	Buck + LDO	Dual-input Buck	RC	Buck + SC
Input Voltage [V]	2.4	0.8	3.5 - 70	< 20	12 - 70
Output Voltage [V]	1.8	0.7 - 5	2 - 5	1.45	2
Self-Powered / Cold Start	No	Yes	Yes	No	Yes
Operation Frequency [Hz]	225	134.6 - 229.6	50	6	1 - 5
Extraction Improvement	2x-3x	2.7x - 6.81x	N/A	3.43x	1.62x
Output Power [μW]	47	36.8 @resonance	10.95	0.2	722
End-to-End Efficiency	85% (For Buck only)	95.4%	52.9%	N/A	32.71%

7. CONCLUSION AND FUTURE WORK

7.1. Overview

In this thesis, the first on-chip parallel-SSHI implementation of a triboelectric energy harvester is proposed. The triboelectric nanogenerator is manufactured in-house. The characteristics of the triboelectric nanogenerator are modeled and imported to the CAD tools to be used to design a 70-to-2 V energy harvesting integrated circuit.

The integrated-circuit operation is divided into three sub-blocks: parallel SSHI interface, buck converter, and the switched-capacitor DC-DC converter. The design procedure started with the justification of the parallel-SSHI interface usage, as it is compared with the full-bridge rectifiers. Then, the parallel-SSHI interface's superiority is confirmed with the measurement results where 61.9% more power is delivered to the output when the parallel-SSHI interface is used. Then, arousing complexities are discussed for the low power circuit design in the case of high voltage, and solutions for these problems are proposed for every specific case to obtain a reliable system architecture. The amount of power that is available to the system led design to be two-stage. The first stage, which consists of TENG and parallel-SSHI interface, charges an output capacitor to 70 V in three seconds. The second stage, which consists of a buck converter and the switched-capacitor DC-DC converter, down converts 70 V to 2 V and delivers power to the load in 4 ms.

The design process continues with the down-conversion stages. The buck converter down-converts 70 V to 10 V and deals with the high voltage challenges in every step of the design due to the technology breakdown voltage level. The buck converter takes advantage of high voltage level shifters, high voltage transistors and diodes, and high voltage wells that are available in the design kit to deal with the high voltages. The buck converter load is the switched-capacitor DC-DC converter, which down-converts 10 V to 2 V in two cascaded stages. The switched-capacitor DC-DC converter utilizes level shifter circuits to deal with the technology breakdown voltage

level. The average efficiency of the DC-DC converters is measured as 24.3%, and the peak efficiency of the DC-DC converters is measured as 47.27%.

As a final remark, the system is self-powered; hence no external power supply is used. High-voltage circuits are carefully designed to operate up to 70 V without oxide or junction breakdown. Energy is accumulated on an external capacitor C_{RECT} until its voltage reaches 70 V, which happens in three cycles for 1 Hz motion. A subsequent start signal initiates the buck down-conversion from 70 V to 2 V through a cascade of a buck converter and a switched-capacitor DC-DC converter. The output can supply 722 μW power to a load for 4 ms. The design is manufactured in 0.18 μm HV BCD process with a chip area of 6.25 mm^2 and the measured end-to-end peak efficiency of the energy harvester system is 32.71% which results in the delivery of 2888 nJ in 3 seconds.

7.2. Future Work

The integrated-circuit manufactured in this thesis study gave a profound insight related to the high voltage circuit operations. The measurement challenges that we faced during this process enlightened us with some very bright ideas that can be taken into account for the next level.

As future work, sub-block can be merged without allowing standalone operations to decrease the possible losses due to the parasitics coming from the pins and paths on the PCB. The efficiency graphs of the buck converter and switched-capacitor DC-DC converters show that there is a significant power loss when operating the circuits near the edge of the technology breakdown voltage levels. Therefore, a better down-conversion step choice such as the down-conversion of 70 V to 8 V and then 8 V to 2 V would be a much better option in terms of obtainable efficiency.

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