ROBUST ULTRA-WIDEBAND TRANSCEIVER INTEGRATED CIRCUIT DESIGN

by

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ABSTRACT

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Pulse-based wideband and UWB radios are well known for their use in radar technology. UWB has also been popular for its use on high data rate applications in recent years. UWB wireless sensor networks are known for their low power and long range operation. UWB is not only a low cost and low complexity technology with precise ranging and multipath immunity properties, but it also has certain challenges such as pulse based synchronization, which requires low jitter and precise delay blocks. In the dissertation, low-power, high data-rate, and moderate range IR-UWB transceivers are designed with robustness to impulsive noise. The non-idealities of the receiver and transmitted pulse are also studied to create an efficient IR-UWB transceiver. As a first step, the existence of the impulsive noise in wideband channels is shown with measurements and fitted noise models. Top level computer automated system models are written, extensive simulations are performed, and performance metrics are defined. Then, these system models are converted to circuits in a top-down fashion. Various UWB transceiver architectures are reviewed in terms of performances and hardware complexity. Then, both coherent and non-coherent IR-UWB transceivers architectures are realized in standard CMOS technology. During the thesis work, three chips have been fabricated using UMC 130 MMRF technology. Co-planar waveguide FR4 PCBs and UWB antenna designs were realized to realize overall system and minimize coupling problems.

ÖZET

GÜRBÜZ ULTRA-GENİŞBANT ENTEGRE DEVRE TASARIMI

Darbe tabanlı geniş bant radyoların radar teknolojisinde yaygın olarak kullanıldığı görülmektedir. Geçtiğimiz senelerde ultra-genişbant (UGB) sistemler yüksek hızlı veri aktarımı gereken uygulamalarda oldukça popüler olmuşlardır. UGB kablosuz algılayıcı ağları, düşük güç ve uzun mesafelerde calışma özellikleri ile öne çıkmaktadırlar. Aynı zamanda düşük masraflı ve karmaşıklıktaki bir mimari yapı ithiva etmekle birlikte yüksek hassasiyette uzaklık ölçümü özelliği bulunmaktadır. Bununla birlikte çok yollu yayılma problemine karşı bağışık özelliği vardır. Ancak darbe tabanlı işaretlerin eşitlenme zorluğu nedeni ile düşük seğirmeli ve hassas geciktirmeli yapıların kullanılması gibi zorlukları vardır. Tez çalışması içersinde düşük güç tüketimli, yüksek veri hızında, orta derece mesafede çalışan ve aynı zamanda dürtün gürültüye karşı gürbüz alıcı-vericiler tasarlanmıştır. Etkili bir dürtün radyo UGB alıcı-verici ikilisi tasarlanabilmesi için gönderilen darbe işaretinin ve alıcı yapısının ideal olmayan parametreleri üzerinde çalışılmıştır. Tasarımda birinci adım olarak dürtün gürültünün geniş bantlı kanallarındaki varlığı ölçüm sonuçları ve bilgisayar modellemeleri kullanılarak kanıtlanmıştır. Yüksek seviye otomatik hale getirilmiş bilgisayar sistem modelleri yazılarak performans değerleri belirlernmiştir. Bu bilgisayar modelleri tepeden tabana tasarım kullanılarak devre yapılarına dönüştürülmüştür. Bir çok geniş bantlı alıcı-verici yapısının başarımı ve donanım karmaşıklığı incelenmiştir. Sonrasında evre uyumlu ve evre uyumsuz yapılarının ikisi içinde darbe tabanlı radyo alıcı-verici tasarımları gerçeklenmiştir. Tez süresince üç adet yonga tasarımı UMC 130 MMRF teknolojisi kullanılarak üretilmiştir. Düzlemdeş dalga kılavuzu yöntemi kullanılarak baskı devreler ve UGB anten tasarımları yapılarak tüm sistem gerçeklenmiş ve bağlaşım sorunları en düşük düzeye indirgenmiştir.

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LIST OF SYMBOLS

a_1	digital bit 1
a_2	digital bit 2
a_3	digital bit 3
a_4	digital bit 4
a_5	digital bit 5
a_6	digital bit 6
A	Impulsiveness Variable
C_{Load}	Load Capacitor
C_{ps}	Pulse Shaping Capacitor
dB	Decibel-watts, logarithmic unit
dBm	Decibel-milliwatts, logarithmic unit
GHz	Giga-hertz, frequency unit
I	Current
kbps	Kilo bits per seconds, data rate
kHz	Kilo-hertz, frequency unit
Mbps	Mega bits per seconds, data rate
MBps	Mega bytes per seconds, data rate
MHz	Mega-hertz, frequency unit
mm^2	Area of the chip in metric system
mW	milliwatt, power unit
nm	Nano-meters, metric unit
ns	Nano-seconds, time unit
fF	Femto-farads, capacitor unit
pF	Pico-farads, capacitor unit
pJ	Pico-joules, energy unit
pJ/pulse	Pico-joules per pulse, figure of merit
ps	Pico-seconds, time unit
R	Resistance

T_d	Delay
V_{in}	Delay
V_{DD}	Supply
τ	Pulse width in nanoseconds
μm^2	Area in metric system
μW	micro-watt, power unit
Γ'	Noise power
ε	Envelope of the interference

LIST OF ACRONYMS/ABBREVIATIONS

3D-HD	Three-Dimensional High Definition
ADC	Analog to Digital Converter
ASIC	Application Specific Integrated Circuit
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BPF	Band Pass Filter
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CAD	Computer Aided Design
CLK	Clock
CMOS	Complementary Metal Oxide Semiconductor
CSI	Current Starving Inverter
DCDE	Digitally Controlled Delay Element
DCO	Digitally Controlled Oscillator
DFF	D Type Flip Flop
DLL	Delay Locked Loop
DS	Direct Sequence
DVK	Development Kit
EMF	Electromagnetic Field
EPB	Energy Per Bit
EPP	Energy Per Pulse
ESD	Electrostatic Discharge
EVK	Evaluation Kit
FOM	Figure Of Merit
FF	Fast-Fast
FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FSK-OOK	Frequency Shift Keying On-Off Keying

GG	Glitch Generator
GPR	Ground Penetrating Radar
GSM	Global System for Mobile Communications
HD	High Definition
HDMI	High Definition Multimedia Interface
I&D	Integrate and Dump
IEEE	The Institute of Electrical and Electronics Engineers
IFFT	Inverse Fast Fourier Transform
IR	Impulse Radio
IR-UWB	Impulse Radio Ultra-wideband
LNA	Low Noise Amplifier
MATLAB	Matrix Laboratory
MEMS	Microelectromechanical Systems
MB-OFDM	Multi-Band Orthogonal Frequency Division Multiplexing
MMRF	Mixed Mode Radio Frequency
MODELSIM	Verilog Simulator
MRC	Maximal Ratio Combining
NF	Noise Figure
NMOS	N-channel Metal Oxide Semiconductor
OOK	On-Off Keying
OFDM	Orthogonal Frequency Division Multiplexing
OPM	Orthogonal Pulse Modulation
PA	Power Amplifier
PAM	Pulse Amplitude Modulation
PCB	Printed Circuit Board
PDF	Probability Density Function
PER	Packet Error Rate
PG	Pulse Generator
PMOS	P-channel Metal Oxide Semiconductor
PlL	Phase Locked Loop
PPM	Pulse Position Modulation

PRF	Pulse Repetition Frequency
Q	Quality Factor
QFN	Quad Flat No-leads
QPSK	Quadrature Phase Shift Keying
RAM	Random Access Memory
RF	Radio Frequency
RFID	Radio-Frequency Identification
RTL	Register Transfer Level
SMA	Sub-miniature Version A
SNR	Signal to Noise Ratio
SS	Slow-Slow
S-OOK	Synchronized On-Off Keying
S-V	Saleh-Valenzuela
T	Temperature
TDC	Time-to-Digital Conversion
TH	Time Hopping
TV	Television
TX-BW	Transmitted Signal Bandwidth
SS	Slow-Slow
UWB	Ultra-wideband
VDL	Variable Delay Line
VGA	Variable Gain Amplifier
VHDL	Very High Speed Digital Language
VHDL-AMS	Very High Speed Digital Language Analog Mixed Signal
WIDI	Wireless Display
WPAN	Wireless Personal Area Network
UMC	United Microelectronics Corporation

1. INTRODUCTION

Ultra wide-band (UWB) technology has been used and developed for well over 50 years. The origins of the technology stem from the work in early 1960s on time-domain electromagnetics, which is a study of electromagnetic-wave propagation as viewed from the time domain, rather than from the more common frequency-domain perspective [2].

UWB technology has a wide range of application areas [3]. Pulse-based wideband and UWB radios are well known for their use in radar technology [4]. Very short pulses in time are sent, received, and processed to identify far-away objects. This method is used in applications such as ground penetrating radar (GPR) [5], through wall imaging [6], and breath detection [7]. UWB technology is also utilized in automotive radar applications including collision detection and auto-drive systems [8]. Utilization of short pulses also helps UWB to achieve battery-less operation. UWB is the key method for wireless sensor networks [9], because of its ultra-low power consumption property. It is employed in remotely powered biomedical circuits operating in the 0-960 MHz band [10].

UWB has also been popular for its use in high data rate applications in recent years [11]. Consumers always demand high definition (HD) content. Therefore, the data rate requirements keep on increasing with the customer needs. For instance, three-dimensional HD (3D-HD) format started to dominate the blue-ray market. Ethernet cables are supporting multi gigabits per second data transfer rates. High definition multimedia interface (HDMI) cables already have support for 5 Gbps data rate. In parallel to these new technologies, HD wireless streaming is also in demand. Even battery operated devices use HD content. UWB technology already plays an important role for short range wireless personal area networks (WPAN). Commercial products such as wireless screen share, Intel' wireless display (WIDI), wireless-usb hub

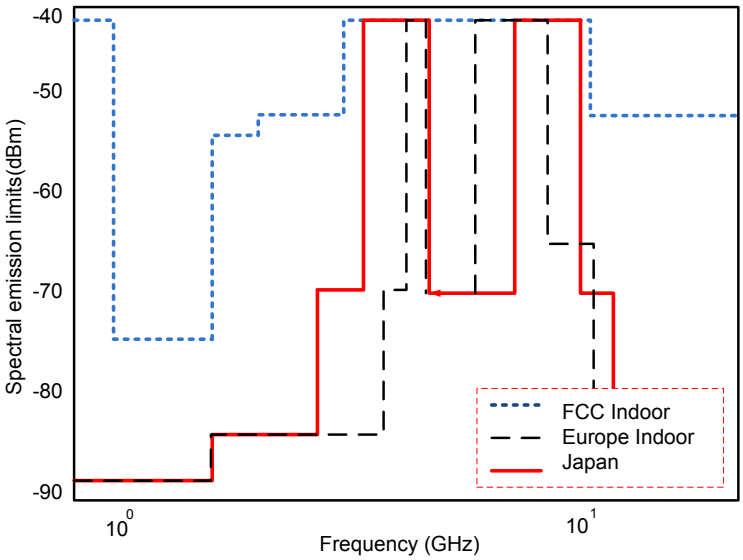

Figure 1.1. UWB Spectrum Limits.

are all utilize the UWB technology.

The communication range is in the order of a few meters for high data rate communication, because of strict spectral mask requirements. The 3.1-10.6 GHz frequency band with -41.3 dBm/MHz spectral limitation as shown in Figure 1.1 was allocated for the unlicensed ultra-wideband technologies by the U.S. Federal Communications Commission (FCC) in 2002 [12]. Any wireless communication technology that produces signals with a bandwidth wider than 500 MHz or a fractional bandwidth greater than 0.2 is considered as UWB.

UWB is an unlicensed technology, which coexists with other licensed and unlicensed narrowband systems. As mentioned above, because of the strict power requirements, UWB can only be allowed to coexist with other technologies under very strict power constraints. In spite of all these strict rules, UWB offers attractive solutions for WPAN, wireless telemetry, tele-medicine, and wireless sensor networks. UWB systems are also able to provide much higher capacity than the current short-range narrowband systems.

UWB systems provide the possibility of using an extremely wide and unlicensed frequency spectrum. Using UWB with other technologies on the same frequency inter-

val greatly increases spectral efficiency. UWB also offers great flexibility of spectrum usage. These transceivers can also be used for optimizing systems performance as a function of the required data rate, range, power, quality of service, and user preference.

The high temporal resolution of UWB signals results in low fading margins, implying robustness against multipath fading. Excellent time resolution property of UWB systems and multipath resistance leads to more accurate ranging applications. Extremely short duration pulses allow centimetre ranging [13].

The key benefits of UWB systems can be written as:

- Radar operation; accurate ranging, real-time through-wall imaging, and movement detection,
- Low power applications; wireless sensor networks, telemetry, and radio-frequency identification (RFID) [14],
- High data rate communication,
- Low interference and immunity to multipath propagation.

On the other hand, some key challenges of UWB system design can be given as;

- Pulse and spectrum shaping spectrum of transmitted signals,
- Wideband RF front-end and antenna design,
- Accurate synchronization and channel parameter estimation,
- High sampling rate for baseband digital implementations,
- Detection of ultra-low energy signals under noisy environment,
- Multiple access and multi-user interference.

1.1. Literature Survey and Objectives

There are mainly two methods in realizing UWB systems in the literature. These methods employ impulse radio UWB (IR-UWB) and multi-band orthogonal frequency division multiplexing (MB-OFDM) techniques. This thesis focuses on the IR-UWB

technique. In IR-UWB, very narrow pulses are utilized. These pulses occupy a very large spectrum in the frequency domain, even if there is no modulation associated with the pulses. This behaviour reduces the possibility of interference [12]. Narrow UWB pulses give high resolution precise position information capabilities by using time of arrival and angle of arrival techniques [15, 16].

UWB radio transmission uses very low power and spread spectrum techniques for multi-user communication. These methods can be categorized as time hopping (TH) and direct sequence (DS) [17]. The performance of these methods depends on the multipath interference. The design of the receiver system architectures play an important role on the performance under multipath interference [18]. Multipath fading channel can be modeled as in [19–23].

The channel model is created using measurements in various locations by IEEE 802.15.3a channel modeling sub-committee and this model depends on the Saleh Valenzuela (S-V) channel model [24]. However, impulsive noise is ignored in these models. The presence of impulsive noise in various locations (house, bus stops, computer laboratories, hospital) has been shown using measurements at very high frequencies [25]. The receiver operation must be robust to these unpredictable noise bursts. Therefore, impulsive noise must be taken into account in the design phase of the receiver.

On the other hand, the modulation method has to be decided in the selection of the receiver architecture. Pulse amplitude modulation (PAM), pulse position modulation (PPM), on-off keying (OOK), binary phase shift key (BPSK), and orthogonal pulse modulation (OPM) are commonly utilized modulation schemes in IR-UWB transceivers. OPM is generated with different Gaussian pulses and it has a large hardware complexity. Thus, it is rarely used. PAM method has very low immunity to noise and hence is not preferred. BPSK [26–32], PPM [33–35], and OOK [36–39] are the modulation schemes mostly employed in the literature [40, 41]. BPSK has very high noise immunity and synchronization is easier compared to PPM. However, the circuit design for phase modulated signals is complex and brings additional hardware costs. OOK is widely used in the literature because of its circuit simplicity compared to the

other methods.

IR-UWB receivers can be implemented by either coherent or non-coherent architectures [42, 43]. Coherent architectures are commonly used in UWB transceiver systems. Rake type receiver was one of the first methods utilized in UWB systems [44]. However, rake receivers require many parallel branches of the same receiver scheme to find the right multipath component. The increased number of branches in a rake receiver results in high power consumption. Another coherent receiver type is the correlated receiver [45]. In correlated receivers, the received signal is initially multiplied with a template signal, then it is integrated and compared with a DC reference to obtain digital data. Transmitted reference method is a type of correlated receiver which does not use a template signal. Instead, the delayed version of the incoming signal is multiplied by itself. These two methods are effective, but they have some important challenges in the design such as the requirement of overlap in the template and the incoming signal. The same problem exists in the transmitted reference method. On the other hand, energy detection method is the most common scheme in non-coherent receivers. The realization is much easier compared to coherent systems. However, there is no information about the received signal. Thus, it is called blind synchronization. Therefore, the design of the synchronizer is the most important part in energy detection receiver [46]. Both coherent and non-coherent methods are challenging and require extensive design time.

Transmitter and receiver blocks must be designed starting from the system level simulations. One can design individual UWB blocks with excellent specifications. However, the best transceiver performance is not necessarily obtained from optimizing these blocks individually. System performance can be enhanced by designing these consecutive UWB blocks by taking system level specifications into account. Once the blocks are connected at the system level, better performance under a given power budget can be achieved by blocks having lower specifications. Therefore, one of the objectives in this thesis is to model the non-idealities of the UWB blocks to observe the effects on the system performance.

Non-idealities are the imperfections of the circuit level representations of the transceiver blocks. The properties of the blocks also affect the system performance and have to be considered in system simulations [47]. These non-idealities and properties are tabulated in Table 1.1.

Table 1.1. Non-idealities and System Blocks Properties.

Pulse Generator	Pulse Order, Bandwidth, Jitter
LNA	S parameters, Matching, Linearity, NF, Q, BW
VGA	Gain, BW, Linearity
Mixer	BW, Leakage, Linearity
Synchronizer	Jitter, Time Resolution
ADC	Quantization levels, Sensitivity

There is a need for system modeling environment for UWB to observe and design the transceiver architecture. Very high speed hardware description language analog mixed signal (VHDL-AMS) environment is selected for system modelling in this thesis. VHDL-AMS enables simulations of behaviourally described blocks and circuit netlists simultaneously. In this architecture, low noise amplifier (LNA), variable gain amplifier (VGA), squarer, integrate and dump (I&D) and analog to digital converter (ADC) blocks can be described as analog and mixed signal blocks as depicted in Figure 1.2. Synchronization, noise estimation, demodulation, and gain control units are to be designed nearly digital or purely digital. At the transmitter side, the PPM and OOK are pure digital, whereas the pulse generator (PG) and power amplifier (PA) are the analog blocks.

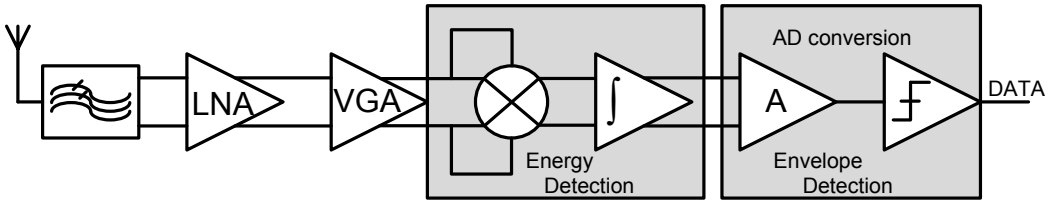

Figure 1.2. Energy Detection IR-UWB receiver.

On the transmitter side, the pulse shaper could be chosen to have 5th order of Gaussian mono-cycle, which best fits to the FCC spectrum from 3.1 to 10.6 GHz [48]. However, designing hardware with 7 GHz bandwidth especially at the receiver side is a complex and power consuming task. Therefore, it is better to use higher order derivatives with wider pulse widths in order to achieve a smaller band between 3 GHz and 5 GHz. The complexity is exchanged with bit rate.

The objective is to connect these blocks at the system level, make non-ideal model simulations, and derive the system specifications together with the effects of the non-idealities on the system performance. Another goal of the thesis is to make the system robust to impulsive noise. The field measurements and fitted noise models match the condition of impulsive noise in different environments [25]. It has been shown that impulsive noise can be observed even at high frequencies. Additive White Gaussian Noise (AWGN) noise model does not hold at impulsive noise environments [25]. Although multipath effects have been considered in UWB systems, nature of the noise and its effect on the UWB system has been ignored. Therefore, effect of impulsive noise over the channel must be considered while designing communication hardware for broad-band wireless systems like UWB.

Impulsive noise consists of sudden step like transitions with large amplitudes. There have been studies on removing the effect of impulsive noise in IR-UWB rake receiver type receiver architecture by introducing zero order hold block before combining the rake paths. The robust rake receiver can eliminate the effect of impulsive noise by removing the large-amplitude outliers at the outputs of the matched filters employed by the conventional rake receiver at each of its fingers, which is followed with the usual maximal ratio combining (MRC) [49].

Middleton's class-A noise model approximation which is called mixture model can be used for representing the impulsive noise in channel simulations. The mixture model consists of an infinite expansion of Gaussian density functions with different variances and identical means.The first two terms of the expansion sufficiently describe the class-A noise pdf. In addition, the mixture model is much more tractable than the

class-A noise probability density function (PDF) [50].

If the impulsive noise occurs at an undesired location, then it will be integrated. Since its value is high, it will change the received signal. Therefore, an error will be introduced. Since the impulsive noise has a very high bandwidth, on chip band pass filter (BPF) can be used prior to the LNA block to limit the amplitude of the impulsive noise. To further eliminate the impulsive noise, the level of the integrated signal can be checked without altering the system architecture. If the signal level is much higher than the expected maximum value, then the decision mechanism can ignore that signal by treating it as a noise and can check the other PPM bit location. The comparison of just one PPM location with the threshold will give a correct result. The same method can be applied to OOK as well. The performance of the system will be reduced slightly in the case of threshold comparison. However, the error that will be introduced by the impulsive noise will be eliminated. In the case of high density of impulsive noise environment, the BER will be close to the BER graph of threshold comparison. In the non-impulsive noise environment the results will be a few dB better. Robust energy detection IR-UWB receiver can be achieved without introducing additional hardware costs.

This architecture is a promising one for IR-UWB system with low hardware complexity and has potential for robustness without additional hardware. Another objective of this thesis to construct an UWB transceiver that is robust to impulsive noise. Synchronization errors could be introduced in the circuit level simulations. These errors can be lowered by taking a larger time window for integration. A larger time window brings higher BER because of the channel noise. There is a trade-of between BER and synchronization. These decisions can automatically be made by the receiver according to channel noise present in the system. Therefore, the overall performance can be increased.

1.2. Contributions and Organization of the Dissertation

In this thesis, OOK modulation scheme is selected for the transceiver designs due to its hardware simplicity. Both coherent and non-coherent IR-UWB transceivers are realized in 130 nm CMOS technology. An ultra-low power dual-band transmitter is designed with wide channel separation. The dual-band transmitter can operate both in 0-960 MHz and 3.1-5 GHz bands with reconfiguration of the off-chip passive elements. A fully configurable transmitter design is realized that is robust to manufacturing process variations. The mono-cycle pulse width and shape is digitally configured to obtain the desired center frequency and bandwidth. The non-coherent receiver employs clock-less reception using envelope detection at 240 Mbps. Impulsive noise aware design is achieved by LNA input matching BPF. The BPF also serves as a clipper to reduce the introduced impulsive noise. The coherent design is based on the template receiver. Therefore, timing is an essential parameter, necessitating careful consideration of the effect of jitter. A very high speed, low jitter, and high resolution Vernier delay line design is completed. During the thesis, three chips were fabricated using UMC 130 MMRF technology. The details of the fabricated ICs are given in Table 1.2. Coplanar wave guide FR4 printed circuit boards (PCB) and UWB antenna designs were made to minimize the coupling problems and have correct measurements.

Table 1.2. Manufactured ICs.

ICs	**Transmitter**	**Receiver**	**Additional Blocks**
1	Dual-band design	Non-coherent design	Buffer
2	x	2nd Non-coherent design	Pulse generator
3	Reconfigurable design	Coherent design	Vernier Delay Line, Envelope detector, Self Correlator, High frequency sampler

Full-custom designed and realized transceiver blocks of the integrated circuits

(IC) can be listed as;

- Ultra-low power dual-band IR-UWB transmitter,
- Ultra-low power reconfigurable IR-UWB transmitter (Shift register for reconfigurability),
- 240 Mbps non-coherent IR-UWB receiver (LNA, VGA, self mixer, integrator, baseband VGA, hysteresis comparator),
- Coherent IR-UWB receiver (LNA, VGA, mixer, active balun, delay line, template pulse generator, baseband VGA, 12 level ADC),
- 800 MHz linear and low jitter shunt capacitor Vernier delay line.,
- 1 GHz 5 bit Up/Down counter with asynchronous reset and enable,
- High frequency sampling based non-coherent correlation OOK demodulator,
- Envelope detector using unbalanced inverter,
- Self-correlation based non-coherent OOK demodulator.

The contributions of this thesis are as follows;

Existence of impulsive noise in broad-band and UWB wireless communication channels are proven with impulsive noise measurements and models. In Chapter 2, impulsive noise measurements and system models are explained in detail.

It is followed by system level models of UWB systems in Chapter 3. There was an absence of an computer automated simulation environment for top-down design of transceivers for multi-band and impulse radio UWB systems. MATLAB and VHDL co-simulation environment is constructed for synthesizable MB-OFDM UWB transceiver architecture. MATLAB and VHDL-AMS co-simulation environment is also created for top-down design of IR-UWB transceiver. The high level models are written in VHDL-AMS. Computer aided automation (CAD) tool is prepared by crating a link MATLAB and VHDL-AMS using dedicated scripts. Analysis and simulation of circuit level non-idealities are performed with the proposed CAD tool. Then, the effects of the non-idealities on system performance are studied in terms of BER figure.

VLSI designs of the ultra-low power transmitters are explained in Chapter 4. An all-digital ultra-low power dual-band IR-UWB transmitter is designed and tested. Then, a configurable version of the all-digital transmitter that has better power consumption performance is designed.

In Chapter 5, the receiver architecture designs and measurement results are discussed. 240 Mbps low-power non-coherent energy and envelope detection IR-UWB receiver design is successfully tested. Synchronization free non-coherent demodulation methods are proposed. A low power template based coherent IR-UWB receiver architecture is designed and implemented. A linear and low jitter Vernier delay line for template synchronization based on shunt capacitor technique is designed.

Antenna and PCB designs and measurements are given in Chapter 6. Tests of 3 wireless mixed signal RF UWB chips in 130 nm CMOS technology are completed with patch antenna and PCB designs using coplanar wave-guide technique.

Chapter 7 provides performance comparisons and details about commercial UWB development boards. Several measurements and comparisons have been made to observe the data rate and reception quality.

The thesis is concluded with final remarks and discussion on future works in Chapter 8.

2. MEASUREMENTS AND MODELING OF IMPULSIVE NOISE IN BROADBAND COMMUNICATION CHANNELS

2.1. Introduction

In the previous wideband and UWB transceiver designs in the literature, the transmission channel has always been assumed to have AWGN behaviour. Effect of impulsive noise has been ignored for UWB systems. The traditional approach considers just the thermal noise, which is modelled as a stationary and memoryless Gaussian random process, that does not agree with relevant field measurements. It has been reported in the indoor measurements [50] that there is a performance degradation seen, when the UWB system is subject to the impulsive noise produced by the office machines such as printers, fax machines and photocopiers.

Impulsive noise consists of sudden step-like transitions between two or more levels (non-Gaussian), as high as several hundred microvolts, at random and unpredictable times. Electrical and mechanical machinery can produce non-Gaussian impulsive noise bursts in wireless receivers. Effects of impulsive noise can be seen in populated metropolitan areas. Devices with high voltages such as ignition motors, microwave ovens, hair dryers, blenders, photocopiers and printers are significant sources of impulsive noise in office and retail environments. In crowded cities, impulsive noise is most probably caused by the large number of vehicles older than 10 years and also due to the electromagnetic noise generated by industrial equipment and household appliances [51–53].

Our aim in this chapter is to characterise and present the impulsive behaviour of the wideband and UWB communication channels. In this thesis, taking into account impulsive noise and interference, Middleton's Class-A mathematical noise models are constructed from the electromagnetic field (EMF) measurements. By presenting the

Figure 2.1. Rohde and Schwarz FSH-6 EMF measurement device.

channel which has impulsive behaviour even at higher frequencies, we can design a new wideband transceiver which can work under impulsive noisy and interfering communication channels as well as AWGN. This chapter aims to show the importance of impulsive noise aware design of UWB system. Noise measurements are taken with the portable spectrum analyser as shown in Figure 2.1 at various indoor and outdoor locations to show the presence of impulsive noise. The spectrum analyser (Rohde-Schwarz

FSH6) with tri-axis isotropic antenna is capable of taking measurements from 100 kHz to 3 GHz. These measurements are modelled with Middleton's Class-A noise model. The results fit quite well to the mathematical models.

2.2. Impulsive Noise Measurements

EMF measurements have been taken in indoor and outdoor locations to observe the noise at different frequencies. These locations are presented in Table 2.1 with their respective total field strength over the range 100 kHz to 3 GHz. At the hospital, measurements were taken at the technical room of the MR service. Computer lab of the university was used to measure the noise. For the measurements in the house, blenders, exhauster and other household devices were used. At the bus terminal, vehicle ignition noise was considered. Noise of the electronic devices are measured at the TV/Radio towers. In the following section, detailed results are provided.

Table 2.1. Field Measurements.

Locations	**Field Strength (V/m)**
HOSPITAL	0.8796
MEMS LAB	0.8808
COMPUTER LAB	0.9384
HOUSE	0.9475
HOUSE 2	0.9483
BUS TERMINAL	1.6032
TV/RADIO TOWERS	4.1227
TV/RADIO TOWERS 2	7.2493
TV/RADIO TOWERS 3	12.1032

2.2.1. Measurements

Locations where impulsive noise dominates are as follows;

2.2.1.1. House. Two measurements were taken. At the first measurement all household devices were left working. Blender, exhauster, vacuum cleaner, and dishwasher were used while taking the measurements. In the second measurement, switching activity of exhauster only was recorded. In Figure 2.2, the measurement at the house environment was taken between 900 MHz and 1 GHz frequency band. Note that there is also a the GSM signal at around 950 MHz. It can be seen that GSM signal is affected by the impulsive noise.

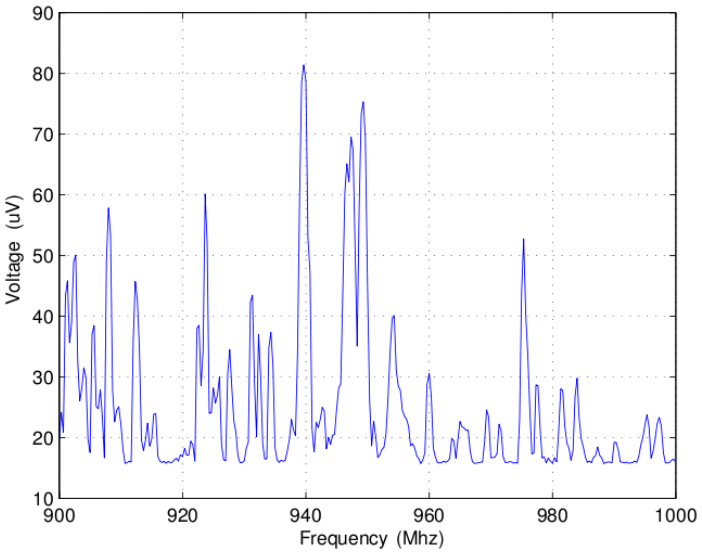

Figure 2.2. Indoor EMF measurement taken in the presence of household appliances.

2.2.1.2. Bus Terminal. Measurements were taken at a crowded bus terminal. Vehicles in the terminal were very old. Therefore, vehicle ignition noise was dominating as impulsive noise. In Figure 2.3, the ignition noise can be observed around 1.4 GHz. Vehicle ignition noise is also present at lower frequencies.

2.2.1.3. Computer Lab. Measurements were taken at the computer lab with 17 computers. A task was given to the computers to run them at full speed. Measurements do not show big noise impulses and it is very hard to detect them. The results are shown in Figure 2.4 at between 1.8 GHz and 1.9 GHz range. It can be seen that small impulsive noise can be detected near the GSM signal.

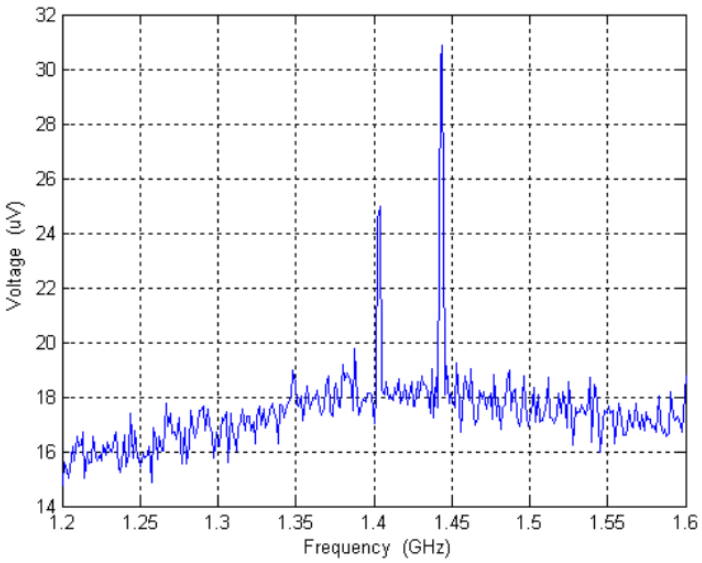

Figure 2.3. Outdoor EMF measurement taken at a bus terminal.

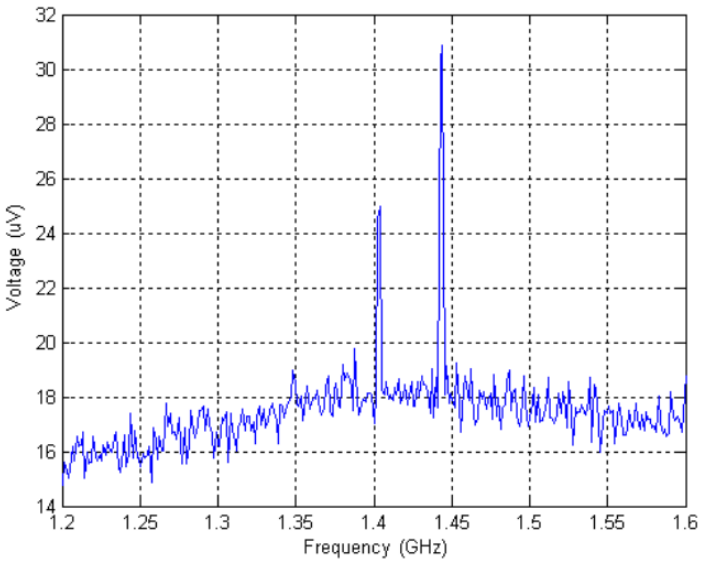

Figure 2.4. Indoor EMF measurement taken at a computer lab.

2.2.1.4. TV/RADIO broadcasting towers. TV/Radio tower measurements were taken at three different locations. Measurements in Figure 2.5 were taken at the TV/Radio towers. TV broadcasting signal and GSM signals dominate but it can be observed from Figure 2.5 that small impulses above the noise floor are also present. Since the other signals are very strong, impulsive noise appears to be small.

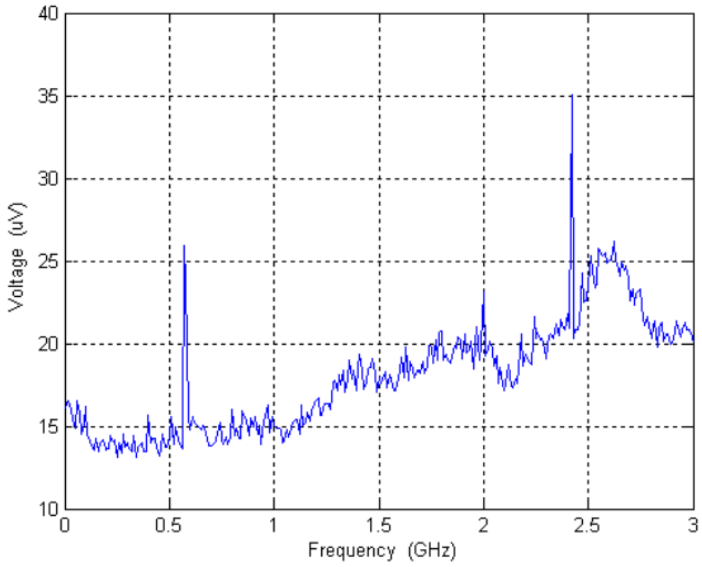

Figure 2.5. Indoor EMF measurement taken at a TV broadcast tower.

2.3. Impulsive Noise Model

Noise and distortion are the main limiting factors in communication and measurement systems. Therefore, the modelling and removal of the effects of noise and distortion have been at the core of the theory and practice of communications and signal processing [54]. Middleton's Class-A noise model is a well known statistical-physical model for man-made impulsive radio noise [55, 56]. The model is constructed from Gaussian mixtures with different variances and means. Therefore, the Gaussian mixture fits well to the impulsive noise shape. On the other hand, AWGN does not well represent the communication channel, because the impulse bursts can happen anywhere at any time. From the measurements, it can be observed that the impulsive noise has been found at high frequencies. Middleton's Class-A noise model is given as

$$p\left(x\right) = \exp\left(-A\right) \sum_{0}^{\infty} \frac{A^m}{m! \sqrt{2\pi\sigma_m^2}} \exp\left(-\frac{x^2}{2\sigma_m^2}\right), \tag{2.1}$$

where

$$\sigma_m^2 = \frac{m/A + \Gamma'}{1 + \Gamma'}. \tag{2.2}$$

In Equation 2.2 , $\Gamma^{'}$ is defined as the ratio of the Gaussian component of noise power to the non-Gaussian component of the noise power, such that

$$\Gamma' = \frac{2e_2\left(e_6 + 12e_2^3 - 9e_2e_4\right)}{3\left(e_4 - 2e_2^2\right)^2} - 1. \tag{2.3}$$

In the model equations, A shows the impulsive behaviour of the model. Impulsiveness increases with the parameter A, i.e.,

$$A = \frac{\left(9e_4 + 2e_2^2\right)}{2\left(e_6 + 12e_2^3 - 9e_2e_4\right)^2}. \tag{2.4}$$

By using these two parameters, class-A noise model for a given system is constructed. In class-A impulsive noise model, the impulsiveness of the noise is characterized by these two parameters [56]. These parameters can be estimated by finding the envelope of the measured noise. From the envelope, second, fourth and sixth order of moments are calculated and the parameters are found, as follows

$$\begin{aligned} e_2 &= E\left[\varepsilon^2\right], \\ e_4 &= E\left[\varepsilon^4\right], \\ e_6 &= E\left[\varepsilon^6\right], \end{aligned} \tag{2.5}$$

where ε represents the experimentally measured envelope of interference [56]. To compare the impulsive noise and its model, the amplitude probability distribution (APD) is used. APD is defined as the probability that noise power exceeds a defined noise level [57]. In the case of impulsive noise, this level is the background noise. Figures 2.2-2.5 show the indoor and outdoor EMF measurement results. Figures 2.6-2.9 show the respective APD results and Middleton's Class-A noise model. It can be seen that measurement results are in good agreement with the class-A impulsive noise model.

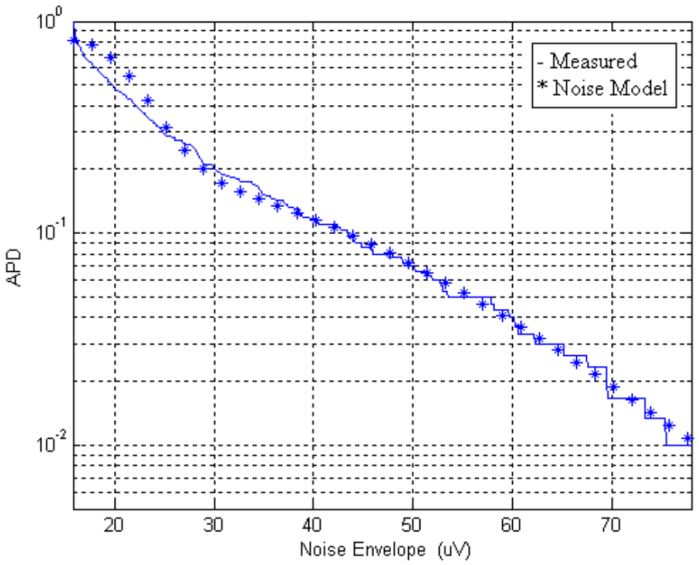

Figure 2.6. APD of Figure 2.2 and noise model fit.

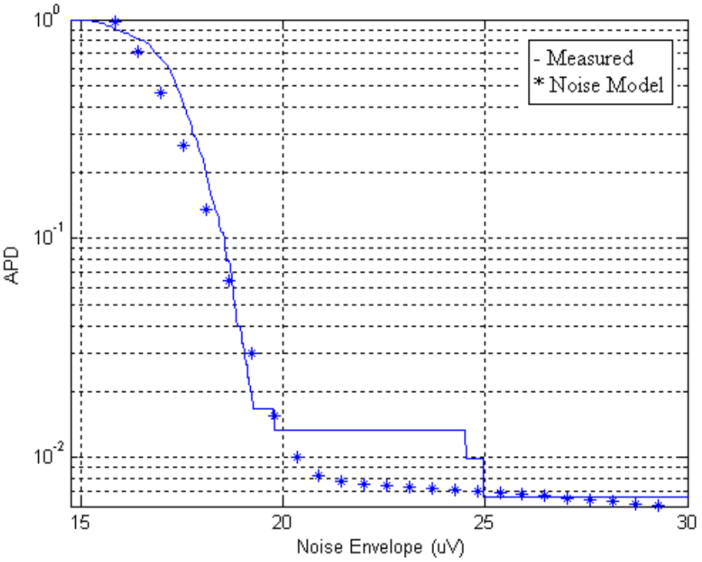

Figure 2.7. APD of Figure 2.3 and noise model fit.

2.4. Conclusion

This chapter gives the analysis and measurements of impulsive noise for a wide band frequency band between 100 kHz and 3 GHz. Indoor and outdoor EMF measurements are taken and Middleton's Class-A noise models are constructed. Class-A

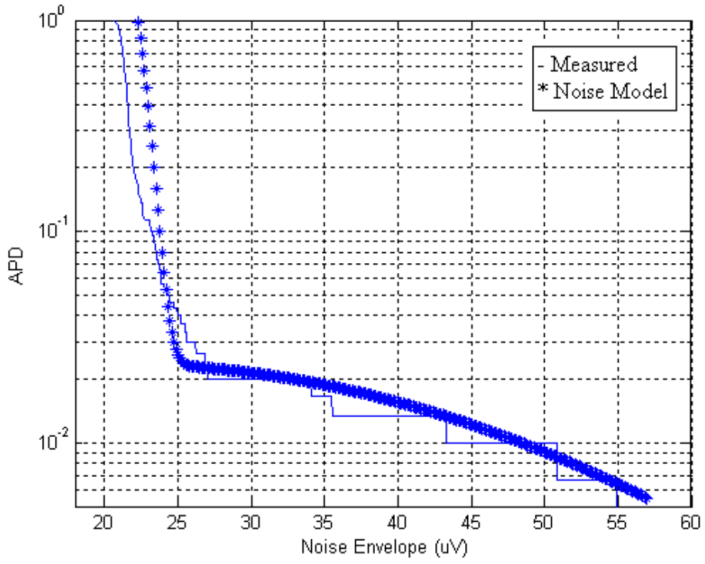

Figure 2.8. APD of Figure 2.4 and noise model fit.

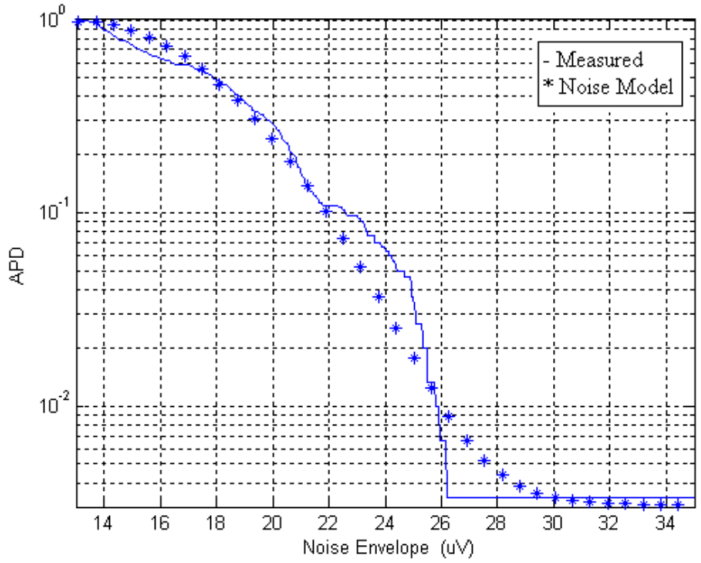

Figure 2.9. APD of Figure 2.5 and noise model fit.

mathematical models and measurement results are in good correspondence. Middleton's Gaussian Mixture model better represents the channel behaviour. It has been shown with the extensive noise measurements and models that the effect of impulsive noise over the channel must be considered, while designing a communication hardware for broad-band wireless systems.

3. UWB SYSTEM MODELING WITH MATLAB AND VHDL-AMS

3.1. Introduction

This chapter focuses on the system level modelling and simulations of both IR and MB-OFDM transceiver architectures. This thesis work is based on the IR-UWB transceivers. However, MB-OFDM architecture was also studied to observe the performances of both systems from a wider perspective and to have a sense on differences between continuous time and pulse based transceiver systems in terms of performance and complexity.

The choice of modelling approaches differ for MB-OFDM and IR-UWB systems. MB-OFDM transceiver system models are built on very high level computer automated MATLAB scripts. The circuit design for the MB-OFDM is not the focus of the thesis. On the other hand, in the IR-UWB based transceiver architecture, the system model is based more on circuit parameters such as gain, linearity, and reflection coefficient.

The main parameter that defines the system performance is BER. The effect of non-idealities and their effects on the system's BER performance is studied for IR-UWB transceiver. But, in the MB-OFDM transceiver design, the system is automatically constructed with user supplied parameters such as FIR filter size, convolution encoder length, and Viterbi decoder complexity. After that, the system performance is measured with these parameters.

Previous studies on UWB system modeling and simulations have been generally performed in MATLAB and SIMULINK. A 200 Mbps fixed point MB-OFDM UWB SIMULINK simulation platform was presented in [58]. Performance differences between floating point and fixed point MATLAB baseband modeling of UWB was discussed in detail in [59].

VHDL is the generic modeling language for communication systems, since they are easily synthesizable to digital hardware with decreasing cost and increasing computational power. FPGAs have become viable alternatives to implementation or rapid prototyping of communication systems. Their flexibility is a major advantage for reconfigurable hardware. ASIC implementations offer higher performance at the cost of reduced flexibility. It should be noted that the same VHDL code can be synthesized on an FPGA or on an ASIC without much difficulty.

A previous study demonstrates a baseband MB-OFDM transmitter [60], which is synthesized on FPGA. FFT system block involves critical multiplication operations. An OFDM module [61] in the literature mainly focuses on the FFT design for MB-OFDM receiver. On the other hand, writing a synthesizable VHDL model for a complex system is a daunting task, because such a model has to be written mostly at the register transfer level (RTL) for good synthesis results.

In this work, MATLAB is used for top level design. However, system models are constructed using VHDL-AMS. In MB-OFDM method, the MATLAB scripts generate the VHDL-AMS codes and test-benches automatically by user supplied parameters. Simulation is performed using VHDL-AMS simulator. Then, the results are automatically read by the MATLAB script and the performance results are displayed. On the other hand, in IR-UWB, the circuit models are hand written on VHDL-AMS with generic parameters that can be changed at the top-level MATLAB code. Since, the top level control is performed by MATLAB scripts, VHDL-AMS simulator works at the background when it is required. The advantage of VHDL-AMS is that these codes can be replaced by real circuitry during the design.

The following sections give details on the designed automation tools, system models, effects of system and circuit parameters on system performance with simulations for both UWB receiver systems.

3.2. Design of Synthesizable Digital MB-OFDM UWB Blocks

The design enviroment is divided into two phases. In phase I, MATLAB scripts create the VHDL model and test benches of MB-OFDM transmitter and receiver with desired parameters. In phase II, the MATLAB script calls the MODELSIM simulator to simulate the VHDL model. After that, the results are fed back into MATLAB in an automated fashion for comparison with MATLAB model simulations and plotting purposes. All UWB blocks are designed to be easily configurable with VHDL input parameters which are entered into MATLAB scripts [62]. Since all of the work is performed automatically, the effect of changing a system or a block parameter can be quickly observed. The designer does not need to redesign the required block again because the block and the overall system is automatically recreated with the new parameters.

MATLAB and VHDL are used together to obtain the automation flow described in Figure 3.1. In this figure, square shaped shaded boxes represent the MODELSIM VHDL simulator. Square shaped boxes without shading represent the VHDL model and test bench files that are generated by the MATLAB scripts. Finally, the elliptically shaped boxes are used for the MATLAB environment where channel model is defined, scripts generating the VHDL models for the receiver and transmitter as well as test benches. Transmitter and receiver blocks are simulated in MODELSIM. The wireless channel model is simulated on MATLAB. The exchange of information between two simulators is achieved without user interaction by dedicated scripts. Detailed explanation of the design flow is given in the following subsections.

3.2.1. VHDL Model Generation

A MATLAB model is developed prior to design of VHDL models. This model is verified by extensive simulations. The aim is to use the results of the MATLAB model as reference for evaluating the results of the hardware models to be developed later. The difficulty of generating efficient synthesizable VHDL code for complex systems was mentioned earlier. This complexity is compounded by the need to evaluate several

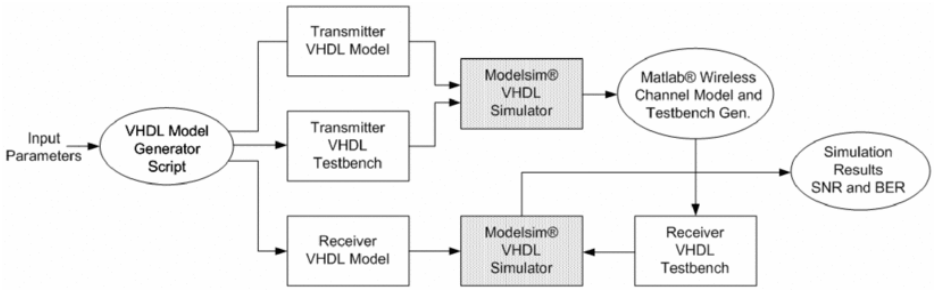

Figure 3.1. MATLAB - VHDL design flow.

alternatives and/or parameter values during the design. Thus, automation in creating VHDL codes is explored. In this study, a series of MATLAB scripts are written which generate synthesizable VHDL models of UWB blocks. Depending on various design parameters such as the size of an FFT block, the appropriate VHDL code is output from the VHDL model creator script. VHDL models for all of the blocks are thus created. A VHDL model by itself is not sufficient for simulation and verification. Test inputs have to be provided to the VHDL model in a specific format called test bench. There are also MATLAB scripts creating these test benches. An additional MATLAB script is also included to combine all blocks at the top level.

3.2.2. MATLAB- VHDL Co-Design

The outputs obtained from the transmitter simulation are converted to a MATLAB file and introduced to a wireless channel model which is implemented again in MATLAB. Since the channel is not a part of the transceiver, a VHDL code for the channel is not targeted. After the channel simulations, the outputs are converted back into testbench format and fed to the receiver. Again, the receiver VHDL model is simulated with the provided testbenches on MODELSIM. The results of the receiver simulation are interpreted by MATLAB for BER and signal to noise ratio (SNR) calculations. It should be noted that transmitter and receiver MATLAB models have also been developed and transmitter-channel-receiver series is simulated on MATLAB simultaneously with the VHDL simulations. Hence, any discrepancy between these two sets of models is easily observable. Also note that all VHDL codes generated by

the proposed system are synthesizable. Consequently, the proposed design flow and system with the associated commercial tools (MODELSIM and PRECISION) form a complete design environment.

3.2.3. Implemented Communication System Blocks

Communication system blocks which are both synthesizable and reconfigurable with desired parameters are given in Figure 3.2. The wireless channel model is simulated in MATLAB and the obtained results are converted to test-benches for receiver VHDL simulations.

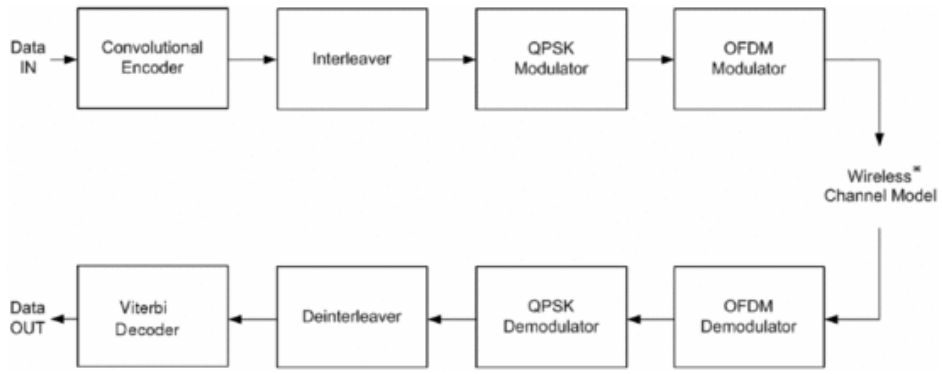

Figure 3.2. Reconfigurable system blocks.

The MATLAB codes generating the convolutional encoder, Viterbi decoder, interleaver, and de-interleaver blocks were designed to obtain the VHDL output with Boolean arithmetic. The remaining modulator and demodulator blocks are designed using the complex arithmetic package which is created again by the MATLAB scripts. Especially OFDM requires complex arithmetic package because of the IFFT and FFT components which establish the orthogonality. Complex arithmetic package is written using floatfix library which is a part of the proposed IEEE VHDL-200x packages. Therefore the VHDL model of the MB-OFDM is fixed point. Resolution of the fixed point system can be adjusted by an input parameter provided by the user to the MATLAB scripts.

3.2.3.1. Convolutional Encoder and Viterbi Decoder. The designed convolutional encoder is configurable between the 1/2 and 1/3 modes. Constraint length of the encoder is taken to be 3 in order to reduce the complexity of the Viterbi encoder at the receiver side. Convolutional encoder block for the non-recursive 1/3 mode with constraint length 3 is given in Figure 3.3. Serial input to the encoder is converted to 3 bits by using the shift register memory elements. Then, the outputs are combined by using adders, and the 3 bit output is obtained. After that, the encoded symbol information is converted back to serial output data.

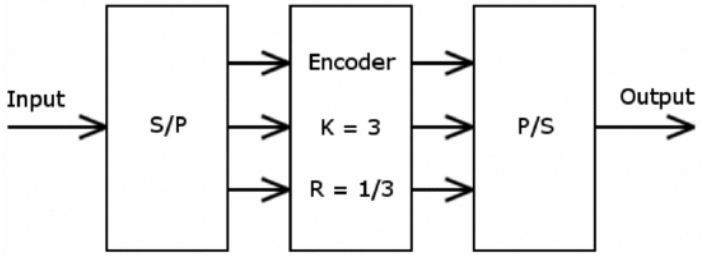

Figure 3.3. Convolutional encoder block diagram.

3.2.3.2. Interleaver/Deinterleaver. Interleaving operation takes place between the symbols and bits within the symbols. Both symbol and tone interleaving have to be performed for high data rate communications. The simplified block diagram for the interleaver block can be observed in Figure 3.4. Buffer stages are needed between the symbol and tone interleaving operations. The resulting data are fed in parallel to the next stage, since the QPSK output will be a parallel input to the IFFT block of the OFDM modulator.

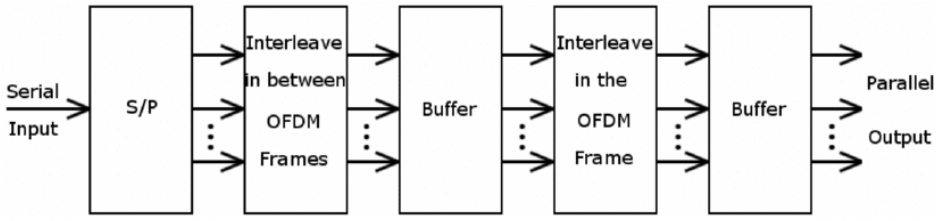

Figure 3.4. Interleaver block diagram.

3.2.3.3. QPSK Modulator/Demodulator. Gray coded Formula shifted QPSK scheme is used for modulation. Several QPSK mappers are used in parallel to increase the performance of the system. QPSK demodulation involves simple comparison demapping. Demapping process is also performed in parallel. QPSK modulator and demodulator block definitions are given in Figure 3.5. QPSK modulator maps N inputs to N/2 outputs and QPSK demodulator demaps N/2 inputs to N outputs as can be observed in Figure 3.5.

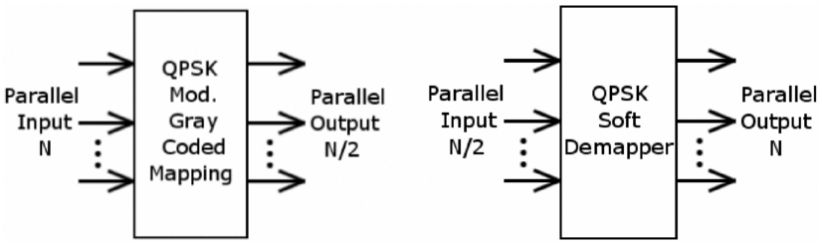

Figure 3.5. QPSK modulator/demodulator block definitions.

3.2.3.4. OFDM Modulator/Demodulator. OFDM modulator and demodulator blocks include FFT/IFFT, cyclic prefix, guard interval, and pilot operations. FFT and IFFT blocks require complex calculations. Since arithmetic package and real numbers cannot be synthesized, a new VHDL complex mathematics package is written for these calculations in order to obtain a synthesizable system. The block diagrams of the modulator and demodulator are given in Figure 3.6 and Figure 3.7. FFT and IFFT operations are implemented by using radix-2 type butterfly operations. The overall OFDM block is also reconfigurable.

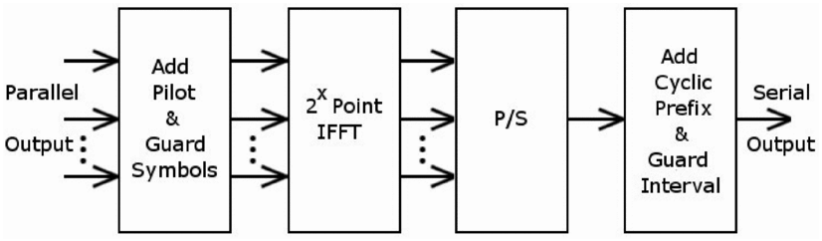

Figure 3.6. OFDM modulator block diagram.

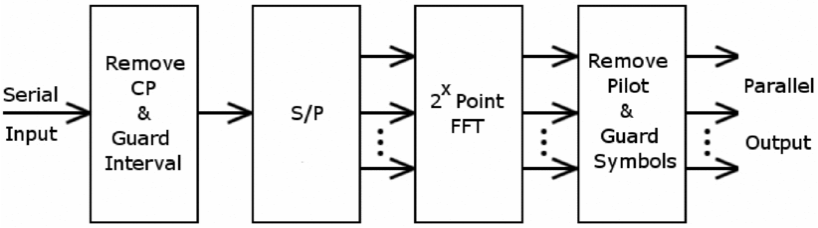

Figure 3.7. OFDM demodulator block diagram.

3.2.4. Simulation Results

SNR vs BER simulations are taken for various input sets. AWGN model has been used in simulations of the wireless channel. UWB VHDL models of the transmitter and receiver blocks are synthesized to an FPGA and results are reported.

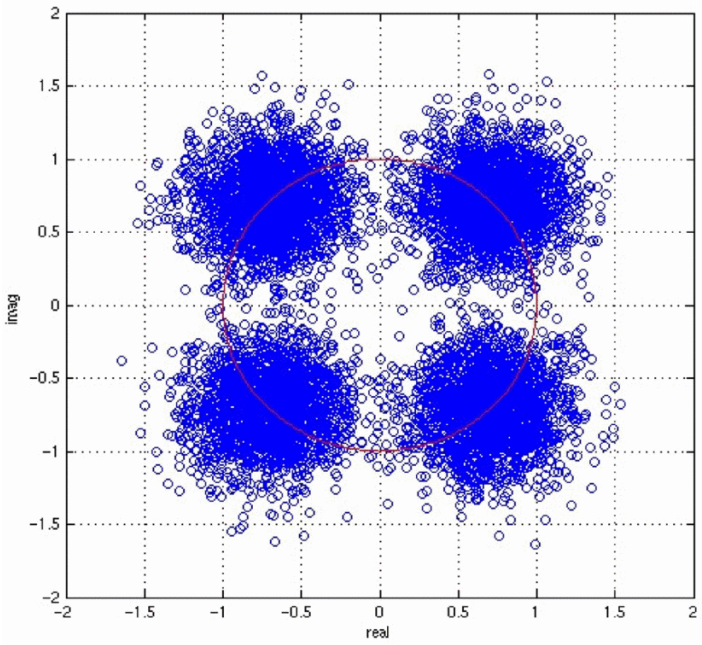

Figure 3.8. QPSK demodulator input at 30 dB SNR.

SNR simulations are taken at the input of the QPSK demodulator to observe the effect of the Viterbi decoder and interleaver processes. The simulations are taken with and without Viterbi decoding and interleaving blocks and gain improvement of about 5 dB has been observed in the simulations. In Figure 3.8, SNR is 30 dB and the

error in the figure seems to be high. However, BER is around $2 * 10^{-6}$ because of the interleaving and Viterbi process blocks.

SNR vs BER simulations are performed under the effect of AWGN channel which is simulated under MATLAB as expained in previous sections. SNR vs BER performance of the overall UWB communication system is given in Figure 3.9.

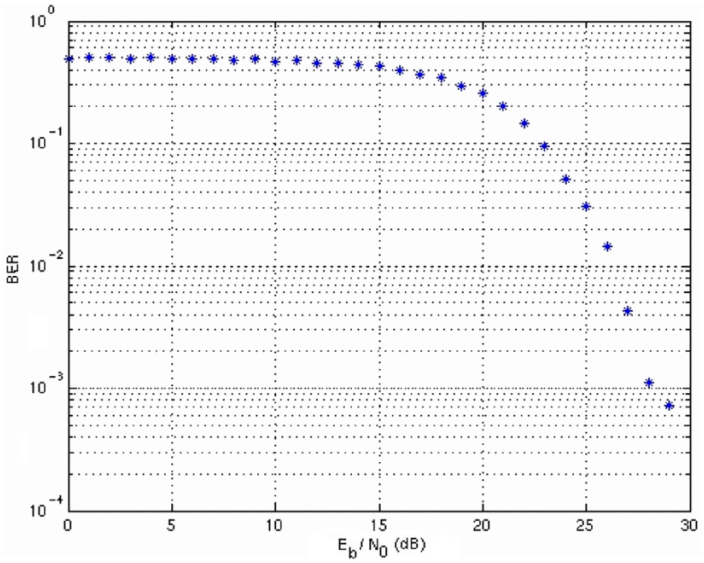

Figure 3.9. BER vs SNR of the overall UWB system.

3.2.5. Sample MATLAB Codes and VHDL Models

VHDL library is written for complex arithmetic operations including addition, subtraction, multiplication, and division as shown in Figure 3.10. In VHDL, synthesizable complex numbers are not available. Therefore, the complex arithmetic package is written by using floatfix-lib. The real numbers are converted to fixed point numbers and then basic complex mathematics operations are performed. FFT and IFFT blocks are scalable with the parameter N which represents the number of points. 128 point FFT and IFFT has been used for the UWB system. As an example, a VHDL model that is generated from the MATLAB script of the single butterfly section, in other words 2-point FFT is given in Figure 3.11. The butterfly operation is computed with twiddle factor in the multiplication and addition steps. Since it is a single stage

```
architecture structure of addition is
  signal tmpc: cmplxres_a;
begin
  tmpc.repart <= a.repart+b.repart;
  tmpc.impart <= a.impart+b.impart;
  c.repart(3 downto -16) <= tmpc.repart(3 downto -16);
  c.impart(3 downto -16) <= tmpc.impart(3 downto -16);
end structure;
architecture structure of subtraction is
  signal tmpc: cmplxres_s;
begin
   tmpc.repart <= a.repart-b.repart;
   tmpc.impart <= a.impart-b.impart;
   c.repart(3 downto -16) <= tmpc.repart(3 downto -16);
   c.impart(3 downto -16) <= tmpc.impart(3 downto -16);
end structure;
architecture structure of multiplication is
  signal tmpc: cmplxres_m;
  signal tmpc1, tmpc2, tmpc4, tmpc5: sfixed(7 downto -32);
  signal tmpc3, tmpc6: sfixed(8 downto -32);
begin
  tmpc1 <= a.repart*b.repart;
  tmpc2 <= a.impart*b.impart;
  tmpc3 <= tmpc1-tmpc2;
  tmpc.repart(3 downto -32) <= tmpc3(3 downto -32);
  c.repart(3 downto -16) <= tmpc.repart(3 downto -16);
  tmpc4 <= a.repart*b.impart;
  tmpc5 <= a.impart*b.repart;
  tmpc6 <= tmpc4+tmpc5;
  tmpc.impart(3 downto -32) <= tmpc6(3 downto -32);
  c.impart(3 downto -16) <= tmpc.impart(3 downto -16);
end structure;
architecture structure of division is
  signal tmpc: cmplxres_d;
  signal numerator, denominator: cmplxres_m;
  signal tmpn1,tmpn2,tmpn4,tmpn5,tmpd1,tmpd2:sfixed(7 downto -32);
  signal tmpn3, tmpn6, denominatortmp: sfixed(8 downto -32);
begin
  tmpn1 <= a.repart*b.repart;
  tmpn2 <= a.impart*b.impart;
  tmpn3 <= tmpn1+tmpn2;
  numerator.repart(3 downto -32) <= tmpn3(3 downto -32);
  tmpn4 <= a.repart*b.impart;
  tmpn5 <= a.impart*b.repart;
  tmpn6 <= tmpn5-tmpn4;
  numerator.impart(3 downto -32) <= tmpn6(3 downto -32);
  tmpd1 <= b.repart*b.repart;
  tmpd2 <= b.impart*b.impart;
  denominatortmp <= tmpd1+tmpd2;
  denominator.repart(4 downto -32) <= denominatortmp(4 downto -32);
  denominator.impart(4 downto -32) <= denominatortmp(4 downto -32);
  tmpc.repart(36 downto -35)
  <= numerator.repart(3 downto -32)/denominator.repart(3 downto -32);
  tmpc.impart(36 downto -35)
  <= numerator.impart(3 downto -32)/denominator.impart(3 downto -32);
  c.repart(3 downto -16) <= tmpc.repart(3 downto -16);
  c.impart(3 downto -16) <= tmpc.impart(3 downto -16);
end structure;
```

Figure 3.10. VHDL complex mathematics package.

butterfly operation, computation is simple.

MATLAB script for the IFFT core VHDL model generation is given in Figure 3.12. Number of stages are calculated from the number of points N which is entered as a parameter to the script. Twiddle factors are computed in MATLAB and entered as constant to the VHDL model. A loop runs and outputs VHDL codes to a VHDL model

```
architecture structure of FFT is
component addition is
  port(a,b: in cmplx; c: out cmplx);
end component addition;
component subtraction is
  port(a,b: in cmplx; c: out cmplx);
end component subtraction;
component multiplication is
  port(a,b: in cmplx; c: out cmplx);
end component multiplication;
signal temp1_1,temp1_2,tempmul1_1: cmplx;
signal tempmul1_2, W1_1, W1_2: cmplx;
begin
-- Buneman's Bit Reversal Algorithm
temp1_1 <= input(1); temp1_2 <= input(2);
-- Stage1 Begins
 W1_1.repart <= to_sfixed(1,3,-16);
 W1_1.impart <= to_sfixed(0,3,-16);
label1_1:
component multiplication
 port map (a => W1_1, b=>temp1_2, c=>tempmul1_1);
label1_2:
component addition
 port map (a=>temp1_1, b=>tempmul1_1, c=>output(1));
label1_3:
component subtraction
 port map (a=>temp1_1, b=>tempmul1_1, c=>output(2));
end architecture structure;
```

Figure 3.11. FFT VHDL model of single butterfly section.

file for each stage. User modification is not required for the generated VHDL model. The VHDL model is created by just one parameter that is the number of points in IFFT. Furthermore, it is important to remember that these generated VHDL models are synthesizable.

3.3. Design of IR-UWB Transceiver System with VHDL-AMS

The IR-UWB transceiver system specifications and performance metrics are determined by top level behavioural system macro-models that are created on VHDL-AMS and MATLAB. The system simulations also include UWB multipath channel models and impulsive noise models [55]. System level simulations are performed using the developed macro-models. Circuit performance metrics are determined by the extracted parameters. Then, these circuit models are replaced by spice circuit descriptions. Therefore, a step by step top-down design methodology is followed.

```
NT=1; stages = log2(N); t=0; l=N;   label = 0;
for d = stages:-1:1
  fprintf(fid,'-- Stage%d Begins\n\t',log2(N)+1-d);
    h=1; f=l/2; t=0; label = 0;
    for s = N/l:-1:1
        for m = l/2:-1:1
        %butterfly operation
        WWW = exp(j*2*pi*NT*(t)/N);
        fprintf(fid,'\n\t W%d_%d.repart<= to_sfixed(%d,3,-16);',d, h, real(WWW));
        fprintf(fid,'\n\t W%d_%d.impart<= to_sfixed(%d,3,-16);',d, h, imag(WWW));
        label =label+1;
        fprintf(fid,'\nlabel%d_%d: \n\t '   ,log2(N)+1-d,label);
        fprintf(fid,'component addition\n\t\t');
        fprintf(fid,'port map (\n\t\t');
        fprintf(fid,'a => temp%d_%d,\n\t\t',log2(N)+1-d,h+f);
        fprintf(fid,'b => temp%d_%d,\n\t\t',log2(N)+1-d,h);
        fprintf(fid,'c => temp%d_%d\n\t\t',log2(N)-d+2, h);
        fprintf(fid,');\n\n'); label =label+1;
        fprintf(fid,'\nlabel%d_%d: \n\t '   ,log2(N)+1-d,label);
        fprintf(fid,'component subtraction\n\t\t');
        fprintf(fid,'port map (\n\t\t');
        fprintf(fid,'a => temp%d_%d,\n\t\t', log2(N)+1-d,h);
        fprintf(fid,'b => temp%d_%d,\n\t\t',log2(N)+1-d,h+f);
        fprintf(fid,'c => tempmul%d_%d\n\t\t',d,h);
        fprintf(fid,');\n\n'); label =label+1;
        fprintf(fid,'\nlabel%d_%d: \n\t '   ,log2(N)+1-d,label);
        fprintf(fid,'component multiplication\n\t\t');
        fprintf(fid,'port map (\n\t\t');
        fprintf(fid,'a => W%d_%d,\n\t\t', d,h);
        fprintf(fid,'b => tempmul%d_%d,\n\t\t',d,h);
        fprintf(fid,'c => temp%d_%d \n\t\t',log2(N)-d+2, h+f);
        fprintf(fid,');\n\n');
        h=h+1; t=t+1;
       end;
     h=h+2^(d-1); t=0;
     end;
  l=l/2;NT=NT*2;
end;
```

Figure 3.12. MATLAB script for IFFT VHDL code generation.

The following section gives details about the automated co-simulation environment design. Then, non-ideality block parameters are defined and system simulations are given.

3.3.1. MATLAB and VHDL-AMS Co-Simulation Environment

There is an absence of a simulation platform between MATLAB and VHDL-AMS simulators. Therefore, a co-simulation environment is needed. Since MATLAB is a very powerful tool, it is selected as the primary development environment. System simulations are performed on VHDL-AMS simulator under MATLAB. Previously developed UWB channel model by [24] is used on MATLAB environment. So, it is not necessary to construct the channel model using VHDL-AMS codes, which takes additional design time. Impulsive noise is also added to the wireless channel simulations.

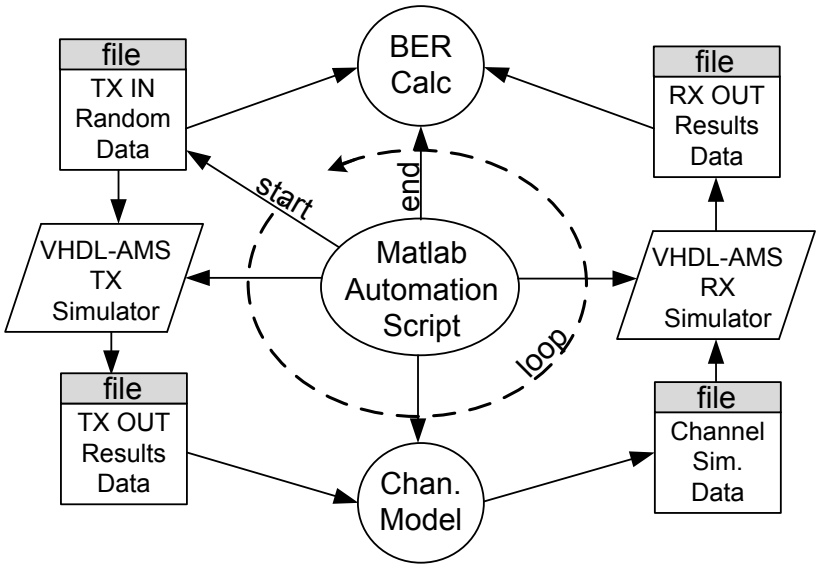

Figure 3.13. MATLAB and VHDL-AMS automated design flow.

The steps of the simulation are similar to the MB-OFDM automation. The simulation steps are represented by the chart in Figure 3.13. A full transceiver simulation environment is prepared. MATLAB scripts first create random data which are saved to a text file to be given as input to the transmitter. After the transmitter simulations are completed in VHDL-AMS, the results are saved to another text file. The transmitter output is an analog waveform. Therefore, it has to be sampled in fine time domain resolution that is matched to the resolution of the wireless channel models. In order to keep simulation time on a reasonable level, the step size is selected as 10 ps which correctly represents UWB pulses with 4GHz center frequency. Then, a wireless UWB channel model including AWGN and impulsive noise is applied to the transmitter results with noise levels are set by the user or swept automatically to observe the overall performance. After the wireless channel simulations of the transmitted UWB pulses, the results are written to another text file to perform receiver simulations on VHDL-AMS simulation environment. The same 10 ps sampling rate is used at the transmitter, channel models, and the receiver to avoid errors. The receiver outputs are then fed back into MATLAB and the system's BER graph is calculated from the receiver results.

3.3.1.1. Taylor and Volterra Series Representation. Mathematical models are written and simulated using the VHDL-AMS language. For correct representation of the blocks, Taylor and Volterra series are used. Linearity is important especially in multi-user OFDM based systems. In IR-UWB systems, extensive simulations are made to observe the effect. Volterra series take memory elements such as capacitors of an integrator into consideration. First three terms of the Taylor series expansion of y(t) is given as

$$y(t) = h_1 x(t) + h_2 x(t)^2 + h_3 x(t)^3. \tag{3.1}$$

The Volterra series is much more complex compared to the Taylor series because of the memory element representation as follows,

$$\begin{aligned} y(t) = &\int h_1(\tau_1)x(t-\tau_1)d\tau_1 + \int\int h_2(\tau_1,\tau_2)x(t-\tau_1)x(t-\tau_2)d\tau_1 d\tau_2 \\ &+ \int\int\int h_3(\tau_1,\tau_2,\tau_3)x(t-\tau_1)x(t-\tau_2)x(t-\tau_3)d\tau_1 d\tau_2 d\tau_3. \end{aligned} \tag{3.2}$$

Since there are no memory elements in LNA and SQR block the Volterra series converges to the Taylor series. Therefore, simple Taylor series can be used for a memoryless system.

3.3.2. Non-ideality Modeling

Receiver non-ideality parameters including linearity, matching, and transmitted pulse shape are studied and their effects on the system performance are determined. These results are used as circuit design parameters of the transceiver blocks.

3.3.2.1. Effect of Linearity on BER. Linearity is an important parameter especially on coherent systems. However, we would like to determine the importance of linearity on the performance of the non-coherent energy detection receiver design. For this reason, the linearity of the LNA and the squarer of the receiver are modelled using

Taylor series expansion. The linearity parameter IIP3 of these blocks are varied and BER performances are compared. The system simulations are given in Figures 3.14 and 3.15. It can be observed from the figures that the effect of linearity is more important in the design of LNA.

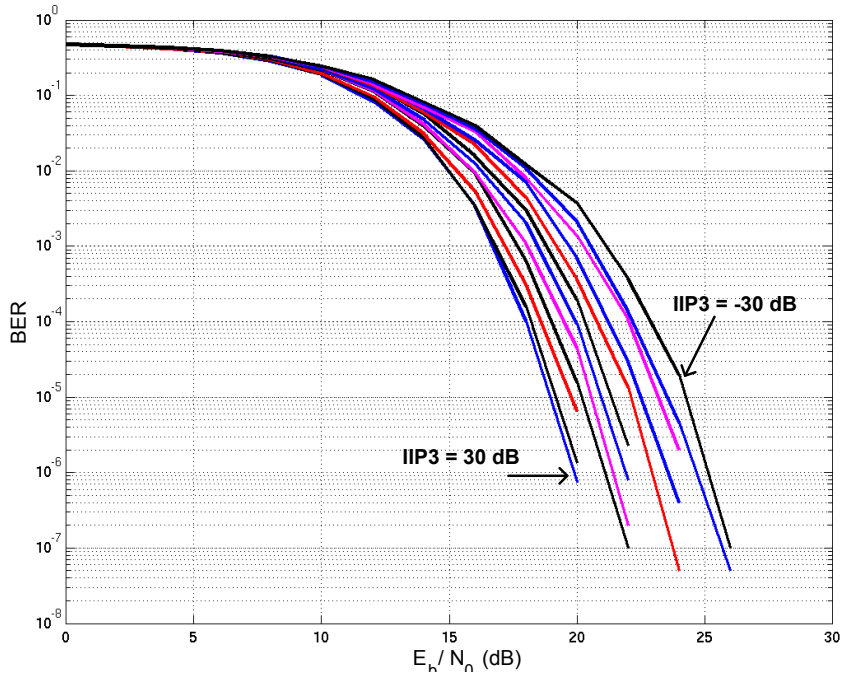

Figure 3.14. Effect of LNA linearity on BER performance.

3.3.2.2. Effect of Pulse Shape on BER. The transmitter generates a Gaussian monocycle pulse which is then filtered to obtain 3-5 GHz band limited signal, which is a high order pulse to fit the spectrum into the required band of interest. The effect of these different order pulses can be studied by system simulations to see which Gaussian pulse order is preferable over the others. The simulation results for different pulse orders; $2, 3, 4, 5, 12$ vs BER performance for non-coherent energy detection receiver are given in Figure 3.16. It can be seen from the figure that pulse shape does not have a significant effect on the performance. However, the energy of the pulse differs on the high order pulses. Nevertheless, system simulations show that different pulse shapes will not have significant effect on performance for moderate range IR-UWB applications.

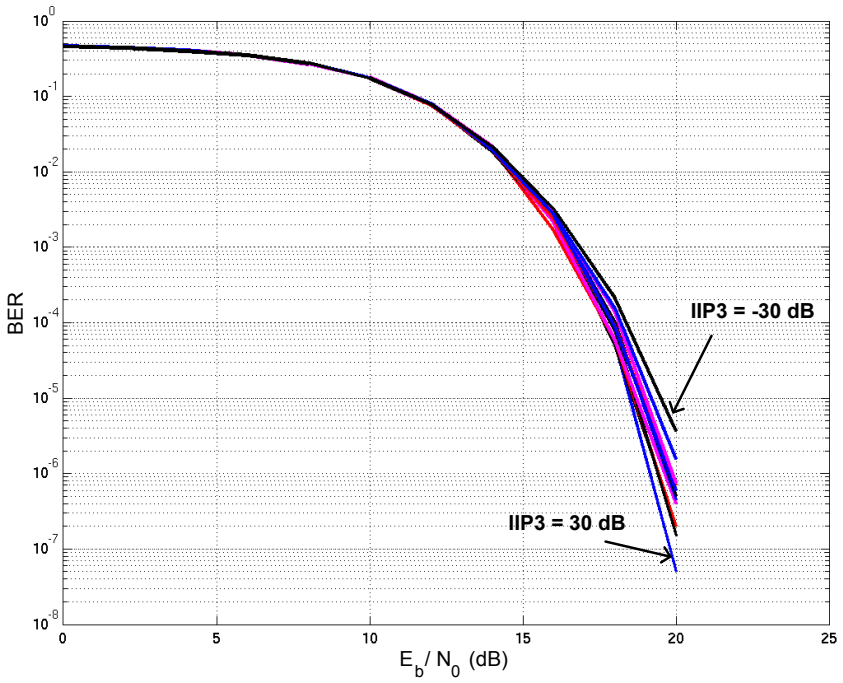

Figure 3.15. Effect of squarer linearity on BER performance.

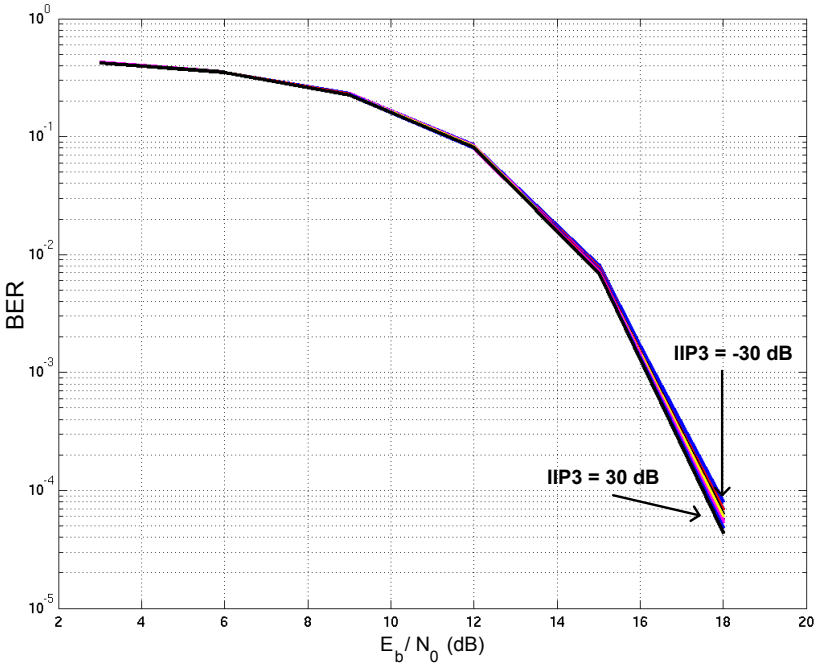

Figure 3.16. Effect of Gaussian pulse order on BER performance.

In the template based coherent IR-UWB receiver, the template pulse slides over the received pulse for synchronization. If the template pulse matches the received pulse, maximum correlation occurs and the peak energy is achieved. In Figure 3.17 the correlation results with different pulse orders are simulated using system level designs. The peak energy of the higher order UWB pulse is higher.

However, the main objective is to have a flatter response on the maximum energy level. Since the delay value is in the order of picoseconds, correlation should have a stable value in a wider time range for better synchronization and stable operation. It can be seen that even if the pulse energy value of the 2nd order Guassian pulse is significantly lower, the normalized energy shape has a flatter maximum energy response which will help receiver maintain synchronization for a longer time.

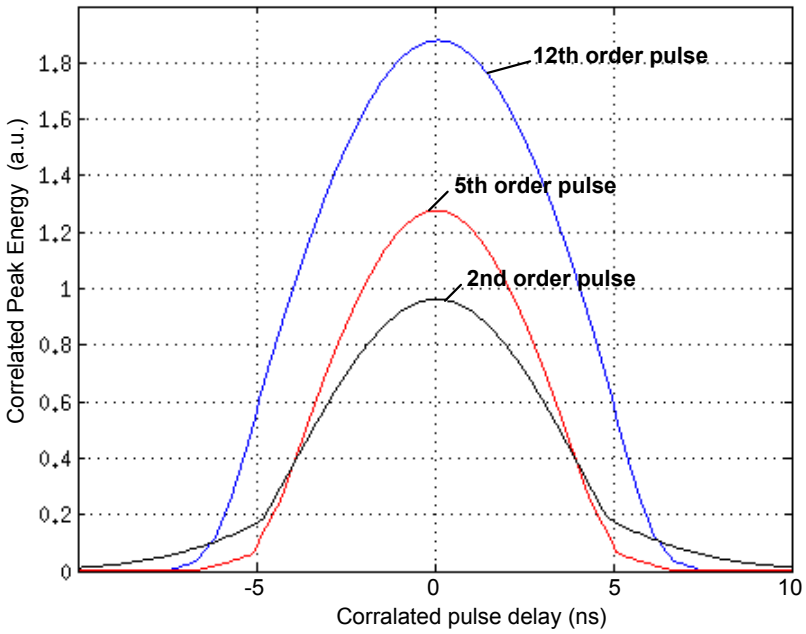

Figure 3.17. Peak energy graph of the correlated pulse.

The choice of the pulse order depends on multiple factors. If communication range is more important than the data rate, then higher order pulses can be used which are more difficult to synchronize. On the other hand, if data rate is important,

then synchronization should be done less frequently. Therefore, using lower order pulses help to achieve this purpose.

3.3.2.3. Effect of LNA Input Matching on BER. For maximum power transfer, the antenna and receiver input impedances must match. However, it should be noted that matching and noise figure are conflicting design challenges. Therefore, an optimum point between the noise figure and matching must be found. Hence, matching will not be at its best for most designs. The effect of matching on system BER is simulated in Figure 3.18. At the matched load, the best BER result is obtained. We can see from the figure that, if not perfectly matched, unmatched resistance must be higher to to have low BER.

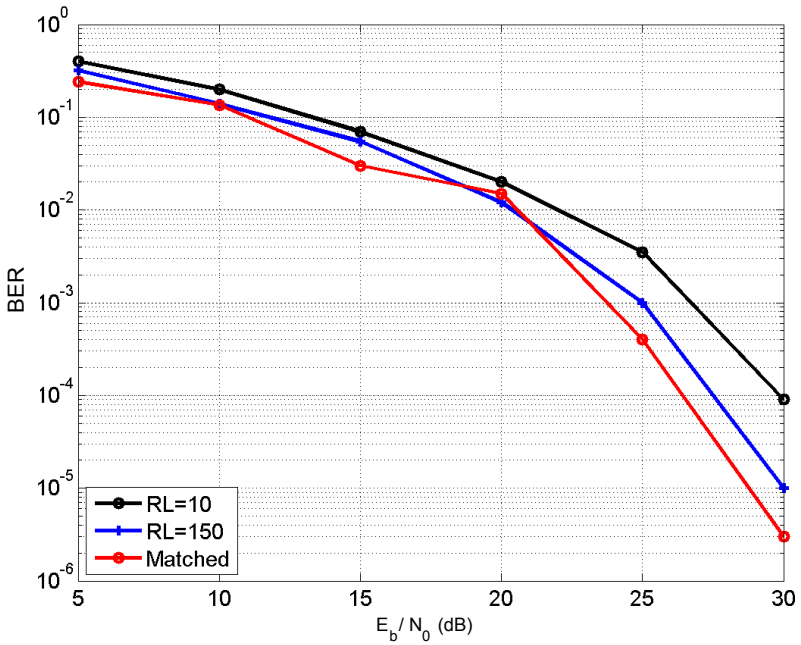

Figure 3.18. Effect of matching on BER performance.

One can clearly seen from system simulations that the system performance is determined by same circuit parameters and some parameters like pulse shape have minor effect. Therefore, circuit complexity can be greatly lowered by using second order Gaussian mono-cycle at the transmitter. The linearity of the squarer can be relaxed and the design can be focused on the sensitivity of the squarer block. On the

other hand, matching and linearity of the LNA must be acceptable in order to reach good BER values at short distances. These results give direction and focus points on the design of better transceiver systems at lower costs.

3.4. Conclusion

Two computer aided co-simulation environments have been created for the automated design of MB-OFDM and IR-UWB transceivers. The created tools help designer to manage the system level circuit coefficients and identify their effects on the system performance. Hence, it will shorten the overall design time and help designer to build better transceiver.

In the MB-OFDM UWB approach, a MATLAB-VHDL design automation environment is presented with its reconfigurable features which avoids redesign of the blocks. Parameters of the blocks are set to obtain the digital baseband VHDL model of MB-OFDM UWB system. The UWB system model is written to be synthesizable and reconfigurable. The VHDL model is successfully synthesized to Xilinx Vertex-4 FPGA. This MATLAB-VHDL design automation system can be applied to VHDL modeling of other OFDM based communication systems. Designer can add analog circuits and can make mixed simulation of the system using VHDL analog mixed signal (VHDL-AMS).

In the IR-UWB approach, the circuit models are hand written on VHDL-AMS with generic parameters that can be changed at the top-level MATLAB code. Since, the top level control is performed by MATLAB scripts, VHDL-AMS simulator works at the background when it is required. The advantage of using VHDL-AMS is that these codes can be replaced by real circuitry during the design.

4. VLSI DESIGNS OF IR-UWB TRANSMITTER

4.1. Introduction

This chapter is focused on ultra-low power IR-UWB transmitter designs. During the thesis, two extremely low power transmitters were designed in UMC 130MMRF technology and measured. The pulse generation methods are similar in both transmitters. The first design is a dual-band transmitter that can work in 3-5 GHz band as well as 0-960 MHz band. The second transmitter is an improved version of the first design which is configurable. The following sections cover both transmitters in detail, as well as a literature survey on IR-UWB transmitter architectures.

4.1.1. Literature Overview of IR-UWB Pulse Generation Architectures

The 0-960 MHz and 3.1-10.6 GHz frequency bands were allocated for the unlicensed ultra-wideband (UWB) applications. The spectral mask limitation of the upper band is set to -41.3 dBm/MHz and the lower band is limited to -65 dBm/MHz for medical applications by the U.S. Federal Communications Commission (FCC) in 2002 [12]. Since then, there has been an increase in research activities for the UWB circuit design in a wide range of applications such as low power radio design for telemetry and wireless sensor networks. For instance, IR-UWB operating in the 0 - 960 MHz band is a key method for building low power circuits for remotely powered biomedical devices. Because the 5–6 GHz band is utilized for the wireless-local-area-network (WLAN) systems, conventional UWB systems have been recently allowed to operate in two bands, i.e., 3.1–5 GHz and 6–10.6 GHz. The unlicensed band of 7 GHz is allocated in 60 GHz for high data rate WPAN applications. Automotive short range radars are operated in 24 GHz and 79 GHz and long range radar is working at 77 GHz. IR-UWB devices utilize large bandwidths in any of these frequency bands by use of short-duration pulses that are compliant with the spectral mask regulations. With the emergence of a large variety of UWB applications, the transmitter, and particularly the transmitted pulse design, has become an active research area within the UWB literature (we refer the

reader to [48], Chapter 7 and the references therein for a thorough review).

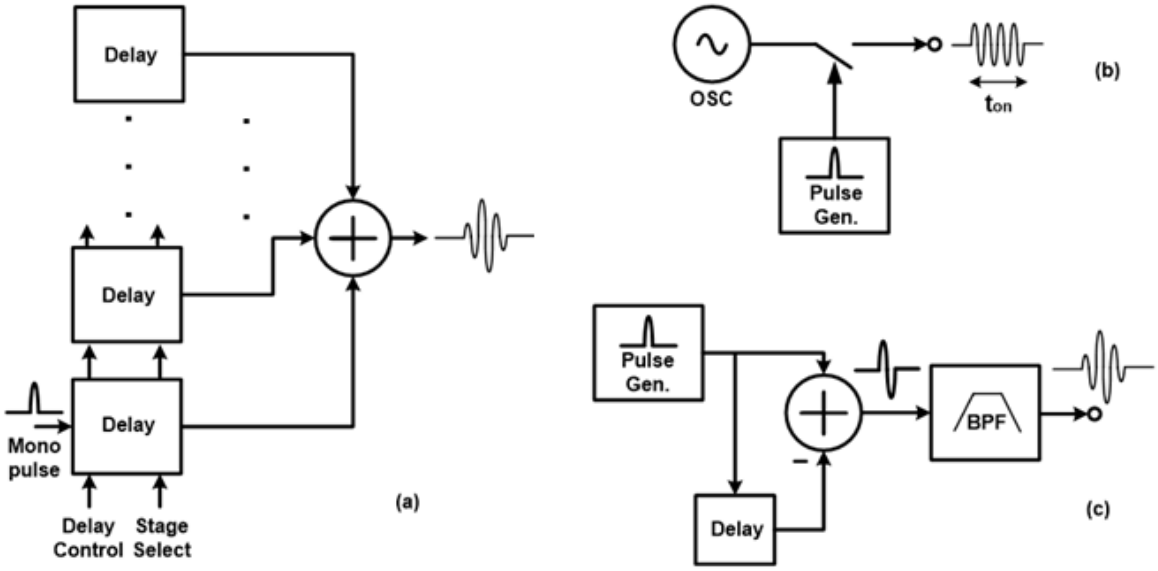

Figure 4.1. Transmitter architetures (a) Pulse combination, (b) Oscillator, and (c) Filtering methods.

As presented in [48]-Chapter 7, various types of pulses can be used for different UWB applications, such as the Gaussian mono-cycle for the 0 - 960 MHz band [63] and the Gaussian 5th order multi-cycle pulse for the entire 3.1 - 10.6 GHz UWB spectrum [64]. At the circuit level, several methods have been employed to generate these pulses, including pulse combining [65, 66], oscillator-aided [67] and pulse-shaping [68, 69]. In the pulse combining method, Gaussian mono-cycles are delayed, inverted and combined to generate higher order multi-cycle UWB pulses as depicted in Figure 4.1a. The delay and inverter blocks must be carefully adjusted in order to create the correct pulse shape. In the oscillator-based methods shown Figure 4.1b, the oscillator signal is applied to the output for a short period of time at the desired center frequency. In the filtering method, a wideband pulse is created and then it is filtered to obtain higher order pulse shape as shown in Figure 4.1c. As illustrated in all three architectures, both the pulse shape/order and also the low-power requirement are key design issues to be considered in the selection of the transmitter architecture.

4.2. Dual-Band Transmitter Design

OOK modulation is selected for the transceiver in this thesis. The transmitter is composed of a pulse modulator, an ultra-sharp glitch generator, delay blocks, and an output pulse shaper with an off-chip pulse shaping capacitor and a BPF. The transmitter is all-digital with the exception of the output pulse shaping stage.

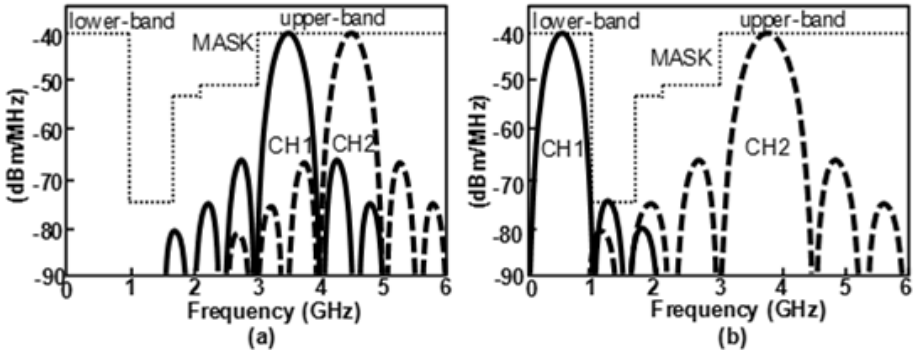

Figure 4.2. Dual-band spectrum (a) conventional method, (b) designed transsmitter.

One of the novel features of the receiver is its dual-band property. The transmitter in [63] is also specified as being "dual band" where this term is used for the two subbands within the 3.1–5 GHz UWB band. For the proposed transmitter, however, it refers to the 0–960-MHz band and the entire 3.1–5 GHz bands as shown in Figure 4.2.

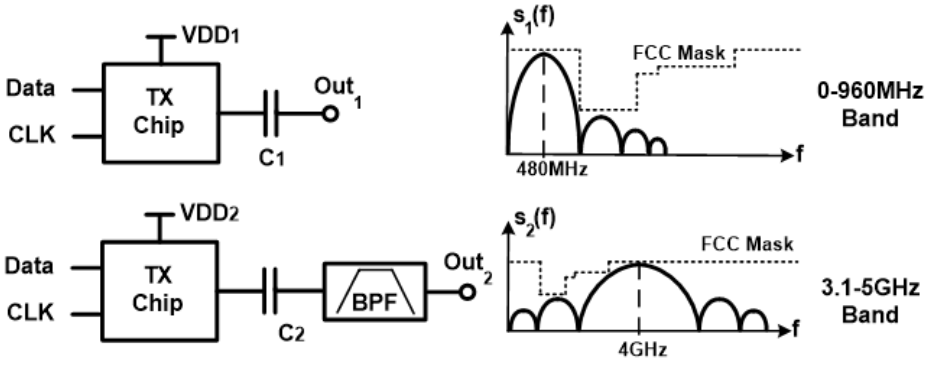

Figure 4.3. Transmitter reconfiguration for dual-band operation.

The pulse orders differ for best coverage of these bands. The best coverage of the 0–960 MHz band is achieved by the Gaussian mono-cycle, whereas there is a need

for a much higher order pulse for the 3.1–5 GHz band. Thus, an external BPF is used to generate the higher order pulse as shown in Figure 4.3. In this system, the two channel bands have a larger separation than the method in [63]. The channelization restrictions are relaxed in the upper band so as to facilitate the use of a low-power bandwidth control circuitry.

In addition to being capable of operating in the two distinct bands, to the best of our knowledge, the proposed UWB transmitter dissipates less power than the other transmitters in the literature designed specifically to operate at only one of the bands (specifically, the architectures in [31–33, 63–65, 67, 68, 70–81]). As a side benefit to the low-power dissipation, the energy per pulse (EPP) of the proposed transmitter remains mostly constant irrespective of the pulse repetition frequency (PRF). Thus, low data rates require lower power, which is not the case for some of the designs such as those in [33], [67], [74], and [77].

The power efficiency and robustness of the pulse design are achieved as follows. Pulse generation in the proposed UWB transmitter utilizes the pulse-shaping architecture as in [66] and [68]. In this approach, higher order UWB pulses are obtained by filtering the output of a Gaussian mono-pulse using a BPF. This method contains a smaller number of components and thus consumes less power than its counterparts such as pulse-combining [64] and oscillator-aided [32] approaches. For more aggressive power reduction, a frequency control circuitry is not employed. A passive BPF is utilized to guarantee the desired pulse shape. The dual-band utilization is achieved by using a single integrated-circuit chip with reconfiguration.

Figure 4.4a and Figure 4.4b show the schematic of the UWB transmitter and post-layout simulation results of the internal waveforms, respectively. The pulse generator is designed to transmit pulses at the rising edge of the modulated signal with the clock. Buffering is performed using inverters to sharpen the edges at the incoming off-chip data and the clock signals. The data signal is modulated with an OOK modulator, which is composed of a nand gate and inverters.

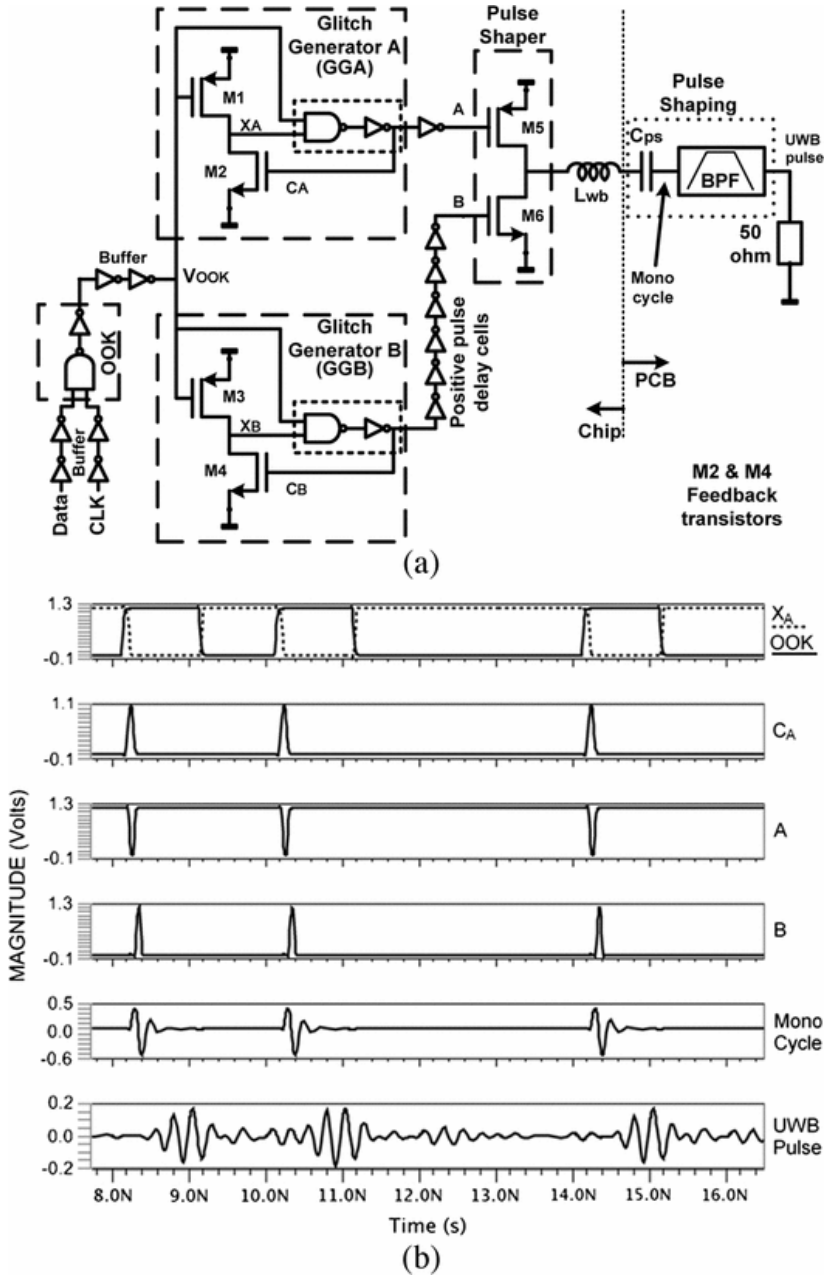

Figure 4.4. (a) Block diagram of the proposed transmitter and (b) post-layout transient simulation results of the internal and external nodes.

Two identical glitch generators (GGs) labeled as GGA and GGB, are designed to generate mono-cycles at the rising edge of the modulated signal. The GG consists of a combiner (M_1 and M_2) and an OOK modulator. The input signal is applied to the PMOSFET of GGA, M_1, and one input of the modulator. The output of the GG is fed back to the input of the combiner through an NMOSFET M_2. The combined

output signal V_{XA} is applied to the other input of the modulator. When the incoming V_{OOK} signal is 0 V, the modulator output is also 0 V. As a result, M_1 turns on and M_2 turns off, and then, V_{XA} becomes V_{DD}. When the input signal rises from 0 V to V_{DD}, M_1 turns off, and V_{CA} becomes V_{DD}. As a result, M_2 turns on, and V_{XA} falls to 0 V. After a short propagation delay through M_2 and the modulator, the GG output returns to 0 V. During this transition, a short mono-cycle pulse is formed. To have a stable pulse, when the input is high, the sizes of M_1 and M_2 are designed such that the OFF-state impedance of M_2 is lower than that of M_1. When the input returns from V_{DD} to 0 V, the upper input of the modulator becomes 0 V. Therefore, the mono-cycle pulse is generated only at the rising edge of the input data. The GGA output is inverted and applied to PMOSFET M5 of the output pulse shaper; as a result, the pulse-generator output becomes V_{DD}. The output signal of GGB (which is identical to GGA) is delayed using a six-stage inverter chain and applied to NMOSFET M_6 that drives the output voltage to 0 V. The output pulse shaper stage transistor M_5 and M_6 sizes have to be selected carefully for correct pulse shape. The M_6 transistor width must be selected to be much larger than that of M_5 to be able to generate the negative pulse. M_6 must not be selected to be very large to avoid the parasitic oscillations.

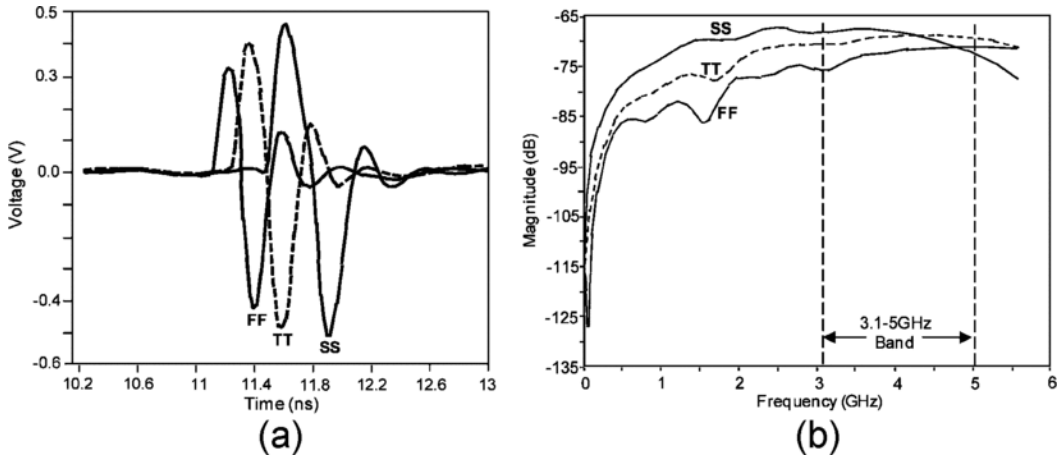

Figure 4.5. Typical–typical, slow–slow, and fast-fast simulations. (a) Pulse shape. (b) Pulse spectrum.

The center frequency of the digital pulse generator relies on the propagation delay that can be controlled by the supply voltage. During the design procedure, the

supply voltage is kept constant at its nominal value of 1.2 V. The gate sizes for the building blocks are determined to have a UWB pulse inside the 3.1–5 GHz band for the best and worst case processes and supply voltage variations, as shown in Figure 4.5b. Then, the supply voltage is reduced gradually to give the sufficient value for the 0–960 MHz band operation (0.51 V in this design). The transmitter efficiency is reduced in the fast–fast (FF) corner case because of the low peak-to-peak voltage level, as seen in Figure 4.5a.

Figure 4.6 shows 100 different Monte Carlo realizations of the generated pulses under process, supply voltage, and temperature variations. As seen from the figure, the transmitter is robust against these parameter variations.

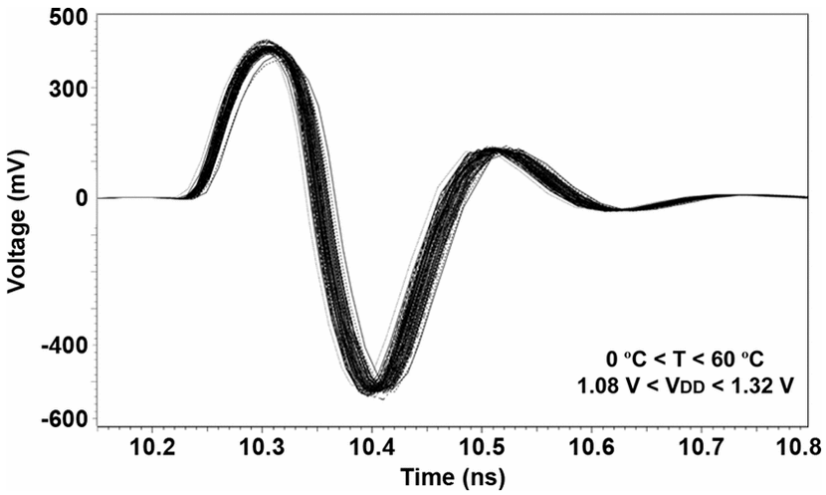

Figure 4.6. Pulse shape over 100 Monte Carlo runs.

The transmitter output shown in Figure 4.4 is applied to the package and off-chip PCB through a wire bond that can be simplified as an equivalent 2.5 nH inductance. A 3.1–5 GHz band BPF is realized using a 0.7 pF series capacitance. The filter order can be increased with an additional off-chip BPF. In this test board, a 1.6 mm $\times$ 0.8 mm off-chip BPF that is 38 times smaller than the chip package size is utilized. Gaussian and higher order UWB pulses are obtained before and after the BPF, as shown in Figure 4.4b.

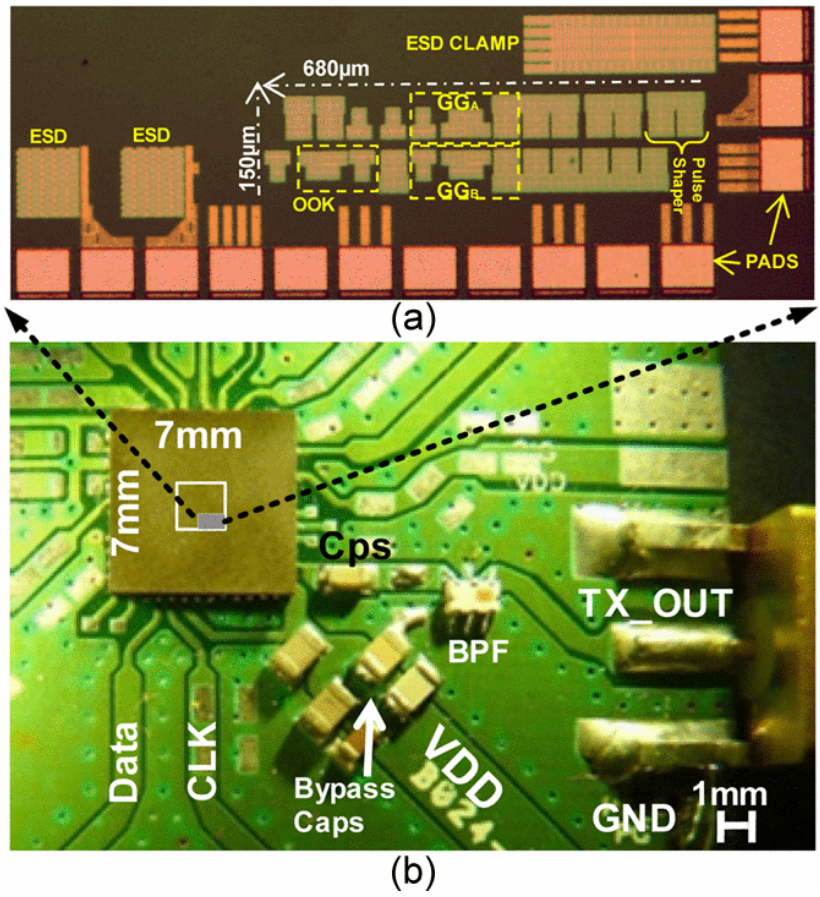

Figure 4.7. (a) Micrograph of the UWB transmitter in a UMC 130-nm process. (b) Picture of the RF FR-4 PCB and components used in the measurements.

4.2.1. Measurement Results

The transmitter is manufactured using UMC MMRF 130-nm CMOS process. The micrograph is shown in Figure 4.7a The whole transmitter including the OOK modulator and the pulse generator, together with the buffers, occupies only a 0.1 mm^2 die area. Electrostatic discharge (ESD) input and ESD clamp protection circuitry are designed to resist 2000 V. Standard metallic radio-frequency (RF) pads of Formula are used for bonding. An air-cavity 48-pin quad-flat-pack no-lead 7 mm × 7 mm package is used for the fabricated silicon die. The measurements are taken from the packaged chip on a designed coplanar-waveguide RF PCB on an FR-4 substrate using subminiature-version-A (SMA) connectors. The RF FR-4 PCB picture with all

components is shown in Figure 4.7b. In the measurements, a signal source is used to generate input to the transmitter. Then, the response of the transmitter is measured with different oscilloscopes and spectrum analyzers according to the band of interest. OOK modulation tests are performed with a 10-Mbit/s Ethernet signal as the data input and a 50-MHz square signal as the clock input to the transmitter. Power measurement results include power dissipation due to the ESD circuitry.

4.2.1.1. 0-960MHz Band Measurements. Figure 4.8 shows the 0–960-MHz-band operation and the measurement results. Here, the V_{DD} is set to 0.51 V, and a 100-nF pulse-shaping capacitor is selected. A Gaussian mono-cycle of 2-ns width is measured. The peak-to-peak voltage is 340 mV including the SMA cable loss. In this band, the DC-to-RF conversion efficiency is measured as 11.1%. Efficiency calculations can be found in [66] and [67].

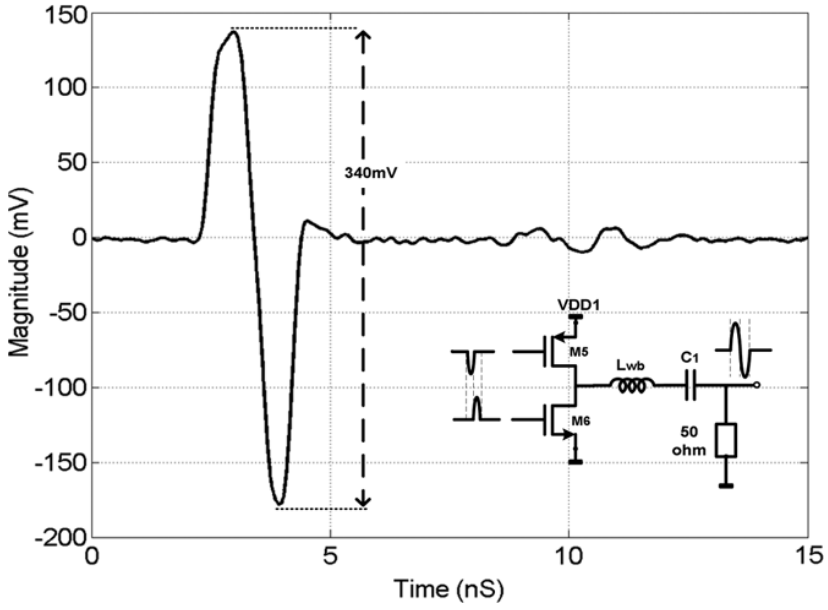

Figure 4.8. Transmitter output with a pulse-shaping capacitor.

The frequency-domain measurements for the PRFs of 300 kHz, 1 MHz, and 8 MHz are shown in Figure 4.9. The transmitter can be used in compliance with FCC up to 300 kHz PRF [12]. The transmitter is capable of UWB signalling up to 500 MHz PRF. Eleven chip samples are mounted on 11 PCB samples to measure the chip-to-chip

variations. Time-domain measurement results and respective fast Fourier transforms (FFT) are shown in Figure 4.10a and Figure 4.10b, respectively. The temperature variation effect is also measured by heating the board from Formula to 70 °C. The measurement results are shown in Figure 4.10c and Figure 4.10d.

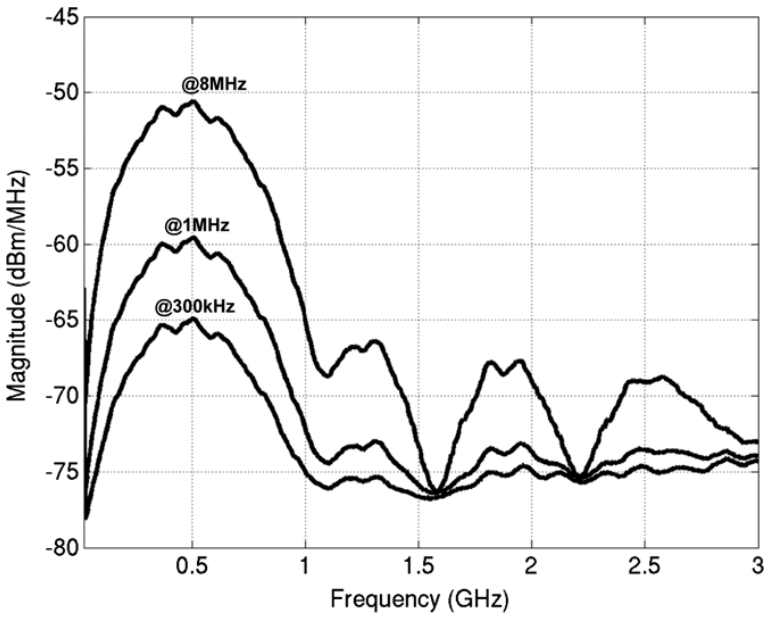

Figure 4.9. Spectrum measurement in the 0–960 MHz band with PRF at 300 kHz, 1 MHz, and 8 MHz.

4.2.1.2. 3.1-5 GHz Band Measurements. For the 3.1–5 GHz band operations and measurements, the Formula is set to its nominal voltage of 1.2 V. A 0.7 pF pulse-shaping capacitor is used at the output. The output SMA connector is plugged to the oscilloscope without a BPF. Notice that the RF peak-to-peak voltage is larger than the oscilloscope limits; therefore, a 6 dB attenuator is connected between the pulse generator and the oscilloscope. After the calibration of cable and attenuator losses, the peak-to-peak voltage is measured as 810 mV. Figure 4.11 shows the time-domain measurement results where the positive and negative cycles of the Gaussian mono-cycle are observed. Due to the bond-wire inductance and parasitic capacitances, a damped oscillation can be seen at the end of the Gaussian mono-cycle.

To create band-limited IR-UWB pulses, a 3.1–4.9 GHz Johanson 4000BP15U1800

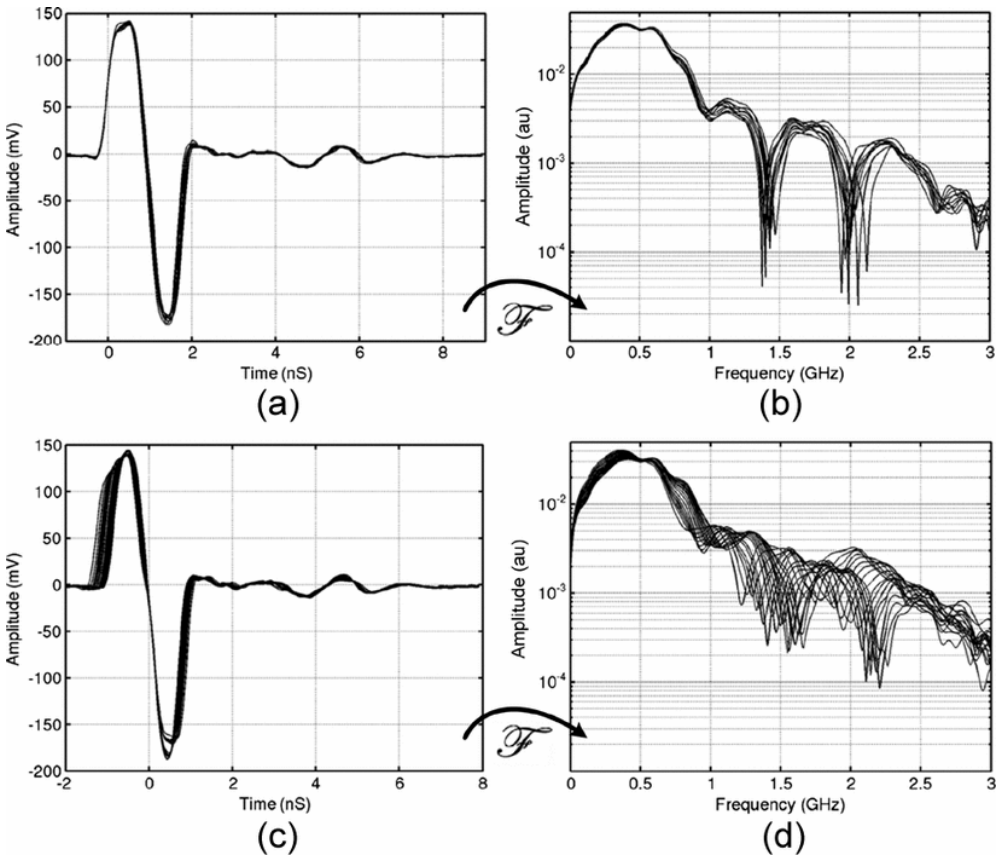

Figure 4.10. Output variation in time domain of (a) 11 chip samples (c) from -20 °C to 70 °C at 5 °C steps. Output variation in the frequency domain of (b) 11 chip samples (d) from -20 °C to 70 °C at 5 °C steps.

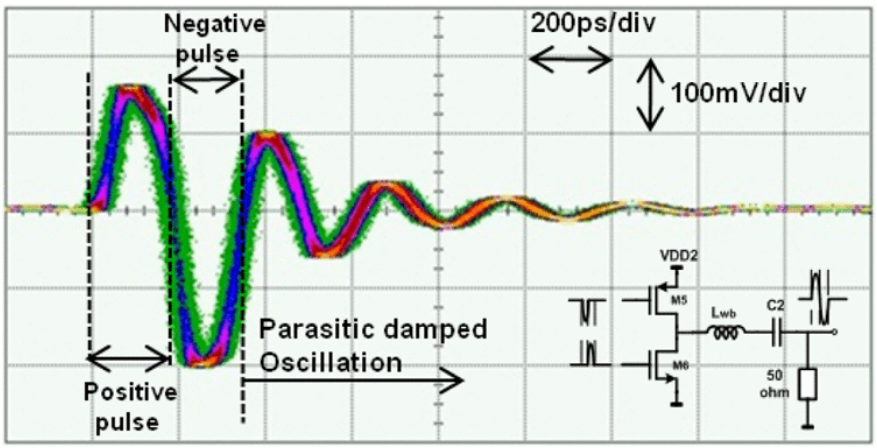

Figure 4.11. Transmitter output with pulse-shaping capacitor.

BPF with 2-dB insertion loss is used after the pulse-shaping capacitor. This insertion brings an additional 3.4 dB loss at the output. To compensate for this loss, the 6 dB attenuator used to scale the waveform in the oscilloscope screen is removed. The time-domain response for a PRF of 200 MHz is shown in Figure 4.12. The output swing including the cable loss is measured as 530 mV. The DC-to-RF conversion efficiency is measured as 4.8% in the 3.1–5 GHz band. The pulse width including the pulse tail is 1.8 ns.

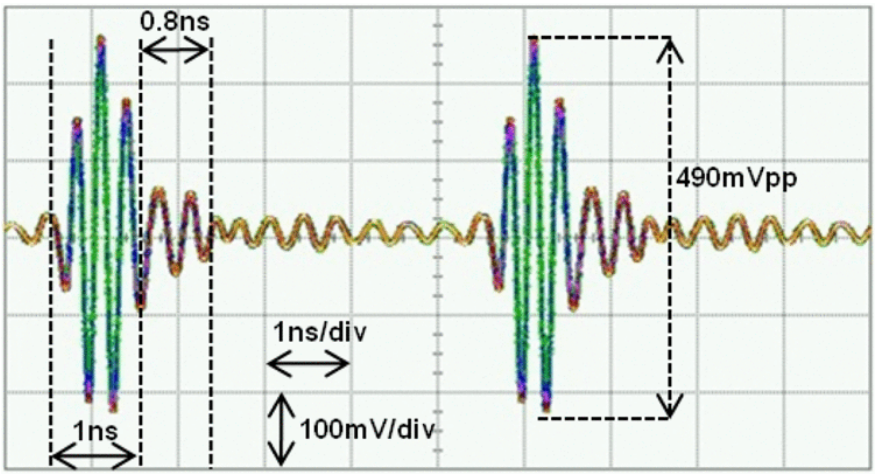

Figure 4.12. Transmitter output with BPF.

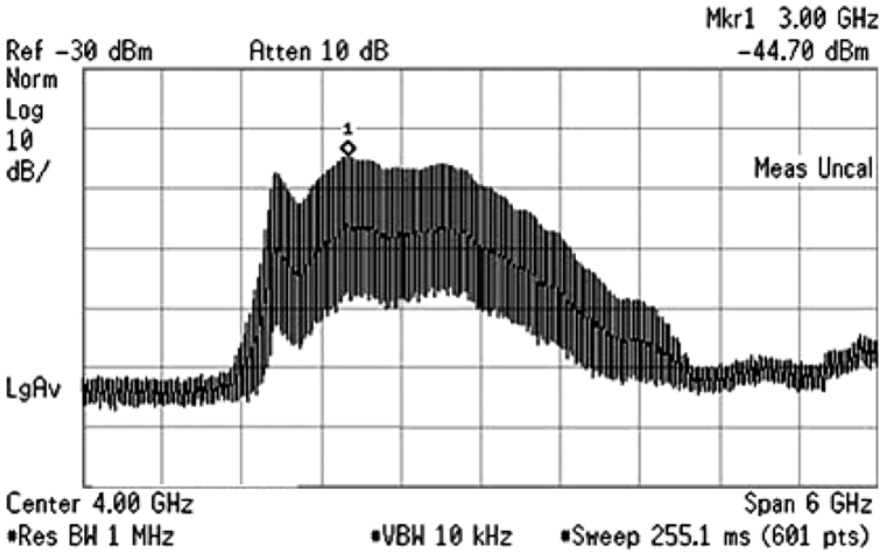

Figure 4.13. Output spectrum in the upper band at 10 MHz PRF.

The frequency-domain response is shown in Figure 4.13. The bandwidth is between 2.6 and 4.4 GHz with −44.7 dBm/MHz power spectrum. At a PRF of 10 MHz, the transmit signal levels exceed the mask. However, in practice, the signal complies with the mask because the transmit antenna increases the filtering order to be able to fit in the 3.1–5 GHz band. This pulse generator can also be used without any additional filter using low transmit power in short-range applications.

The measurement results are summarized in Table 4.1. To increase the propagation delay in the digital circuitry, the supply voltage is reduced to 0.51 V for the lower band. The times required to generate the UWB pulse (turn-on time) are less than 1 and 10 ns for the upper and lower bands, respectively.

Table 4.1. Measurement Results.

	0-960 MHz Band	**3.1-5 GHz Band**
FCC Compliant PRF	0-300 kHz	0-7 MHz
Max. PRF Range	0-500 MHz	0-550 MHz
Supply	0.51 V	1.2 V
Power Consumption	5.6μ@1 MHz	31μ@1 MHz
Standby Power	0.36 μW	1.7 μW
Pulse Width	2 ns	1.8ns with tail
Output voltage swing	340 mV	530 mV
Energy/pulse	5.3 pJ@10 MHz	26.5 pJ@10 MHz
Pulse Energy	0.59 pJ	1.27 pJ
Efficiency	11.1%	4.8%
TX-BW(-10 dB)	750 MHz	1.8 GHz
Turn on time	10 ns	1 ns

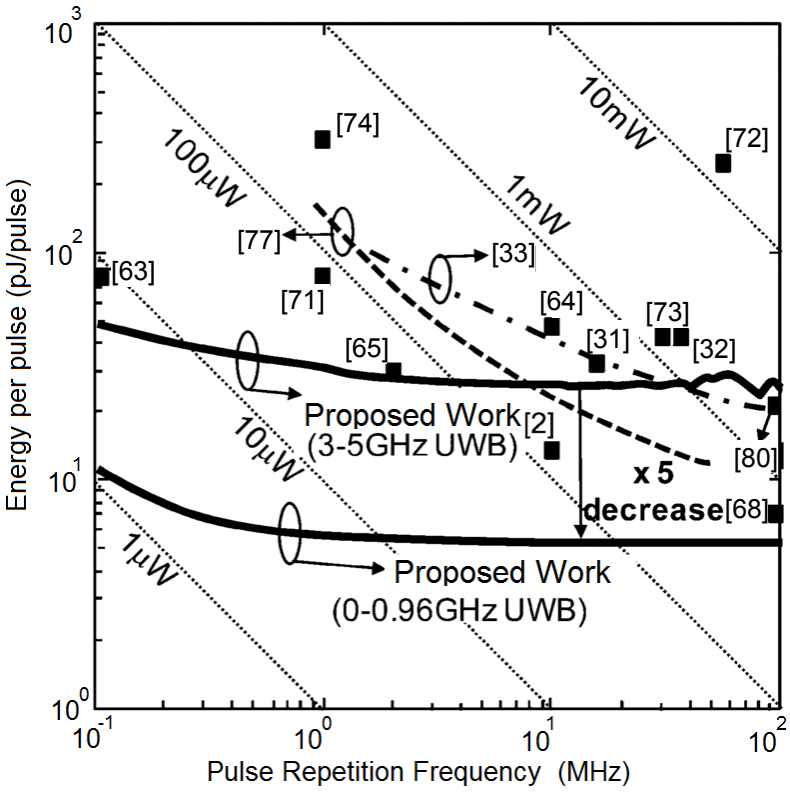

Figure 4.14. EPP Comparison.

4.2.2. Discussion and Comparison

The measurement results of the transmitter are compared with the previous low-power and high-efficiency architectures [31–33, 63–65, 67, 68, 70–81] in Figure 4.14. The EPP [68] figure-of-merit (FOM) comparison is shown in Figure 4.14 and Table 4.2. As the PRF decreases, the effect of static power increases. High-complexity digital architectures with sub-100 nm channel lengths have large static power consumption in the low data rates due to the leakage currents. On the other hand, the leakage power of the proposed transmitter is less than 2 Formula. The effect of leakage current is observed when the PRF is less than 200 kHz. Because of the low-leakage digital circuitry and off-chip passive pulse shaping, the proposed dual-band transmitter consumes less power than the recently reported IR-UWB transmitters operating in the 0–960 MHz and 3.1–5 GHz bands. The work in [79] has an EPP of 1.8 pJ/pulse at 100-MHz PRF. However, it should be noted that the lower EPP is due to the lower peak-to-peak

voltage and short pulse width. The efficiency of the proposed transmitter is 74-fold better than that of the pulse generator in [79].

Table 4.2. Performance Comparison.

Refs	**f-band (GHz)**	τ **(ns)**	**Vpp (mV)**	**EPP (pJ/Pulse)**	**Effic. %**	P_{DC} μ**W**	**Ext BPF**
Our Work	3.1-5	1.8	530	26.5	4.8	1.7	Yes
[**70**]	3.1-5	3.5	160	16.8	0.4	3900	No
[**68**]	3.1-10.6	0.38	660	8.14	2.6	19800	No
[**74**]	3.1-5	2	385	300	0.0024	-	Yes
[**75**]	3.1-10.6	0.46	1420	9	6	3200	No
[**76**]	0-0.96	0.81	510	27	1.95	-	No
[**77**]	3.1-5	3	91-126	12	1	170	No
[**79**]	3.1-10.6	0.15-0.35	28-107	1.8	0.065	-	No
[**81**]	3.1-5	1	160	90	0.071	-	No

More FOM comparisons including EPP and efficiency are listed in Table 4.2. Also, please note that the EPPs for most of the papers under comparison are obtained with dc power only during the pulse generation, assuming that the circuit is turned off between pulses. However, in our work, steady power consumption is included. If a similar technique is applied, EPP in our work will go to very low values that are close to the pulse's energy.

4.3. Reconfigurable Transmitter Design

The low power requirement can be satisfied by an all-digital IR-UWB transmitter as done in [69]. However all-digital pulse shaping circuits generally have high sensitivity against process variations, causing undesired center frequency shifts. In this regard, the novel contribution of this design is the proposal of an all-digital, ultra-low power and configurable IR-UWB transmitter having an adjustable center frequency

in a wide range. The proposed transmitter can precisely adjust both positive and negative pulse widths as well as the delay between the pulses. Notice that several other configurable architectures have been also proposed in [82–85]. The transmitter in [82] is designed to be used at low data rates with a specific PRF range. Even though the one in [83] provides high data rates, its configurability is added for beam forming purposes. Therefore, the transmitter does not operate in the low frequency band and it can be used for short range applications. In [84], the center frequency can be adjusted with a good EPP performance but in a limited frequency range. In [85], the bandwidth is adjustable with high efficiency but center frequency configurability is not considered. In this regard, the proposed transmitter not only has a reasonably good EPP performance but also operates with a wider center frequency range than previous state-of-the-art in the related literature as demonstrated by extensive measurement results.

4.3.1. Transmitter Architecture

The configurable all-digital transmitter utilizes the pulse combination method to generate UWB pulses. The overall power consumption changes from 9.6 pJ/pulse to 35.6pJ/pulse depending on the configured center frequency and PRF. Off-chip pulse shaping elements are avoided. Instead, an on-chip pulse shaping capacitor is used. Shift registers are employed for configurability.

The block diagram of the transmitter is given in Figure 4.15. There are two configurable parameters; the pulse width and the pulse position of the Gaussian mono pulses, which are then combined to generate Gaussian mono-cycle at the pulse shaper stage. Configurable delay cells are designed to control these parameters. Delay cells are composed of inverters with digitally adjustable shunt loaded capacitors. Shift registers are placed to set these capacitor values digitally by the user.

The output voltage swing can reach up to 1.3 V and the center frequency can be changed between 500 MHz and 4 GHz. The output pulse shaping capacitor is fixed to 700 fF, which results in a large voltage swing of 1.3 V at the 4 GHz center frequency

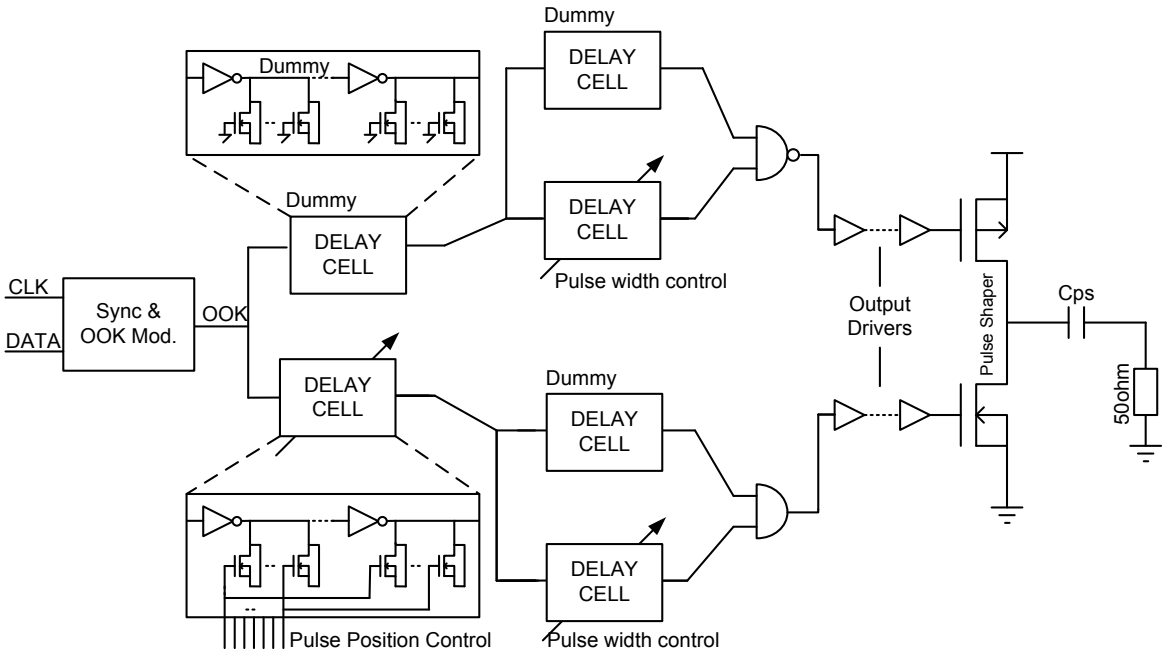

Figure 4.15. Transmitter architecture.

in simulations. At the first mono pulse, the PMOS is turned on and the output pulse shaping capacitor is charged; in the following mono-pulse, the PMOS is turnd off and the NMOS is turned on, and the charge in the capacitor flows to ground. Therefore, the second pulse width is kept a little larger in time than the first pulse, in order to discharge the output pulse shaping capacitor completely. If the capacitor is not fully discharged, unwanted oscillations occur after the Gaussian mono-cycle.

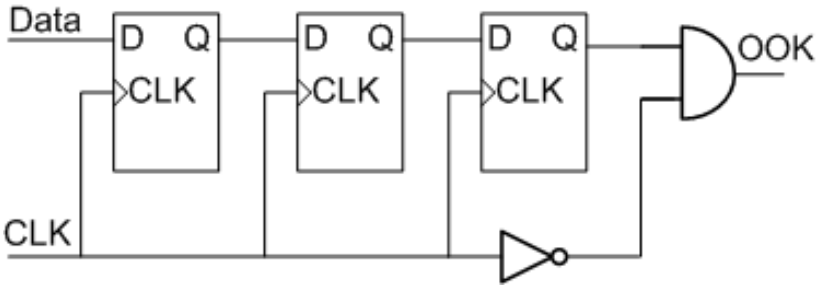

Figure 4.16. OOK modulator with synchronizer.

4.3.1.1. Synchronizer and OOK Modulator. Synchronizer is the first stage of the transmitter. In order to prevent glitches caused by the overlapping of DATA and CLK signals, a synchronizer is needed before the OOK modulation. Otherwise, glitches produce undesired pulses at the transmitter output. Therefore, positive edge trig-

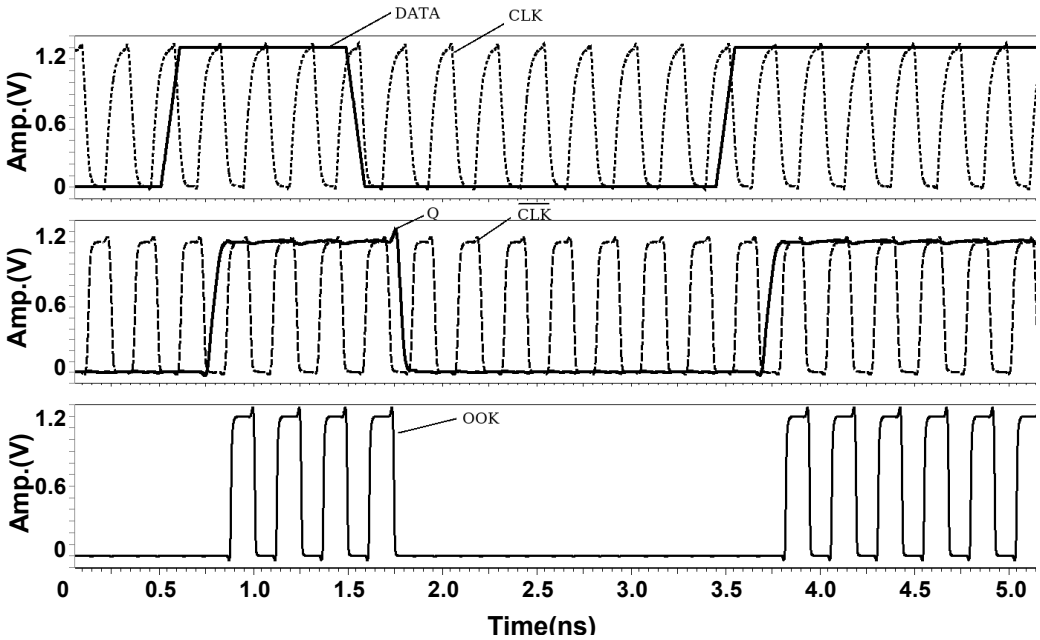

Figure 4.17. OOK modulator simulations.

gered DFF is used to buffer the data using clock signal. Since the data is sampled with the clock signal, it will be perfectly synchronized. However, it has to be noted that the clock must be at least twice the frequency of the data, because of the Nyquist rate. The DFF chain and OOK modulator can be observed in Figure 4.16. OOK is composed of a simple AND gate. To prevent metastability and get more consistent results, three DFFs are connected in series. An additional inverter is used to prevent glitches in the OOK stage because of the overlapping of the rising and falling edges. The simulation results can be observed in Figure 4.17. It can be seen from the results that the data and clock are perfectly synchronized and the output does not have any glitches. Note that the OOK modulator can be bypassed by setting DATA to V_{DD}. Then, CLK can be used as DATA input and external modulation can be applied.

4.3.1.2. Delay Cell. Delay cells are composed of inverter stages with switched capacitor loads as depicted in Figure 4.18. The configurable load capacitor is the easiest and most effective way to control the propagation delay in constant and linear delay increments. The pulse width and the pulse delay values are digitally and linearly configured by these delay cells. MOS capacitors are used at the output of the inverter stages.

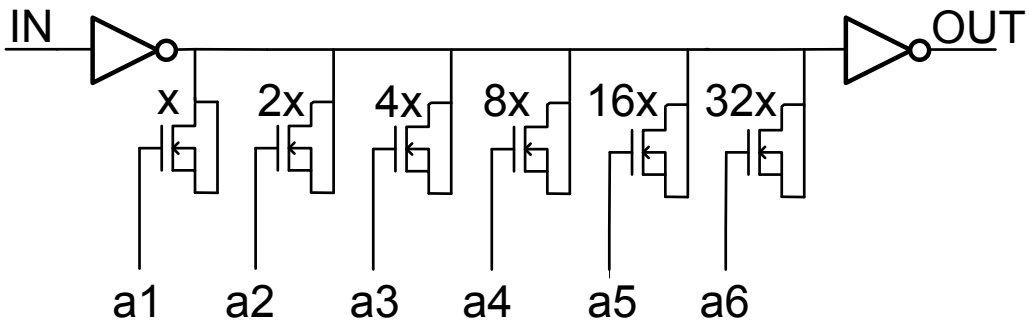

Figure 4.18. Configurable delay cell.

Triple well floating NMOS devices are exploited to reduce the effect of substrate noise. The WL product of the MOS devices determines the value of the capacitor. However, the delay is not increased linearly with the WL product because of the parasitic effects at the drain and source regions. In order to achieve linear delay, a unit size MOS capacitor is selected. Then, instead of increasing the WL product of the MOS capacitor, the number of unit size MOS capacitors is increased.

$$T_d = R \cdot [C_p + C \cdot (a_1 + 2 \cdot a_2 + 4 \cdot a_3 + 8 \cdot a_4 + 16 \cdot a_5 + 32 \cdot a_6] \tag{4.1}$$

represents the total delay, where C_p is the parasitic capacitor of the inverter. The capacitor values are increased in binary increments. Since the output of the counter is also binary, the resulting delay differences between the delay steps becomes a constant value.

4.3.1.3. Transmitter Configuration. Transmitter configuration is done using 18 cascaded high speed DFF shift registers. These registers set the widths of the negative and positive Gaussian mono pulses and the delay between these pulses. The configuration is completed in 18 clock cycles. The simulation results of the configuration and output signals are shown in Figure 4.19. Shift registers include output buffers to prevent changing the register states due to kick-back noise of the MOS capacitors. The kick-back noise can clearly be seen in the simulations.

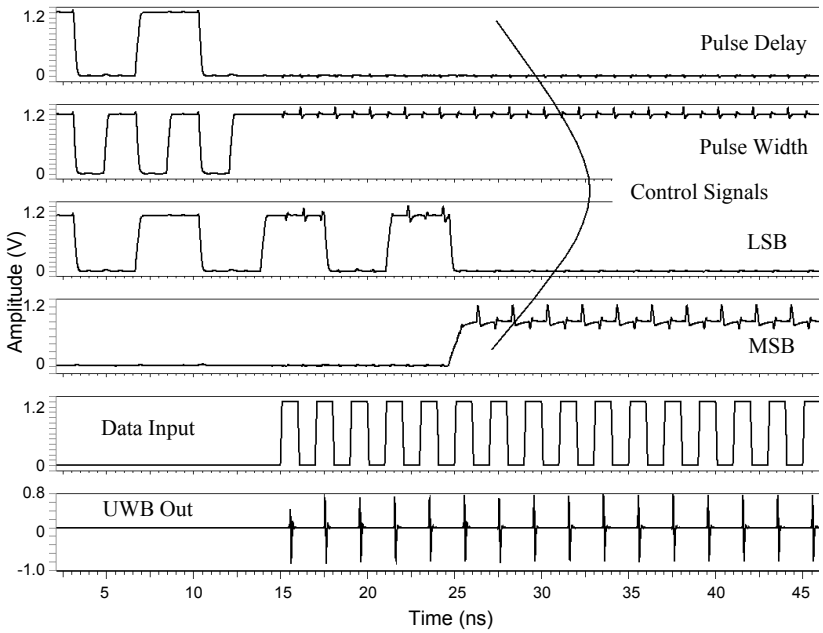

Figure 4.19. Simulation of configuration input signals and transmitter output.

4.3.2. Simulation Results

The corner simulations are performed to observe and alter the effects of the process variations. As a first step, the pulse width and delays are programmed according to standard typical-typical(TT) production. As can be seen from Figure 4.20, the maximum swing is obtained in TT case and center frequency of the TT signal is at 4 GHz in Figure 4.21. However, the chip can operate in the slow-slow (SS) corner case, where the center frequency is shifted to 3.56 GHz and that degrades the performance of the system. In this situation, the transmitter can be programmed to achieve the best performance SS corner case. As can be observed from the simulations in Figure 4.22, the transmitter is reprogrammed to have SS corner center frequency result as 4.02 GHz. The maximum voltage swing is now obtained in SS case as shown in Figure 4.23.

The output voltage swing can reach up to 1.3 Volts and the center frequency can be changed between from 2 GHz to 6 GHz. The output pulse shaping capacitor is fixed to 700 fF, which gives the best voltage swing of 1.3 V at the 4 GHz center frequency.

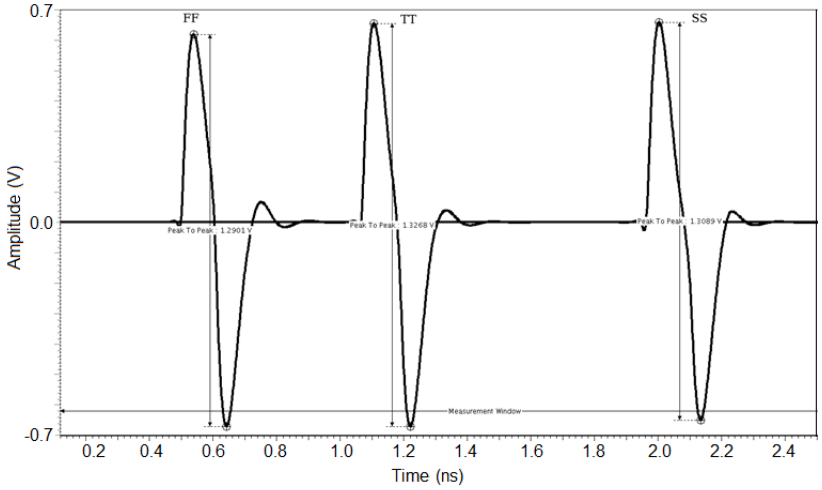

Figure 4.20. Time domain simulation of process variations.

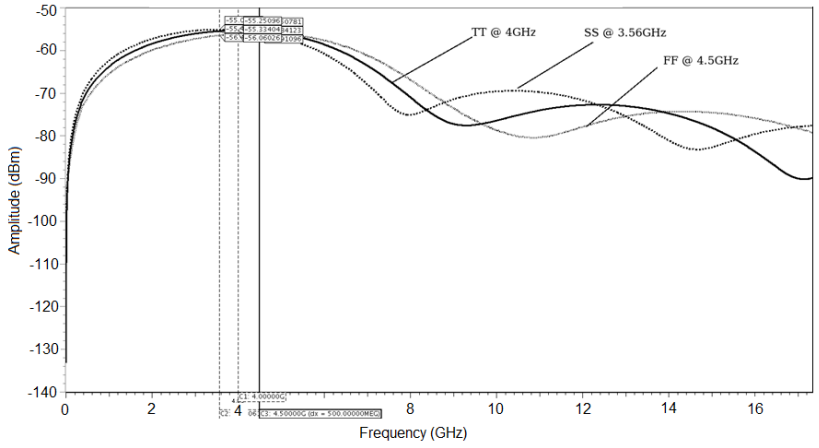

Figure 4.21. Frequency domain simulation of process variations.

4.3.3. Measurement Results and Discussion

The transmitter is manufactured using UMC MMRF 130 nm CMOS process. The micrograph of the fabricated IC is given in Figure 4.24. The core area of the design excluding the ESD protection is 0.03 mm^2. The design also includes the on-chip pulse shaping capacitor which eliminates external circuitry.

The configurability measurement results are listed in Table 4.3. The transmitter's center frequency can be changed from 500 MHz to 4.1 GHz. There are a few

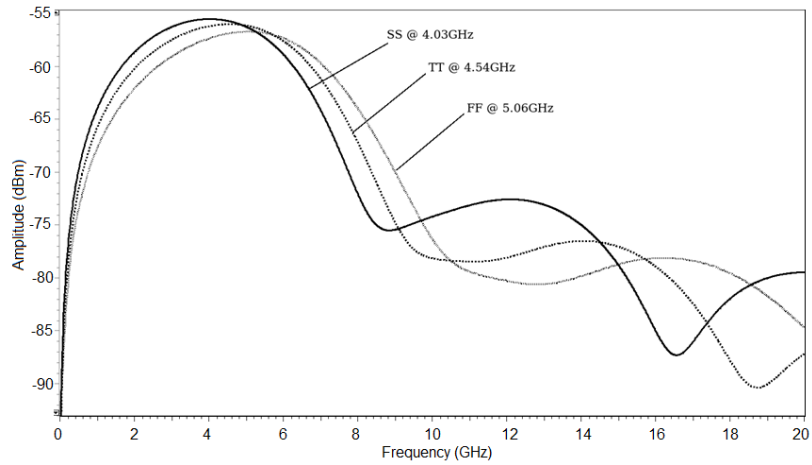

Figure 4.22. Frequency domain simulation of process variations.

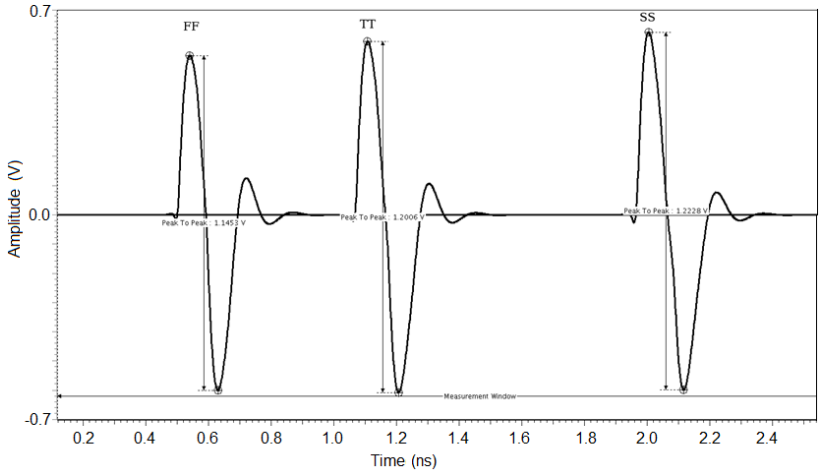

Figure 4.23. Time domain simulation of process variations.

dB difference on the amplitude level, which is caused by the on-chip pulse shaping capacitor. The static power consumption of the transmitter is 1.8 μW, that gives higher energy dissipation on lower PRF values. The power consumption is also higher at lower center frequencies. The load capacitor increases as the frequency decreases. Therefore, the dynamic power consumption and EPP increases as the center frequency decreases. The best EPP figure of the transmitter is achieved at 500 MHz PRF with 4.1 GHz center frequency.

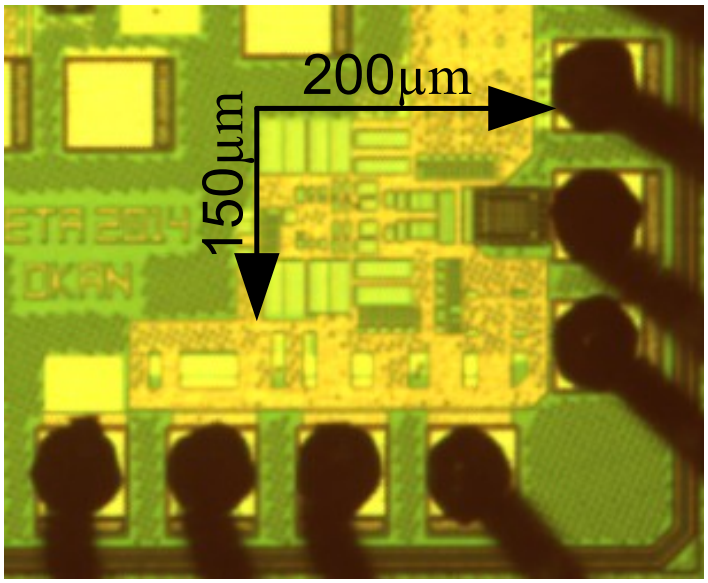

Figure 4.24. Transmitter micrograph.

The spectrum measurement results are given in Figure 4.25 and Figure 4.26. The configurations are changed to adjust the pulse width and hence the center frequency. As can be observed from the figures, the center frequency increases inversely proportional to the programmed word value, because the low word number configuration causes shorter pulse width. Therefore, the center frequency increases. Bandwidth also increases with the center frequency. There are harmonic peaks for the configuration of center frequencies that are lower than 2 GHz, because of the small on-chip pulse shaping capacitor value.

Performance comparison with the previous configurable transmitters are given in Table 4.4. Notice that, [82] can only be used at low data rate with a specific range. The configurability is only added for beam forming purposes. The center frequency can not be changed. On the other hand, [84] achieves good EPP performance and center frequency can be adjusted. However, the range of the center frequency only covers the 3.1-6 GHz band. Operation at the 0-960 MHz band is not possible. [83] has moderate EPP value and high data rate. However, the center frequency of [83] also does not cover the low frequency band and the pulse swing is very low, which limits the transmitter to very short range applications. On the other hand, [85] achieves 7.7 pJ/pulse performance with good efficiency using 65 nm CMOS process. But, only

Table 4.3. Configurability Measurements.

Word Count	Center Frequency (GHz)	Amp @100MHz PRF (dBm)	EPP @40MHz PRF (pJ/pulse)	EPP @200MHz PRF (pJ/pulse)	EPP @500MHz PRF (pJ/pulse)
15	4,10	-34.71	20,86	14,34	9,61
16	4,00	-37.39	20,92	16,23	10,42
28	3,00	-28.65	25,62	17,20	12,18
31	2,30	-28.41	26,08	17,51	12,30
47	2,00	-29.81	31,11	18,00	12,32
56	1,00	-29.28	33,86	20,19	12,40
63	0,50	-28.35	35,69	21,72	12,98

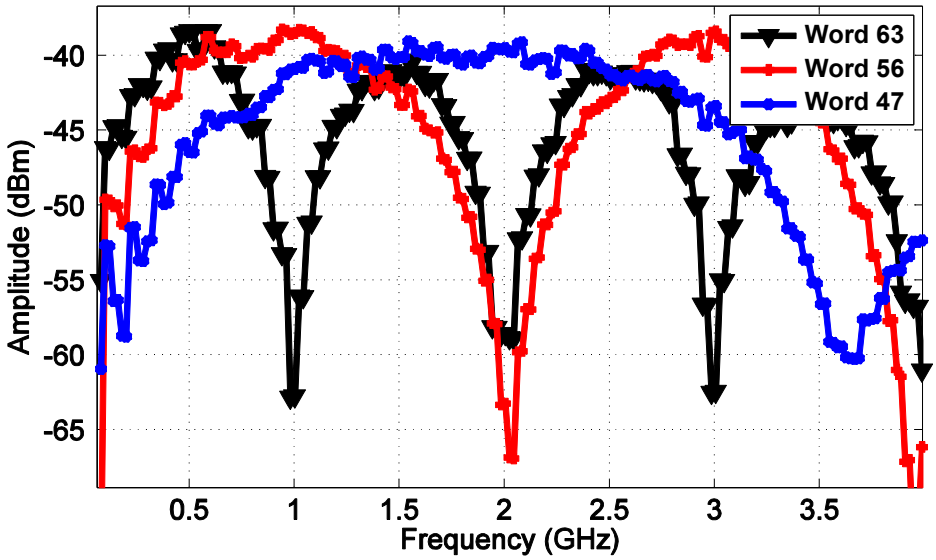

Figure 4.25. Measurements of 500MHz, 1GHz, and 2GHz configurations.

the bandwidth of the pulse can be adjusted. The proposed transmitter can precisely adjust both positive and negative pulse widths as well as the delay between the pulses. Therefore, the proposed transmitter not only has a reasonably good EPP performance but also operate with a wider center frequency range than previous state-of-the-art as demonstrated by extensive measurement results.

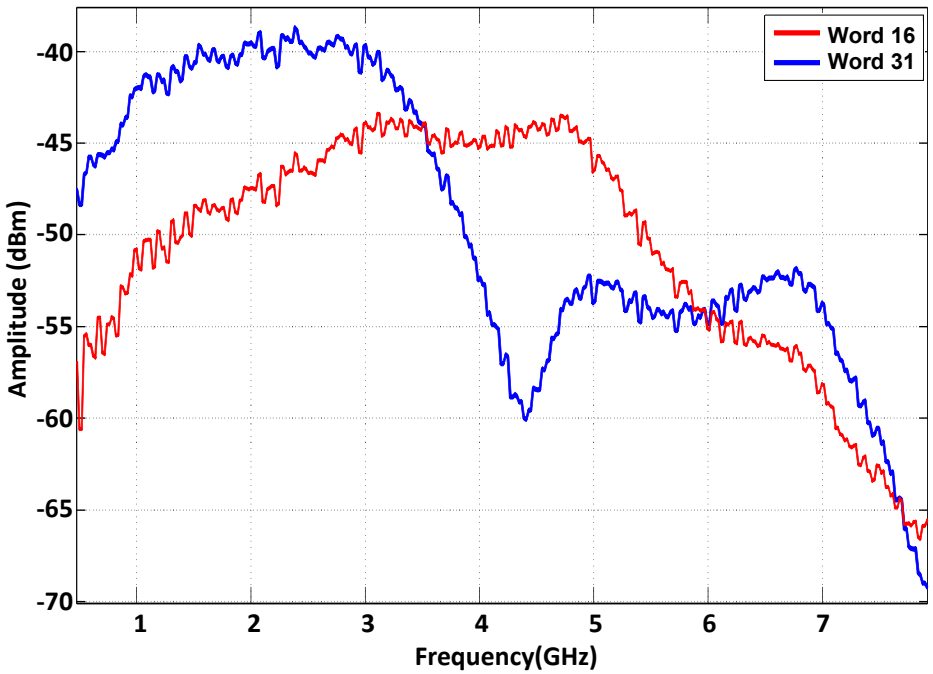

Figure 4.26. Measurements of 2.3 GHz and 4 GHz configurations.

Table 4.4. Performance Comparison with the Previous Work.

	[82]	[83]	[84]	[85]	**Our work**
Technology (nm)	130	180	90	65	130
Supply (Volts)	1.2	1.8	1.2	1.0	1.22
Active Area (mm^2)	-	0.045	0.08	0.32	0.03
PRF (MHz)	10-80	2500	0-500	32	0-600
EPP (pJ/pulse)	10	25	3.6-20	7.7	9.6-35.6
Conf. center freq.	No	Yes	Yes	No	Yes

4.4. Conclusion

Two ultra-low power transmitters are presented with dual-band and reconfigurability features. These designs have better performance in terms of energy efficiency and die area compared to the state-of-the-art.

The dual-band low-power IR-UWB transmitter operates in 0–960 MHz and 3.1–5 GHz bands. The transmitter employs a simple pulse generation and shaping architec-

ture, which lead to energy-efficient operation. The packaged transmitter chip leakage power is less than 2 μW. The energy consumptions per pulse for a PRF of 10 MHz in the 0–960 MHz and 3.1–5 GHz bands are 5.3 and 26.5 pJ/pulse, respectively. The 0–960 MHz and 3.1–5 GHz dual bands are successfully utilized by reconfiguration.

On the other hand, configurability is achieved with digitally programmable shunt capacitor delay lines in reconfigurable transmitter. Shift registers are used in order to configure the delay lines and minimize number of used pins. The transmitter is capable of achieving 500 MHz pulse repletion frequency (PRF) with 9.6 pJ/pulse performance. The transmitter's center frequency can be adjusted in a wide range from 500 MHz to 4.1 GHz. Although configurable transmitters are present in the literature, such flexible ultra-low power transmitters have not been presented before to the best of our knowledge.

5. VLSI DESIGNS OF IR-UWB RECEIVER

5.1. Introduction

IR-UWB receivers can be designed using coherent or non-coherent architectures. During the thesis, two non-coherent and a coherent design are fabricated in UMC 130MMRF technology. The first non-coherent design includes self-mixing and energy detection methods as well as an envelope detector. The second non-coherent design is the improved version of the first design in terms of performance. Therefore, in the following sections, these receivers are not differentiated as first and second design and the results of those of the second design. On the other hand, the coherent design is based on template based synchronization architecture. The measurements of the fabricated coherent receiver are underway. The following sections cover both receivers in detail, as well as a literature survey on IR-UWB receiver architectures.

5.1.1. Literature Overview of Receiver Architectures for IR-UWB

IR-UWB receivers are implemented in both coherent and non-coherent architectures. Notice that both systems are effective in short ranges due to the low-power requirement. However, coherent UWB systems are traditionally preferred in high data-rate applications, whereas non-coherent architectures are mostly used in low data-rate ones such as wireless sensor networks. In Figure 5.1, a general overview of the commonly used coherent and non-coherent IR-UWB receivers is presented. Notice from Figure 5.1a that a common coherent RF-to-baseband conversion method is to use the local oscillator directly in the mixer as given in [86].

This method simplifies the synchronization process but at the cost of increased power consumption. Another coherent receiver alternative is the template-based receiver shown in Figure 5.1b that uses the copy of the transmitted pulse shape at the mixer [87]. Despite its effectiveness, this system is also subject to added cost due to the pulse generation and timing operations. As can be seen from such examples, coherent

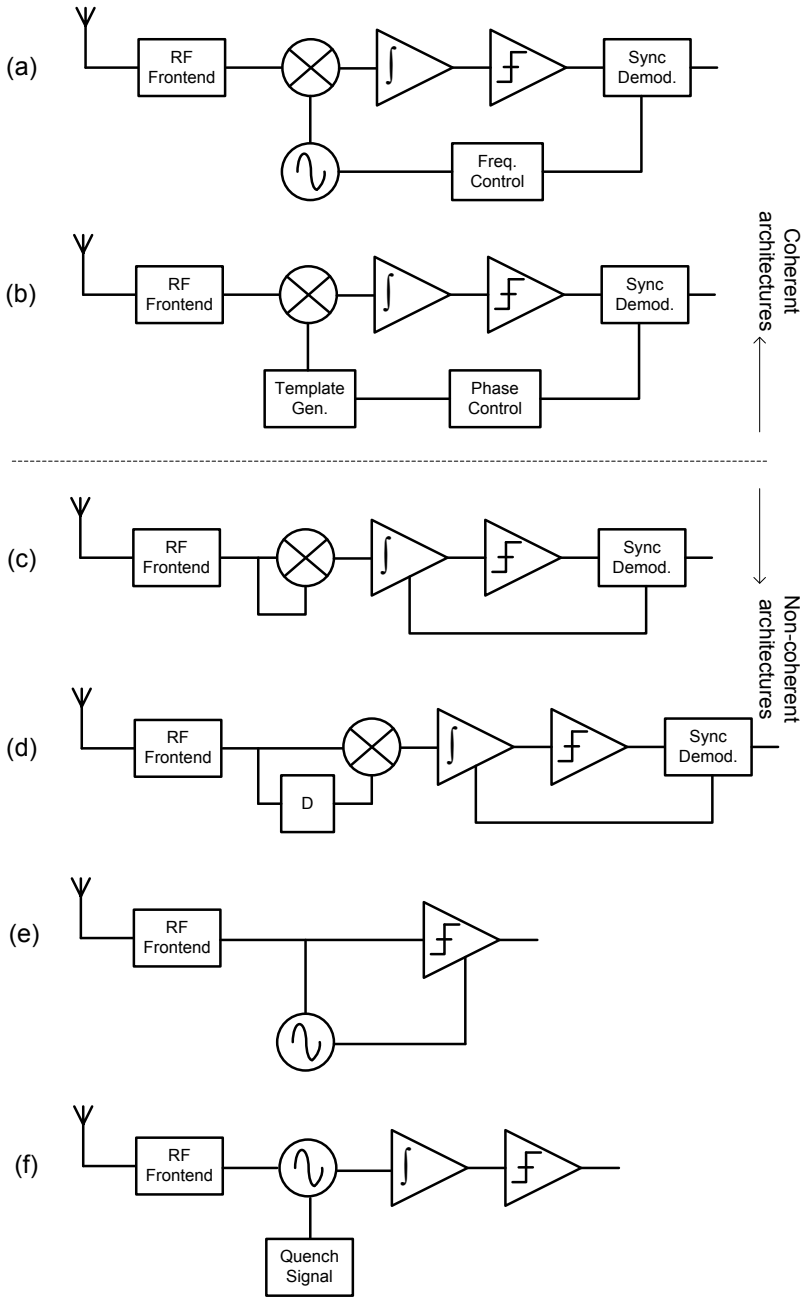

Figure 5.1. Receiver architectures for coherent and non-coherent IR-UWB; (a) Coherent clock synchronization, (b) Template pulse, (c) Energy detection, (d) Transmitted reference, (e) Injection locking, and (f) Super-regenerative.

UWB transceiver architectures can achieve high data-rates but usually at the expense of complex receiver-ends and continuous clock-operation at the mixer. Therefore a feasible alternative is to use non-coherent IR-UWB transmission.

As shown in [88] and depicted in Figure 5.1c, conventional non-coherent receivers employ amplifying, self-mixing, and energy detection blocks for reduced power consumption and simplified design. Alternatively, the transmitted reference method in Figure 5.1d can also be used where a delayed version of the received signal is correlated with itself. Other common alternatives include the injection locking method in Figure 5.1(e), super-regenerative receiver in Figure 5.1(f) or the combinations of the two [86], [89]. In general, non-coherent UWB transceivers can be implemented with lower complexities than their coherent counterparts but also at the expense of reduced data rates. That is why they are preferred for low-rate applications such as insect motion control [90], RFID [91], and wireless biomedical endoscopy sensors [92]. Exceptionally, as shown in [81], a non-coherent and high data-rate architecture can also be designed by combining large gain radio frequency (RF) stage with low-power energy detection. However, the rate increase in [81] comes at the expense of a compromise in the range that is at the order of centimetres, which is a limitation for practical applications.

5.2. Non-Coherent IR-UWB Receiver Design

A high data-rate low-power non-coherent IR-UWB transceiver architecture is designed with improved range capabilities. The receiver of the proposed non-coherent system employs a mixture of energy and envelope detection as shown in Figure 5.2. In addition, it uses a self-mixer that works as the squarer of the energy detection block. The demodulation operation is avoided by using baseband pre-amplifier and comparator blocks as an envelope detector, which simplifies the architecture and reduces the power consumption. All design blocks are outlined and a comparative analysis of the performance of the proposed architecture with respect to others in the literature are presented.

5.2.1. RF Front-End

A wideband FR4 patch antenna with band-pass characteristics is used. The first stage in the receiver is the 3-5 GHz off-chip RF balun to convert the single ended signal

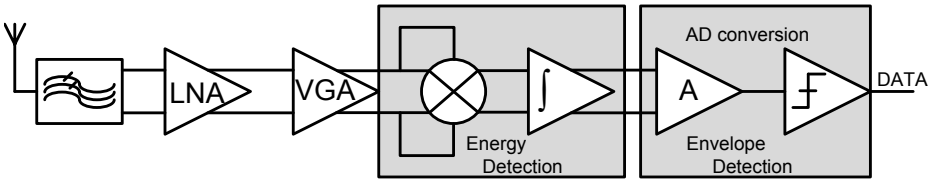

Figure 5.2. Non-coherent receiver block diagram.

to the differential one. Then, a differential common source inductive peaking cascode low noise amplifier (LNA) is used at the receiver chip. The LNA is co-designed with the 800 V electro-static discharge (ESD) circuit using human body model (HBM) [93]. The effect of the input pad capacitance of the chip is also included in the design and simulations.

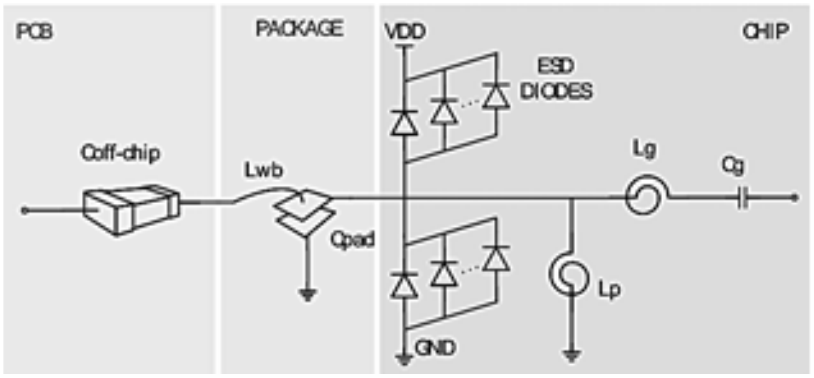

Figure 5.3. 3rd order Chebyshev BPF network.

The matching between the LNA and balun becomes critical since ESD brings additional capacitor and noise to the system together with the pad capacitance. Therefore, the ESD diodes, RF-PADs, and wire bond inductors are used as parts of a third order Chebyshev BPF that also acts as a matching circuit. Additional capacitor and inductors are added as depicted in Figure 5.3. The wire-bond and the air-cavity 48-pin quad-flat-pack no-lead (QFN48) package model of [94] are also included in the simulation to model the parasitic effects realistically. The LNA is drawn at the symmetrical center of the chip edge to reduce the difference in the differential wire bond inputs.

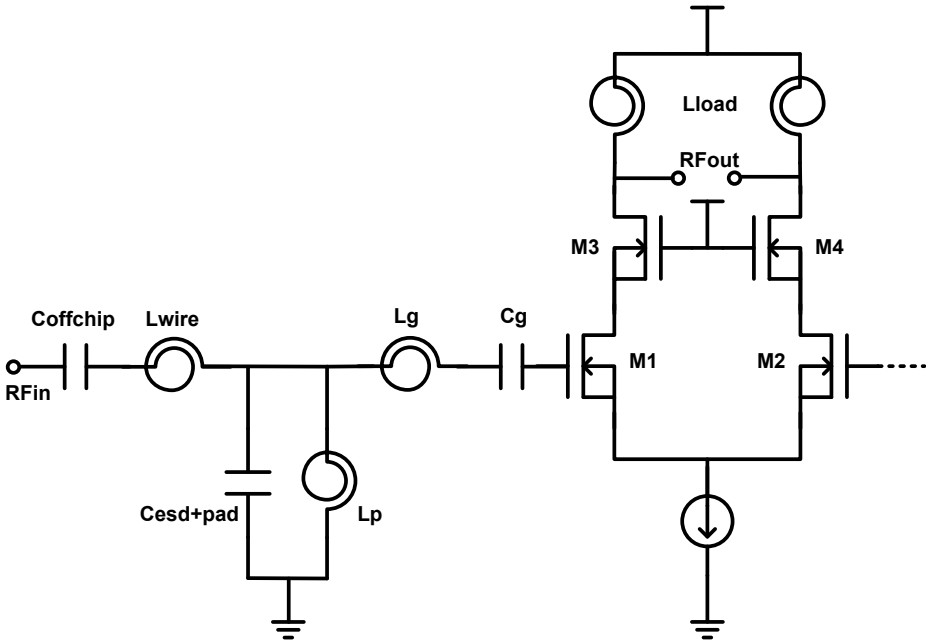

Figure 5.4. Cascode LNA schematic with matching network.

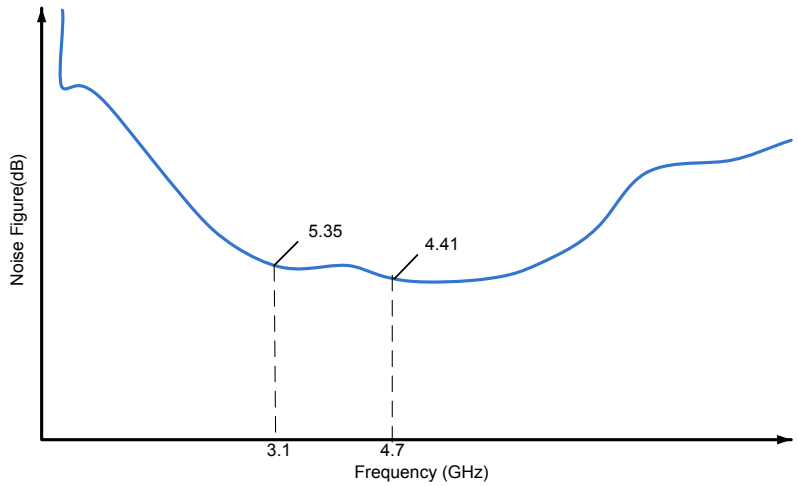

Figure 5.5. LNA noise figure circuit simulation.

The NF is the most important parameter of the LNA. The inductors and ESD capacitors contribute to noise figure. The schematic and layout simulations differ because of the parasitics that are introduced by these large passive elements. The schematic and post-layout simulations are given in Figure 5.5 and Figure 5.6. The matching is also another critical parameter to minimize the reflection on high data

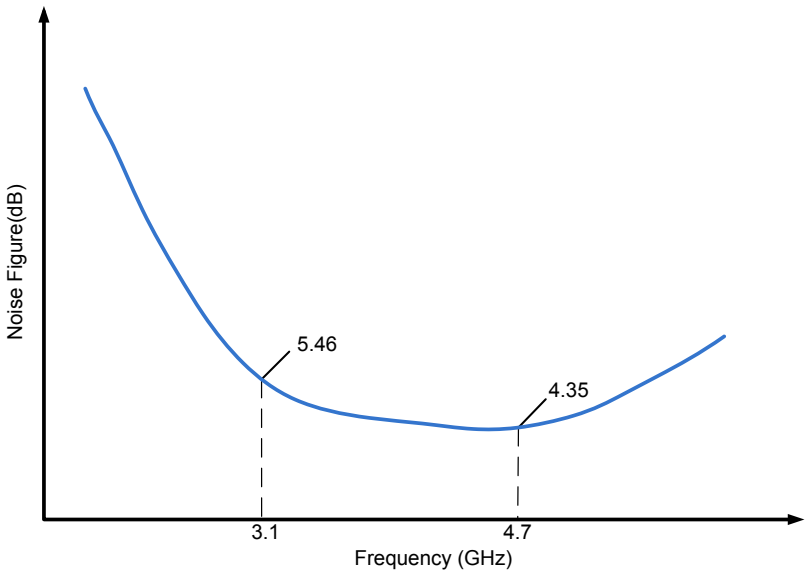

Figure 5.6. LNA noise figure layout simulation.

rate reception. The schematic and post-layout simulations of reflection has a large variation because of the parasitics introduced by the matching network as can be observed in Figure 5.7 and Figure 5.8. The NF and the matching requirements cannot be satisfied simultaneously. Therefore, an optimum point between NF and matching criteria is determined. The inductor and capacitor parasitics after the layout affect the NF and reflection parameters. Therefore, the design is modified after post layout simulations. The NF varies between 4.3 dB and 5.5 dB in the 3-5 GHz band and the reflection coefficient is found to be less than -7 dB in post-layout simulations.

The LNA block is followed by a 5-stage variable gain amplifier (VGA) with active load that is shown in Figure 5.9. 1 pF coupling capacitors are used between VGA stages to remove the DC offset. The total gain including the LNA before mixer is 57 dB(Figure 5.10). The front-end gain can be varied between -30 dB and 57 dB.

5.2.2. Energy Detector

The squarer and integrator form the energy detection block. In Figure 5.11a, an active-loaded double-balanced Gilbert cell is used as the self-mixing squarer. Because

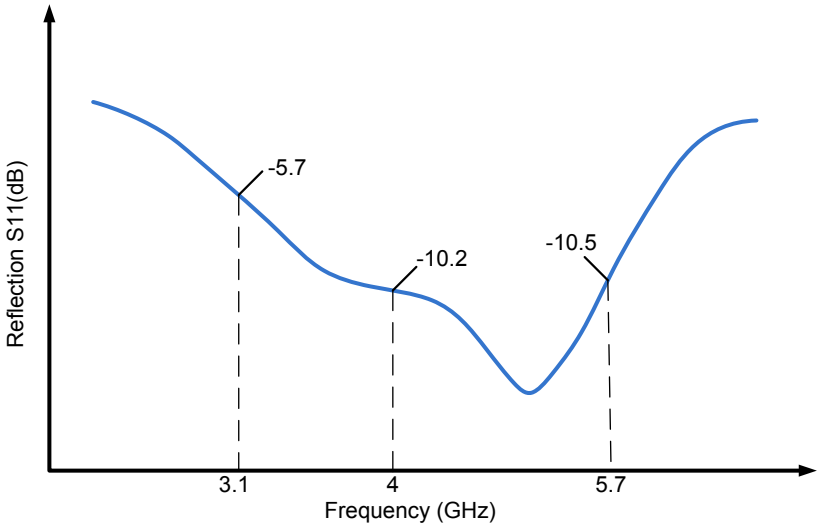

Figure 5.7. LNA input reflection schematic simulation.

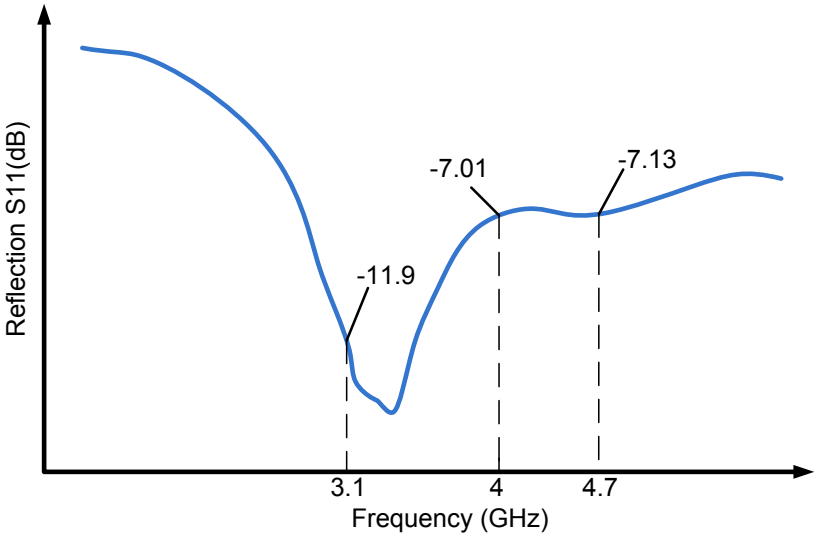

Figure 5.8. LNA input reflection layout simulation.

of the energy detection and the self-mixing of the low-power incoming signal, the linearity becomes a less important design consideration. The sensitivity of the squarer affects the overall system performance. Therefore, power consumption limitation is relaxed in the mixer stage to increase the RF-DC gain that determines the sensitivity of the system.

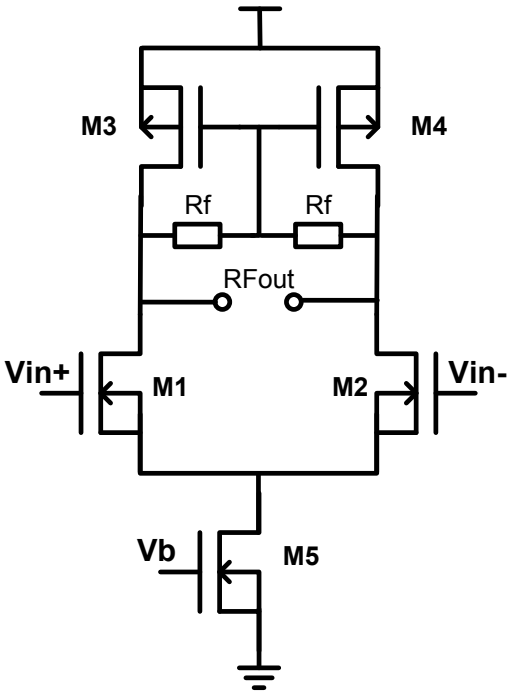

Figure 5.9. Active loaded VGA schematic.

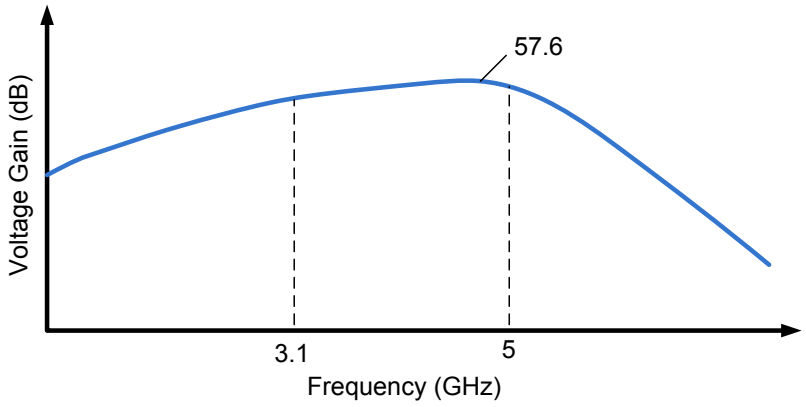

Figure 5.10. RF frontend voltage gain.

A single stage $g_m - C$ integrator that can be seen in Figure 5.11b is used at the energy detector. To achieve high data-rate operation without altering the integration operation, the capacitor value is limited to 400 fF. There is also an additional cascode stage to control the integration window. However, the integration is always kept active to achieve high data rates.

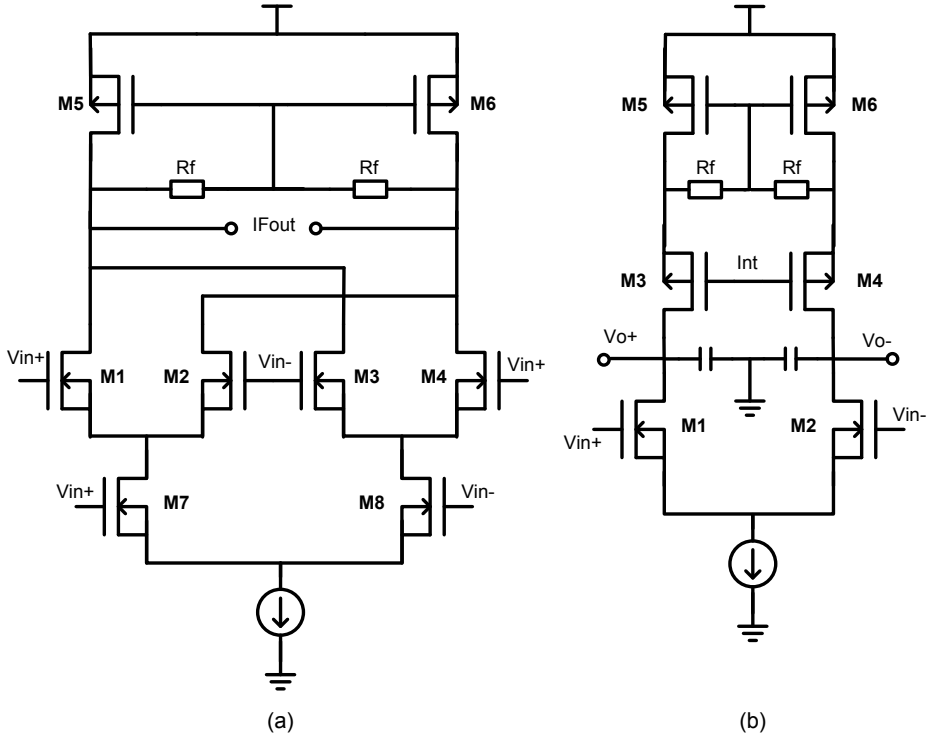

Figure 5.11. Energy detector; (a) Double balanced mixer, and (b) GmC integrator.

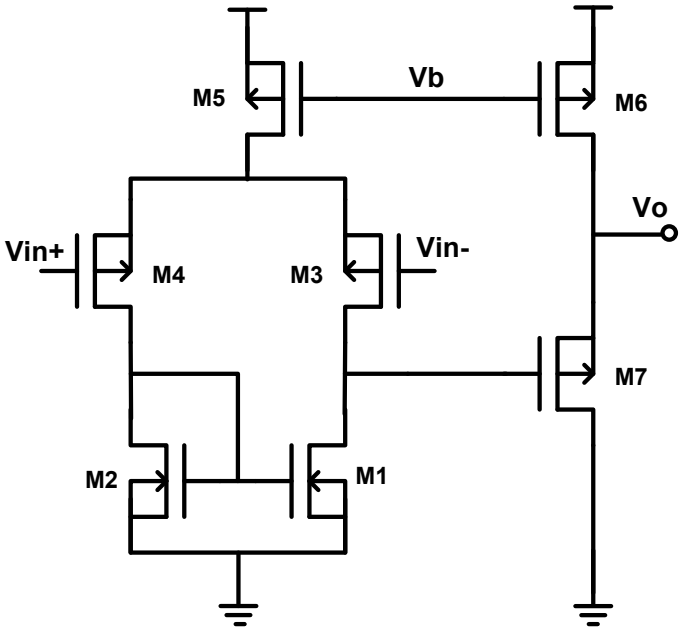

Figure 5.12. Pre-amplifier stage.

5.2.3. Baseband Blocks

The integrator is followed by the pre-amplifier and comparator stages. Signal level at the output of the energy detector is small for analog-to-digital conversion. That is why it is amplified before the comparator. An additional single ended pre-amplifier stage improves the sensitivity of the system. The output stage comprising the transistors $M6\&M7$ provides additional gain before the comparator as seen in Figure 5.12. The pre-amplifier is followed by a hysteresis comparator. The hysteresis is included to prevent the system from generating false outputs due to noise at the cost of a slight sensitivity loss. Therefore, in order not to affect the envelope detection and thus system performance, the hysteresis is set to a small value.

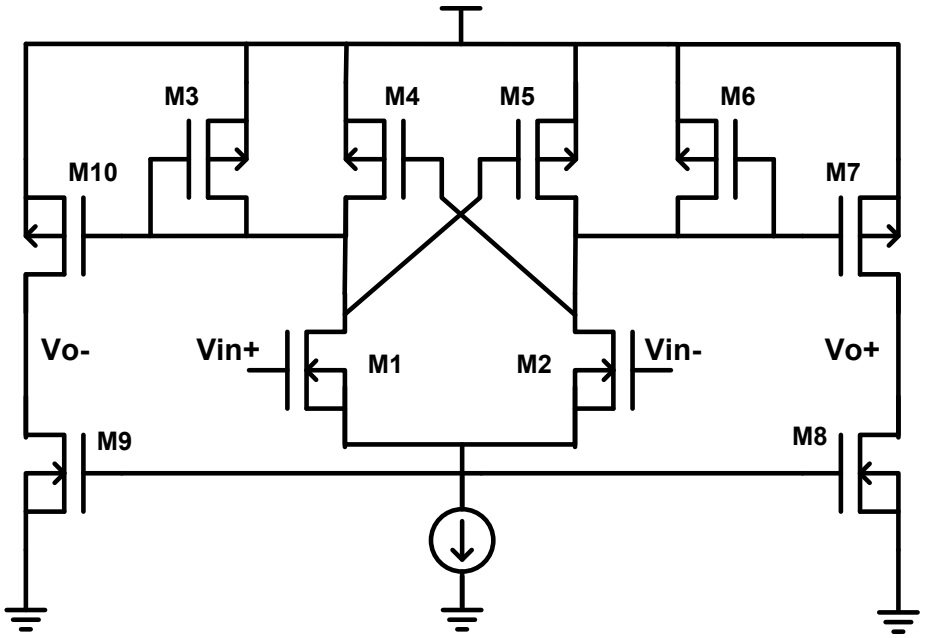

Figure 5.13. Comparator with hysteresis.

Envelope detection is done at the baseband blocks; the pre-amplifier comparator combination acts as an envelope detector as well as a analog to digital converter. It is achieved by slowing down the response time of the ADC. The 480 MHz clock used at the transmitter forms an envelope around the OOK signal in the ADC stage. The comparator in Figure 5.13 then digitizes the envelope output.

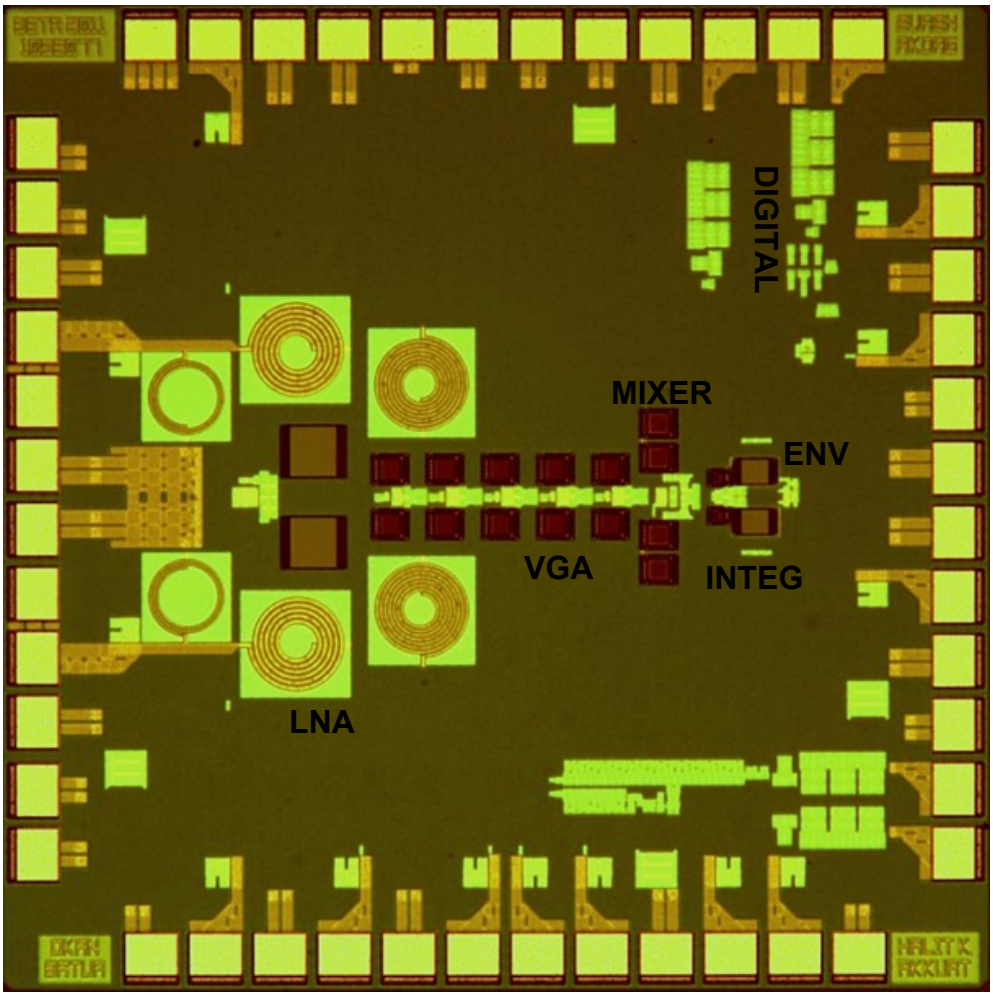

Figure 5.14. Receiver micrograph.

5.2.4. Non-Coherent Receiver Simulations

The receiver simulations are performed with UWB multipath channel, impulsive noise and AWGN models. The robustness against impulsive noise is achieved by receiver's on-chip BPF that works as a clipper. High impulses' energy is clipped by the BPF and wrong signal detection is prevented. The simulation results are given in Figure 5.15, Figure 5.16 and Figure 5.17.

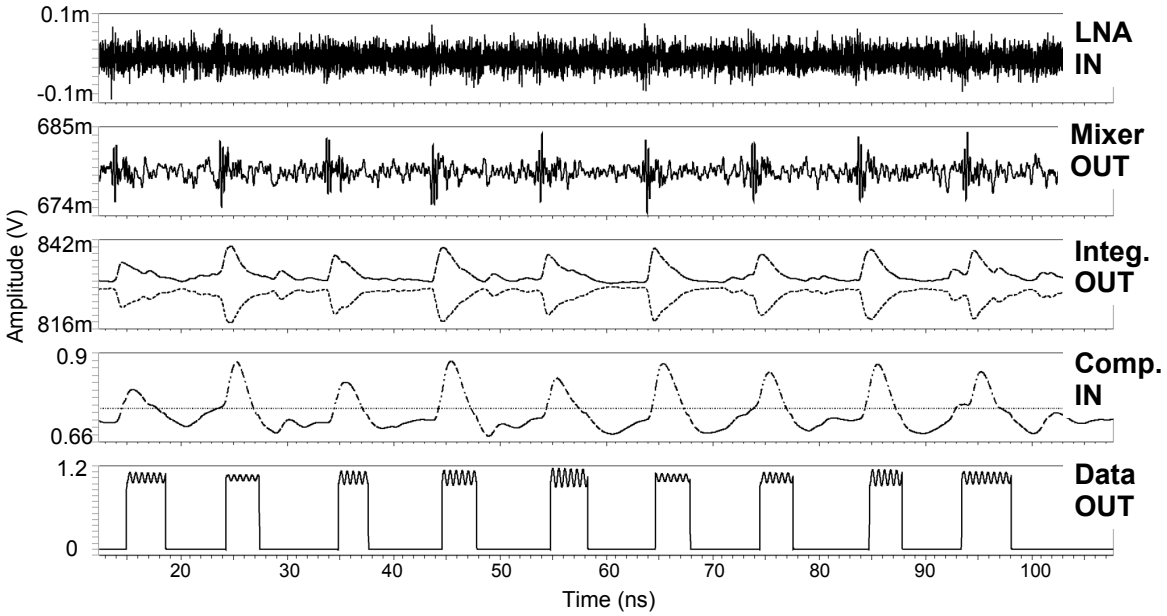

Figure 5.15. Receiver simulations.

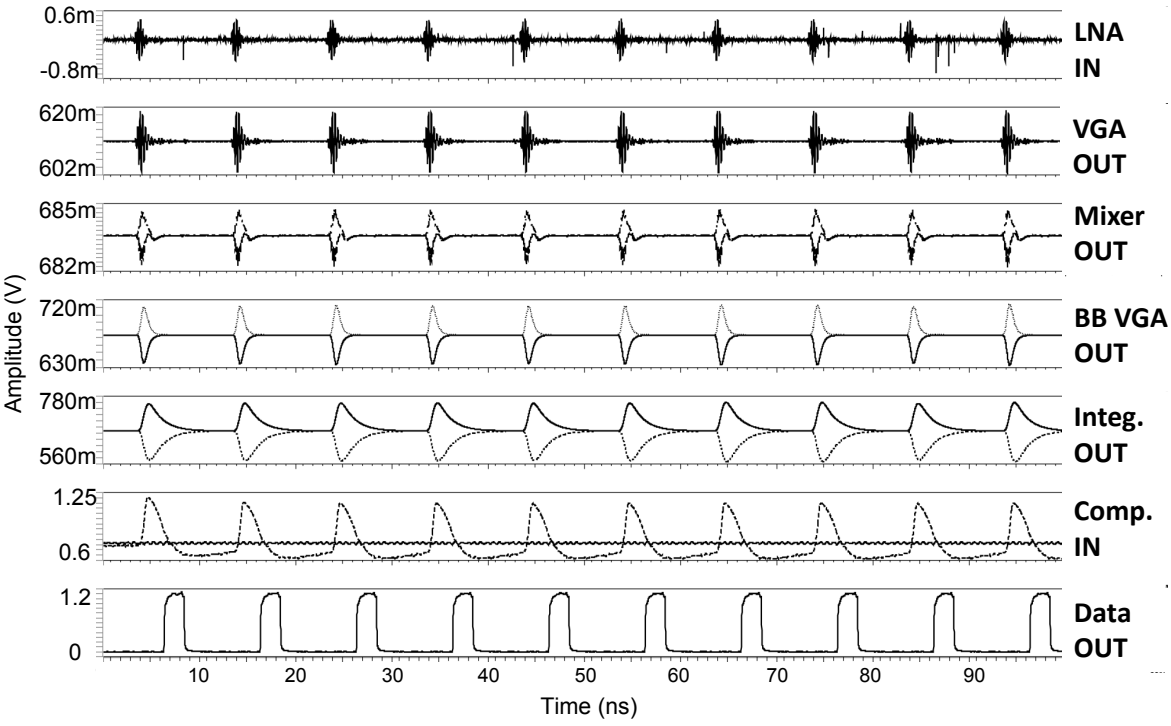

Figure 5.16. Low intensity impulsive noise system simulations.

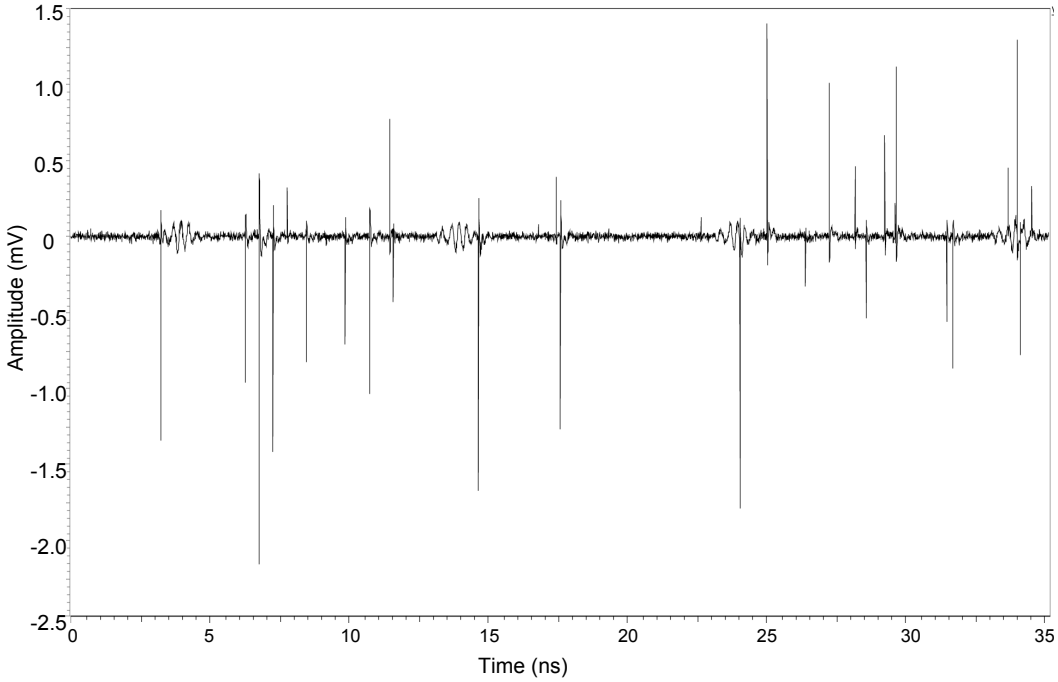

Figure 5.17. High intensity impulsive noise.

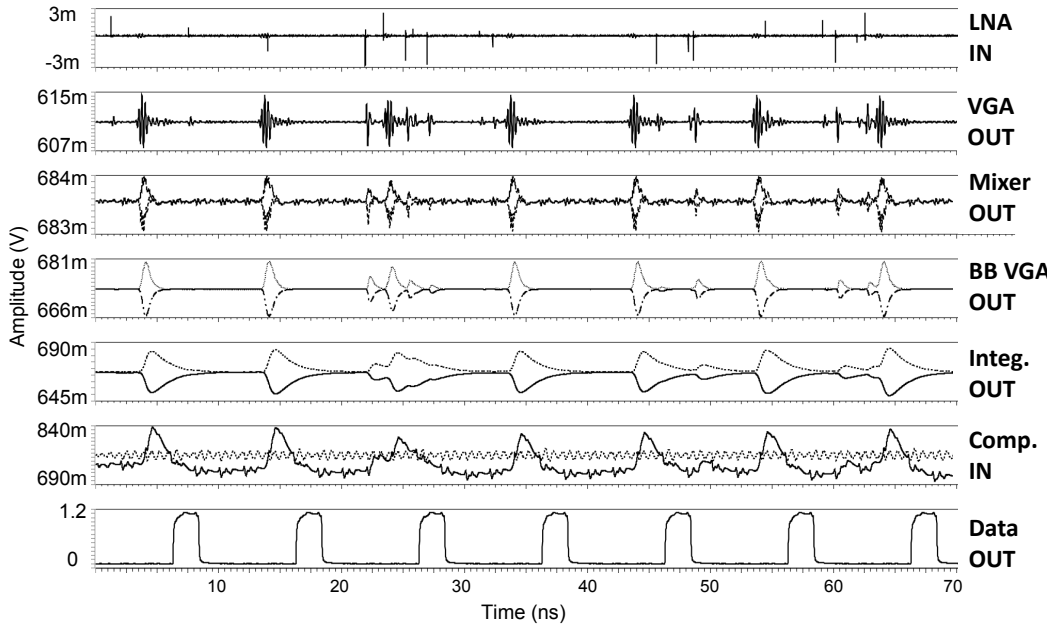

Figure 5.18. High intensity impulsive noise system simulations.

5.2.5. Measurement Results

The receiver is manufactured using the UMC MMRF 130-nm CMOS process and can be seen in Figure 5.14. The receiver uses a 1 mm^2 die area while the transmitter

occupies only 0.1 mm^2. The measurements are taken from the packaged chip on a designed coplanar-waveguide RF PCB with an FR-4 substrate using SMA connectors. A 3.2-5 GHz PCB patch antenna design is used for the transceiver measurements. The receiver with dual-band transmitter design is capable of communication up to 1 meter at 240 Mbps with the power consumption of 48.6 mW, which translates to 0.2 nJ/bit.

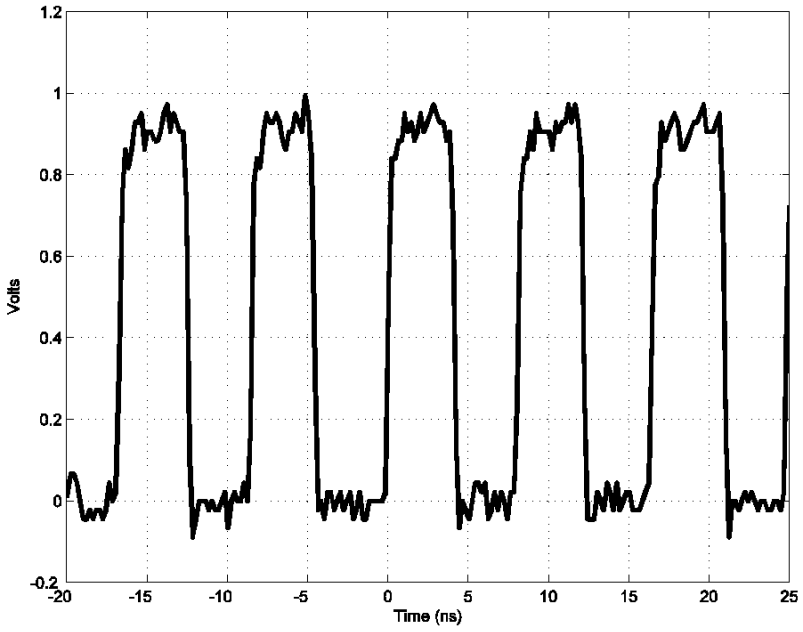

Figure 5.19. 120 MHz clock reception measurement result.

Measurement results of the receiver are given in Figure 5.19. 120 MHz square wave is successfully received which corresponds to 240 Mbps data-rate over 1 meter. Transceiver performance and comparison parameters with the other non-coherent and coherent architectures in the literature are summarized in Table 5.1 . It is well known that non-coherent architectures are more suitable for low data rate medium range communication. However, it is observed that, a few coherent architectures can perform as well as non-coherent architectures at low data rates in the same power budget. It can also be observed from the table that the non-coherent architectures are using data rates as low as 100 kbps resulting in comparable energy per bit (EPB) performance with some of the coherent architectures.

The EPB vs. data-rate comparison is given in Figure 5.20. The low power

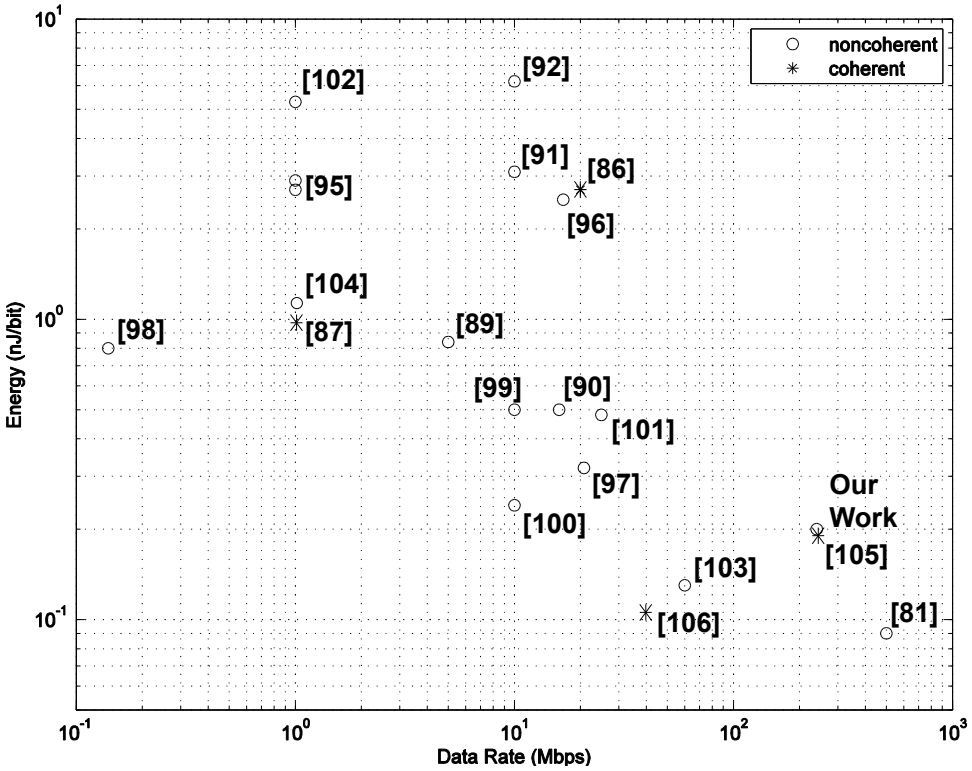

Figure 5.20. EPB vs data rate comparison.

non-coherent architecture is also suitable for short range and high data rate communication. It also shows similar performance with the coherent counterparts with reduced complexity.

There are few studies that achieve high data rate using non-coherent architectures [81], [103]. The receiver in [81], uses low RF gain, which results in 10 cm communication range. In our work, most of the power is consumed in RF 55 dB amplification stage which includes LNA and 5 stage VGA. Thus, 240 Mbps data rate is achieved over 1 meter distance which is more suitable for applications such as body area networks and short range cable replacement. Additionally, only post-layout simulation results are given in [103], which do not yield to a fair comparison for range and EPB.

Most non-coherent architectures in the literature are designed for low data-rate applications below 20 Mbps. The method of using envelope detector together with the energy detector is introduced and the clocking circuitry is avoided which makes it

Table 5.1. Performance Comparison.

Refs	**f-band (GHz)**	**Data (Mbps)**	**EPB (nJ)**	**Sens. (dBm)**	**Mod.**	**Tech. (nm)**	**Coh. ?**
Prop.	3-5	240	0.2	-104 @100 kHz	OOK	130	No
[**89**]	7.28-8.5	5	0.84	-70	PPM	130	No
[**90**]	3.4-4.4	16	0.5-1.4	-76	OOK, PPM	90	No
[**91**]	3.1-5	10	3.1	-70	OOK	180	No
[**92**]	3-5	10	6.2	-79	OOK	180	No
[**81**]	3.1-5	500	0.09	-	OOK	90	No
[**95**]	3.6-4.3	1	2.9/3.9	-60/-66	S-OOK	90	No
[**96**]	3.1-5	16.7	2.5	-99 @100 kHz	PPM	90	No
[**97**]	4.5-5.5	20.8	0.32	-70	OOK	130	No
[**98**]	3.5,4.5	0.14	0.8	-85	OOK	90	No
[**99**]	3-5	10	0.5	-79	OOK, PPM	90	No
[**100**]	3.5,4	10	0.24	-66/-61	OOK	180	No
[**101**]	3-4	25	0.48	-82 @1 MHz	OOK	130	No
[**102**]	3.4-4.5	20	5.3	-82	OOK-BPSK	180	No
[**103**]	3.5-4.5	60	0.13	-	OOK	180	No
[**104**]	4-5	1	1.1	-78	BPSK	130	No
[**86**]	3.1-3.9	20	2.7-4.95	-84 @4 MHz	Chirp	180	Yes
[**87**]	0.25-0.5	1	1	-	OOK	180	Yes
[**105**]	3-10	250	0.19	-	OOK	180	Yes
[**106**]	0-0.96	39	0.108	-55	BPSK	130	Yes

possible to achieve high data rate circuitry with a non-coherent architecture in short range applications. In our work, 240 Mbps data rate is achieved with 0.2 nJ/bit power consumption over 1 m range. To the best of our knowledge, this makes the receiver unique in the literature.

5.2.6. Wireless Ethernet Downlink Tests

Ethernet has different modes of operation; 10Mbps, 100Mbps, and 1Gbps. In the 100Mbps mode, ethernet signals are modulated by Manchester coding, where there are 3 levels of logic signaling to reduce electromagnetic radiation. The 1Gbps mode also uses similar coding. However, 10Mbps mode uses NRZ coding and it has 2 levels, which is suitable to be used at the data input of the transmitter. A DC offset is added to NRZ to convert it to digital logic levels. 10 Mbps ethernet data is sampled with 50MHz clock signal at the OOK input of the transmitter. The normalized Ethernet signal with UWB pulse output measurements can be observed in Figure 5.21.

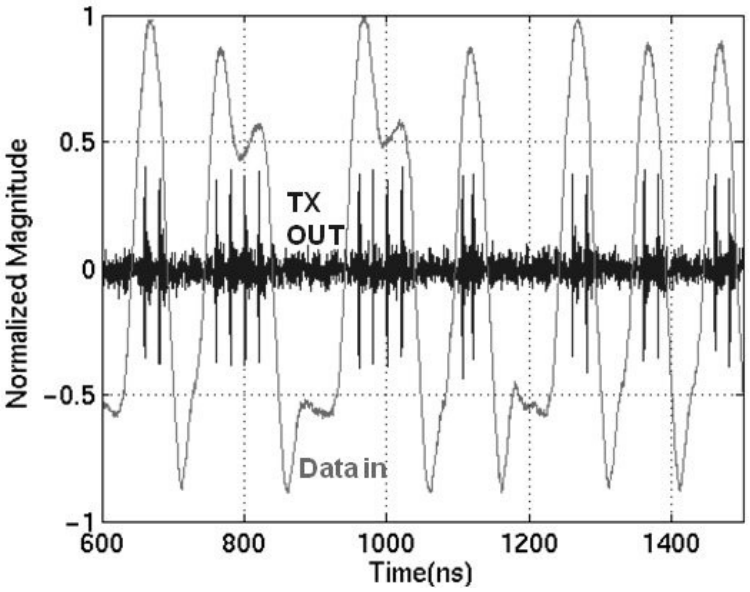

Figure 5.21. Ethernet signal and transmitter output.

The ethernet input of the transmitter and corresponding receiver outputs are given in Figure 5.22 and Figure 5.23. It can be seen from the figures that the ethernet signal is successfully received. Two laptops are cross connected using designed IR-UWB wireless transceiver. A 480p resolution movie was successfully streamed. Higher data rate streaming is only possible with 100 Mbps or higher ethernet connection speed, which requires additional circuitry for decoding the modulated signals to binary logic.

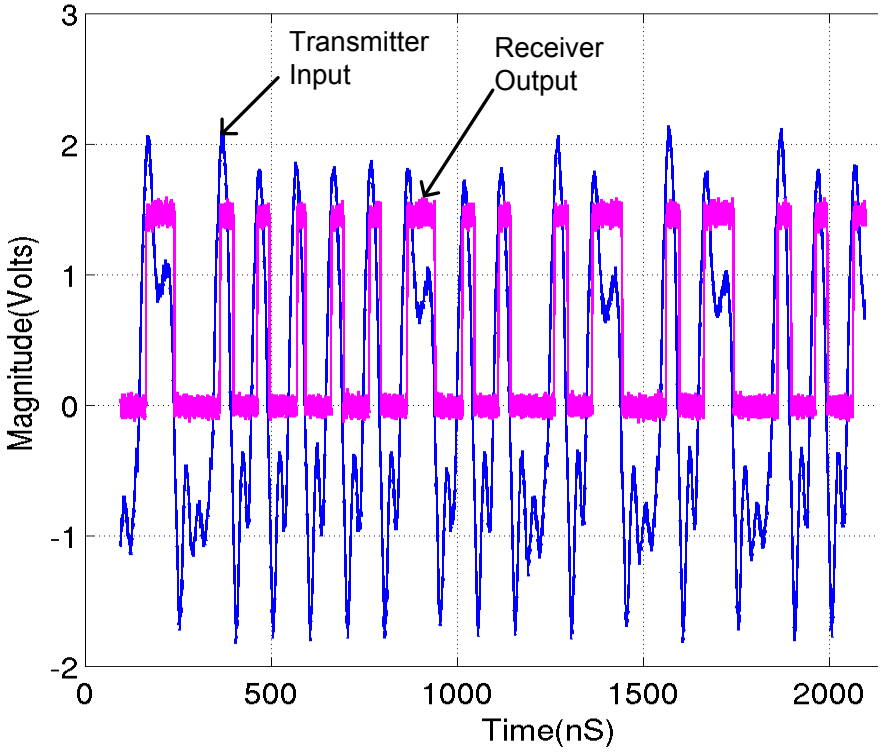

Figure 5.22. Wireless Ethernet tests at 1 meter distance.

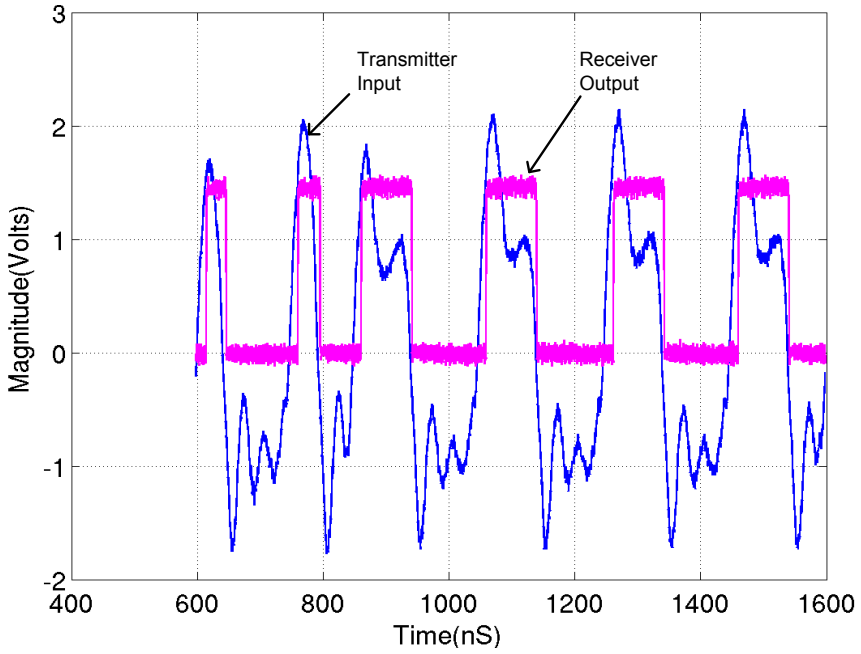

Figure 5.23. Wireless Ethernet test at 1 meter distance.

5.2.7. Synchronization Free Noncoherent OOK IR-UWB Demodulation Techniques

The synchronization of sub-nanosecond IR-UWB pulses is a challenging task for a non-coherent receiver. It requires complex synchronization time domain search algorithms. Furthermore, these algorithms are generally synthesized on chip to avoid synchronization delay problems. This methodology generally brings large area [107] and high power consumption costs. However, there are some digital methods present in the literature that simplify the this problem by employing baseband synchronization and demodulation techniques. Frequency shift keying (FSK) and OOK modulation is combined in [108] to address this problem. FSK-OOK method requires specific modulation and demodulation circuitry both at the transmitter and the receiver side. Another method is presented in [109], where synchronized on-off keying (S-OOK) approach is used by embedding the synchronization information at the transmitted data to construct a simple digital circuit to extract the clock and data signals for low data rate communication [109]. Self-synchronization architecture is presented in [82] by utilizing pulsed control oscillators (PCO) with 150 kbps data rate.

Previous methods in the literature either require high power or they operate only at low data rates as discussed above. In our work, we present three novel and simple methods to solve the demodulation problem by avoiding synchronization. The proposed methods require small area and low power consumption, while achieving very high data rates compared to those in the literature. Two of the proposed methods are implemented in 130 nm CMOS technology and successfully tested. Additionally, the high frequency sampling technique shows good post-layout results.

OOK IR-UWB pulses can be demodulated using digital logic circuit blocks at the baseband without a need for an additional synchronization circuitry. Smaller technologies favour the use of digital circuitry; hence, such approaches tend to become more advantageous in terms of area and power with every new technology. In this section, three different high data rate OOK demodulator designs and their performance are discussed. The following sections give details about the designs together with the

simulation and measurement results.

5.2.7.1. Digital envelope detector. The design is based on pulse stretching technique. The falling edge of the digital signal is stretched using the circuity in Figure 5.24. Therefore, consecutive pulses are merged. Thus, the envelope of the digital data is obtained. This operation is possible for both low and high data rate signals. However, the sampling rate must be kept high, so that the pulses are placed closely enough to achieve envelope detection operation. The overall circuit is composed of 4 inverters and a capacitor. 3 inverters are used for buffering, and the last inverter is utilized as the pulse stretcher. It has a long channel and slow NMOS transistor with 200 fF load capacitor, which delays the falling edge of the OOK data. Simulation results can be observed in Figure 5.25.

The envelope detector is designed to work with sampling rates in the range of 400 MHz to 800 MHz. This range is selected to enable very high data rate operation. 600 Mbps data rate is achieved with this circuitry. The envelope detector also works well at low data rates.

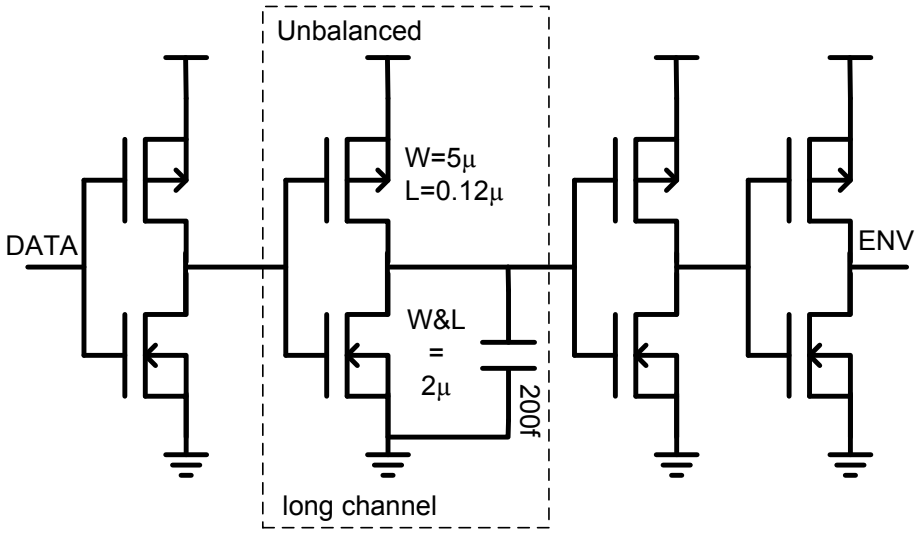

Figure 5.24. Digital envelope detector circuit.

The core area of the design excluding the electro-static discharge (ESD) protection and output buffers is 324 μ m^2. The measurement results show that the total

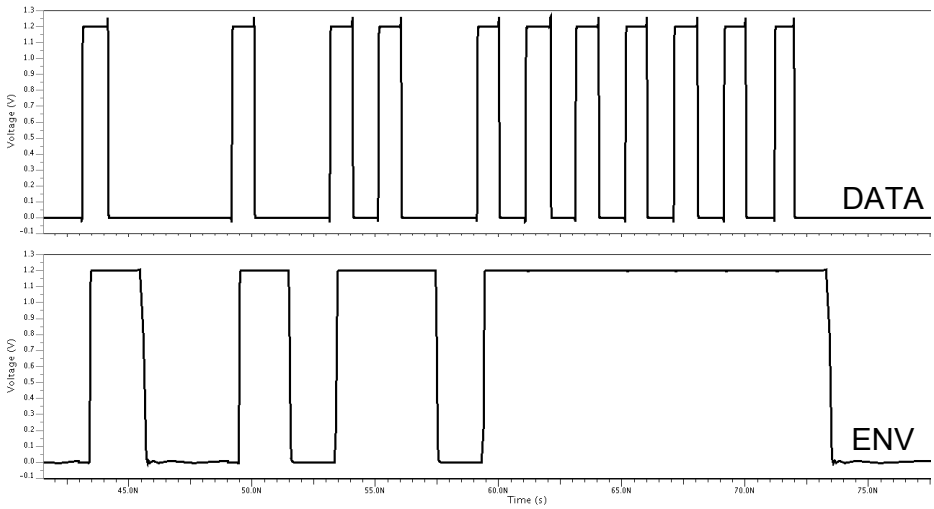

Figure 5.25. Envelope detector simulations.

current drawn from the 0.9 V supply circuit including the pad driver buffer changes between 2.21 mA and 2.33 mA depending on the sampling clock used at the transmitter. Simulation results indicate that around 60% of the power is used to drive the pads, thus yielding an estimate of 1.2 mW for the actual envelope detector. Measurement results for 50 Mbps reception can be seen in Figure 5.26.

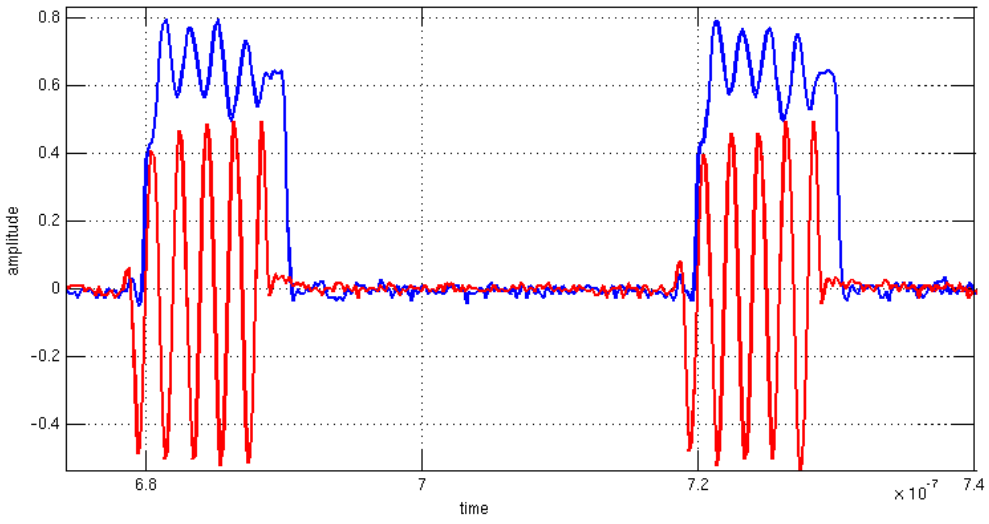

Figure 5.26. Digital envelope detector measurement results at 50 Mbps.

5.2.7.2. Self-correlator. OOK demodulation is commonly utilized in UWB receivers, because the OOK circuitry is less complicated compared to binary phase shift keying (BPSK) and pulse position modulation (PPM) demodulator blocks. A single edge

triggered D type flip-flop (DFF) is used to demodulate the OOK data with a synchronized clock signal. However, the usage of a synchronized clock signal can easily be avoided.

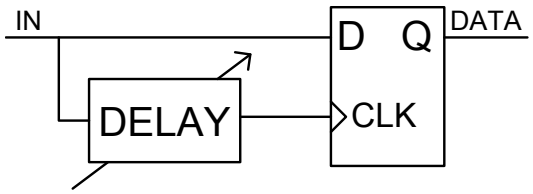

Figure 5.27. Self-correlator schematic.

In our work, the DFF is modified and it is used with an additional delay element that is connected to the clock input of the DFF. The clock input is the delayed version of the data input as shown in Figure 5.27. Therefore, the data signal is correlated with itself using a DFF. The self-correlation operation results in reduction on the duty cycle of the received signal. Thus, it limits the data rate of the demodulated OOK signal. The data rate depends on the sampling clock utilized at the transmitter. 100 Mbps is achieved with this circuitry. The core area of the design excluding the ESD protection and output buffers is 0.58 mm^2.

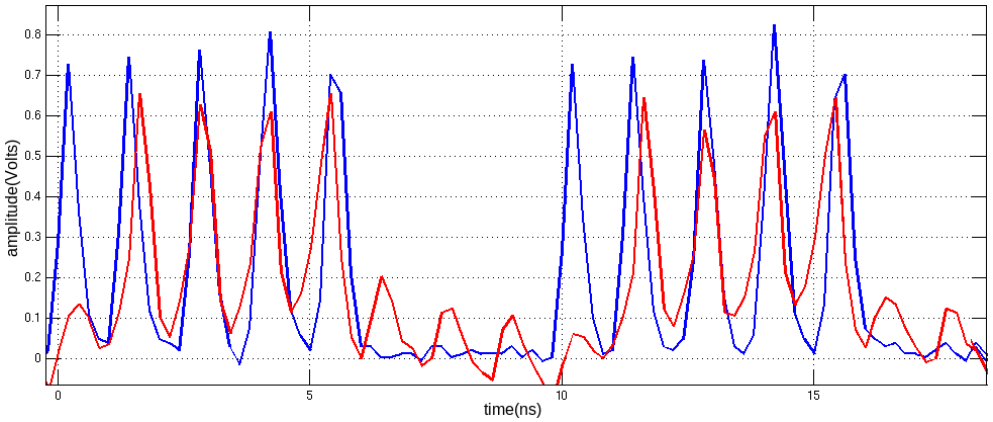

Figure 5.28. Self correlation signals at 200 Mbps.

Measurements of the self correlation signals can be seen in Figure 5.28. 200 Mbps data is sampled with 800 MHz clock at the transmitter. Measurements are performed for different data rates. Measurement results for 10 Mbps and 100 Mbps self correlation demodulation signals can be observed in Figure 5.29 and Figure 5.30.

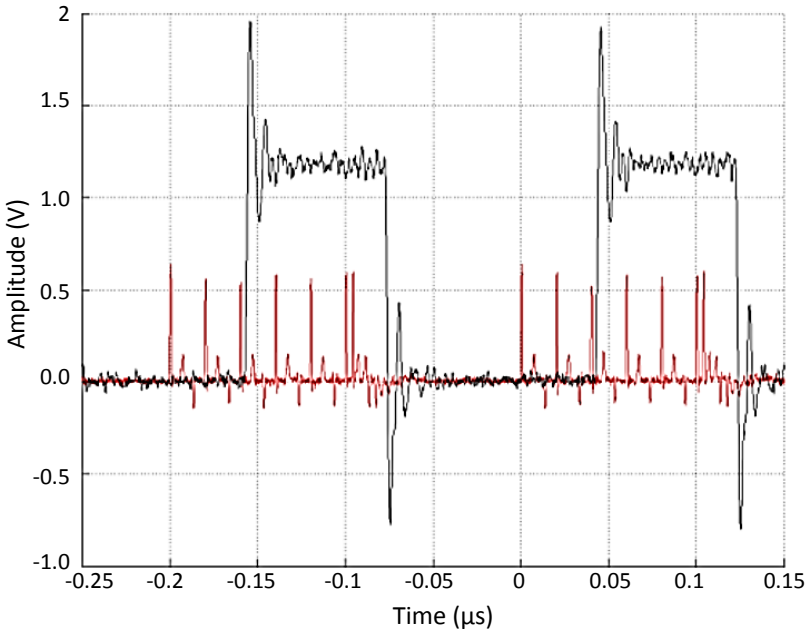

Figure 5.29. Self correlator measurements at 10 Mbps.

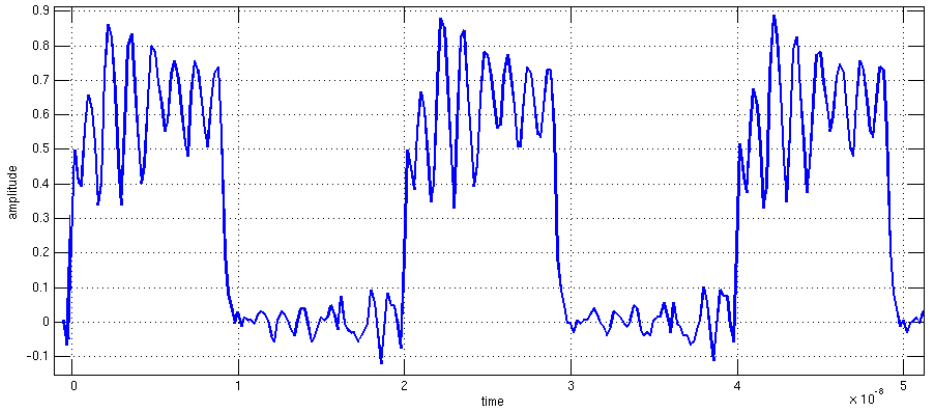

Figure 5.30. Self correlation demodulation result at 100 Mbps.

5.2.7.3. High frequency sampler. In this method, an external high frequency clock is used. However, the clock is not synchronized to data. Instead, baseband OOK IR-UWB pulses are recreated by the high frequency sampler. Therefore, the jitter and synchronization problem between the data and clock is resolved. In order to demodulate data, the clock frequency must be the same as the modulation clock. The data is sampled and demodulated by the circuit given in Figure 5.31. Post layout simulation results for 500 Mbps data and 2 GHz clock are given in Figure 5.32. 500 MHz UWB pulses are sampled with 2 GHz clock using 3 DFFs. The 2 GHz clock

is concurrently divided by 4 to obtain a 500 MHz clock. Then, clock and data are correlated through another DFF to demodulate the UWB pulses to obtain data. This circuit is operational at a fixed data rate for a given clock signal. 500 Mbps is achieved at the post-layout simulations with 2 GHz clock.

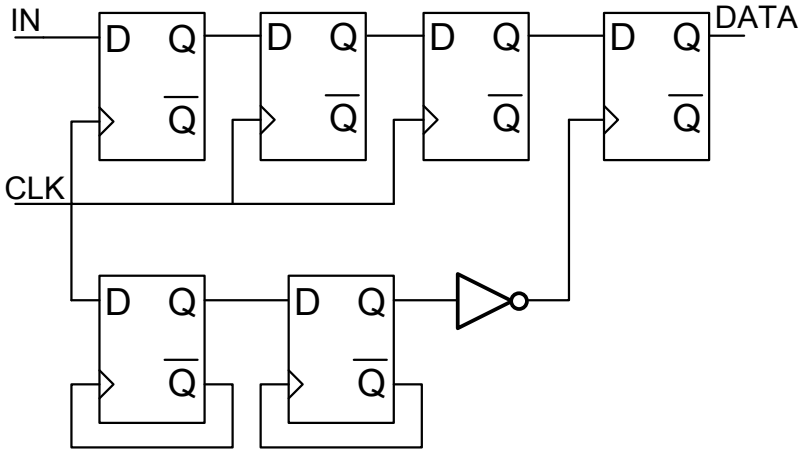

Figure 5.31. High frequency sampler and demodulator.

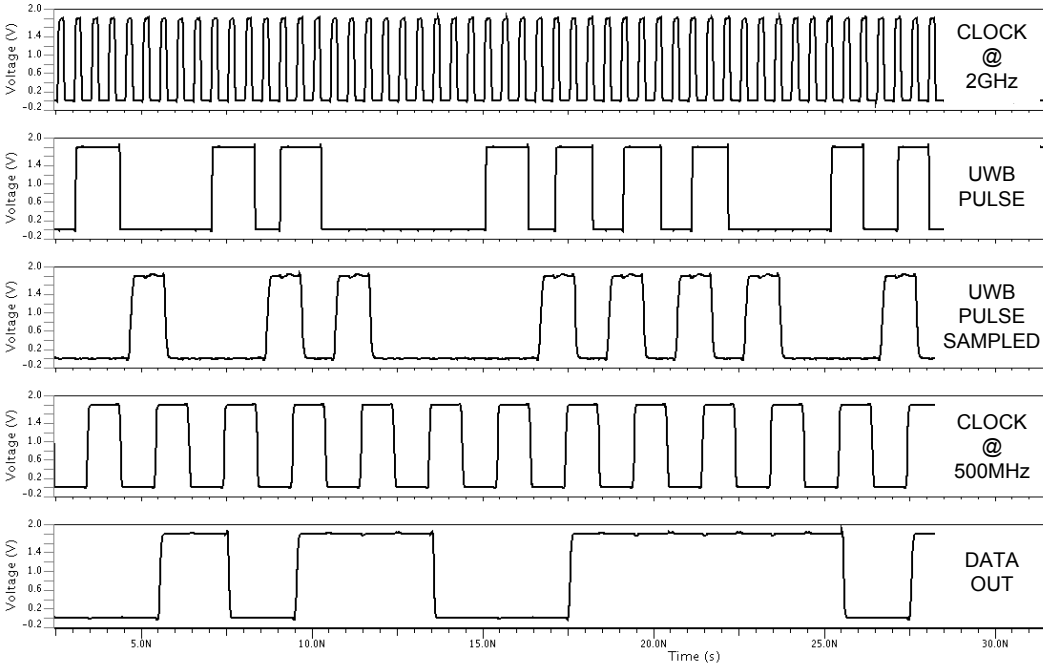

Figure 5.32. High frequency sampling simulations.

5.2.7.4. Discussion. The demodulation circuits are manufactured using UMC MMRF 130-nm CMOS process. The micrograph of the fabricated IC is given in Figure 5.33.

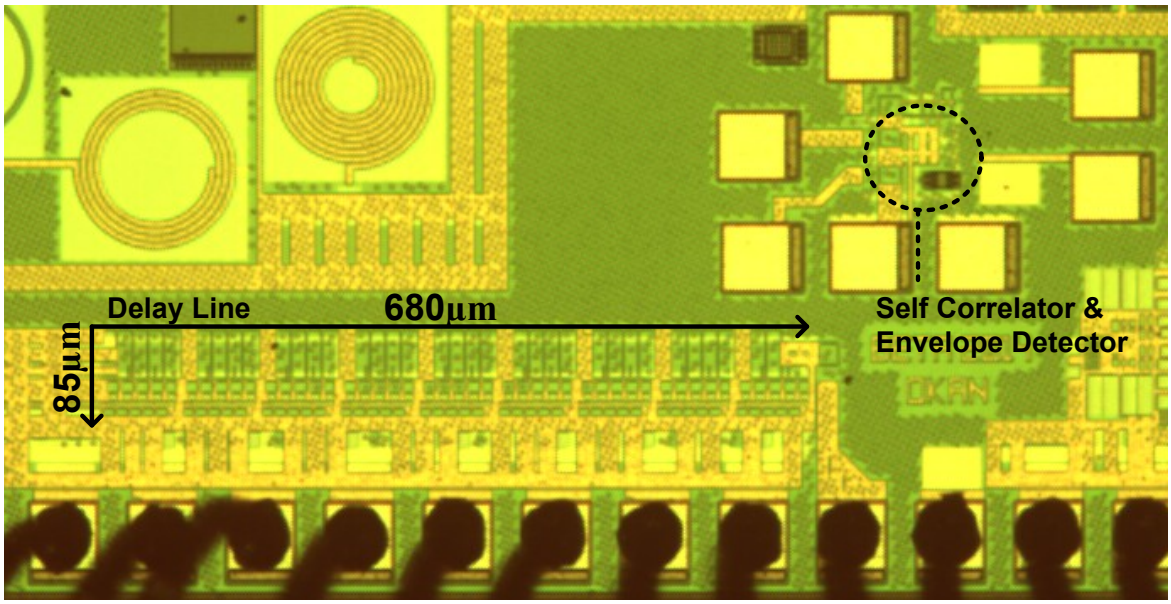

Figure 5.33. Micrograph of the implemented designs.

The measurements are taken from the packaged chip on a designed coplanar-waveguide RF PCB on an FR-4 substrate using SMA connectors.

The performance comparison with the state-of-art is given in Table 5.2. S-OOK is presented in [109] and achieves synchronization at the baseband stage with a low number of circuit elements with maximum 2 Mbps data rate. FSK-OOK architecture is utilized in [108] with 150 kbps bit-rate performance. In [107], the baseband demodulation architecture is synthesized on chip with large area cost. As can be observed from the table, the area and power consumption of the proposed architectures are extremely low. The achieved data rates are much higher then the previous non-coherent architectures in the literature. The self-correlator design utilizes a low jitter configurable delay line. Therefore, it has higher power consumption compared to the other proposed methods.

These designs eliminate the requirement of complex synchronization blocks and algorithms. The digital envelope detection and self correlation methods are implemented in 130 nm CMOS. Post-layout simulation results are presented for the high frequency sampling technique. The digital envelope detector works up to 600 Mbps data rate in the measurements, whereas 100 Mbps is achieved in the self-correlation

Table 5.2. Performance Comparison with the Previous Work.

Ref	**Tech. (nm)**	**Supply (Volts)**	**Area (mm^2)**	**Data (Mbps)**	**Power (mW)**	**EPB (pJ)**	**Mod.**
Envelope Detector	130	0.9	0.003	0-600	2-2.1	3.5	OOK
Self Correlator	130	1.22	0.58	0-100	10	100	OOK
Frequency Sampler	130 Layout	1.2	0.005	500	2	4	OOK
[**107**]	90	0.55	2.55	16	1.6	100	-
[**108**]	250	2.5	-	0-30	-	-	FSK-OOK
[**109**]	130	1.2	-	2	-	-	S-OOK
[**82**]	180	1.8	-	0.15	25	166000	OOK

technique. 500 Mbps data rate is observed in the post-layout simulations of the high frequency sampling technique. Although baseband digital demodulation architectures are present in the literature, such methods with high throughput have not been presented before to the best of our knowledge.

5.3. Coherent IR-UWB Receiver Design

Template based receiver architecture is designed for coherent detection of IR-UWB pulses. The system block diagram can be seen in Figure 5.34. The manufactured IC layout can be seen in Figure 5.35. The receiver has a modular design, where the transmitter circuit itself is also used as a template pulse generator at the receiver. This modular design allows coherent clock synchronization method to be used at the baseband conversion stage. A very fine Vernier delay line block is designed for template synchronization, which can be placed on a separate board to reduce the digital noise on the chip. There is also an active balun design for off-chip template signal input. The receiver has a 12 level flash ADC to differentiate signal from noise for robust detection. These ADC outputs are given to the FPGA board using VHDCI interface for synchronization and demodulation. A digital synchronization algorithm is developed on the Spartan 6 FPGA to control the receiver IC.

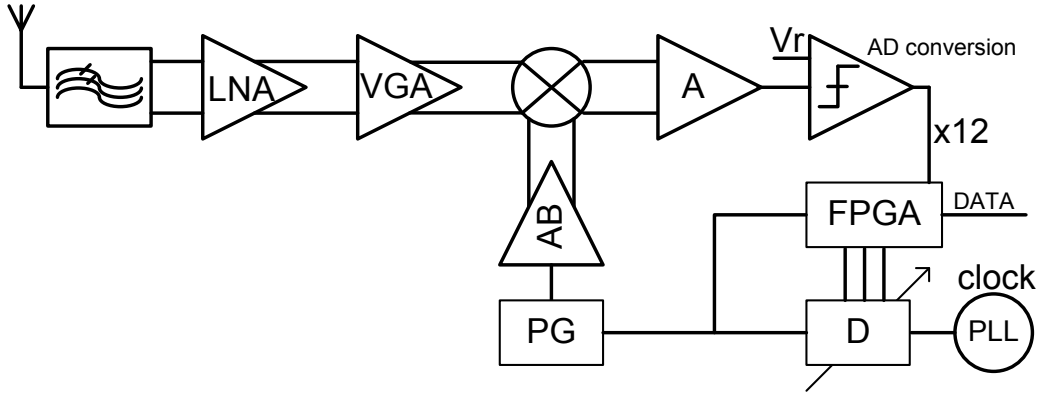

Figure 5.34. Template based coherent receiver.

From the previous two chip designs, it has been observed that the chips are produced at SS corner case, which affects the performance significantly. Therefore, the new chip which includes coherent receiver is designed to work best at SS corner and perform well at TT corner case.

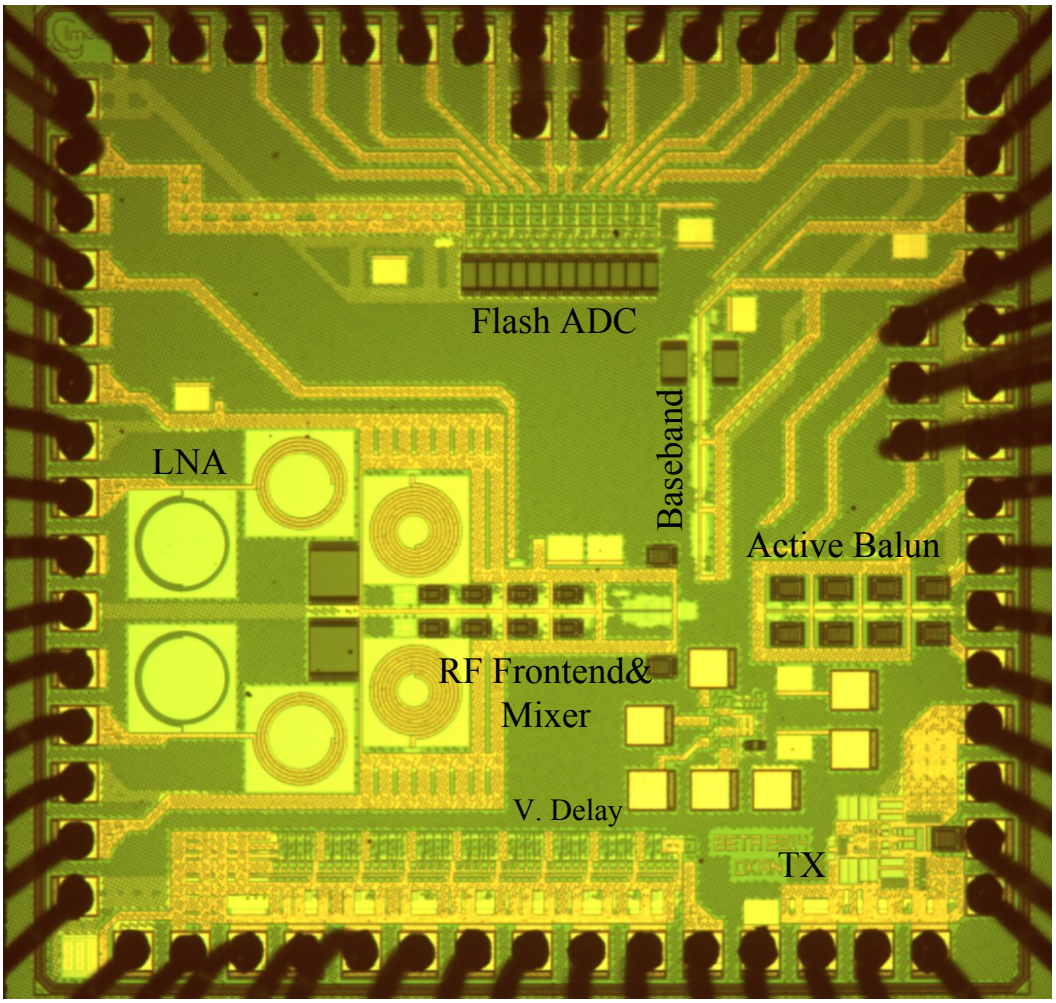

Figure 5.35. Coherent receiver micrograph.

5.3.1. RF Frontend

RF front-end is very similar to the RF blocks in non-coherent design. LNA and VGA performances have been improved. The ESD protection diodes in the BPF matching network are removed, because the shunt inductor of the BPF network also provides ESD protection. The noise figure is improved significantly from 4.5 dB to around 2.5 dB with better matching. LNA simulation results are given in Figure 5.36 and Figure 5.37.

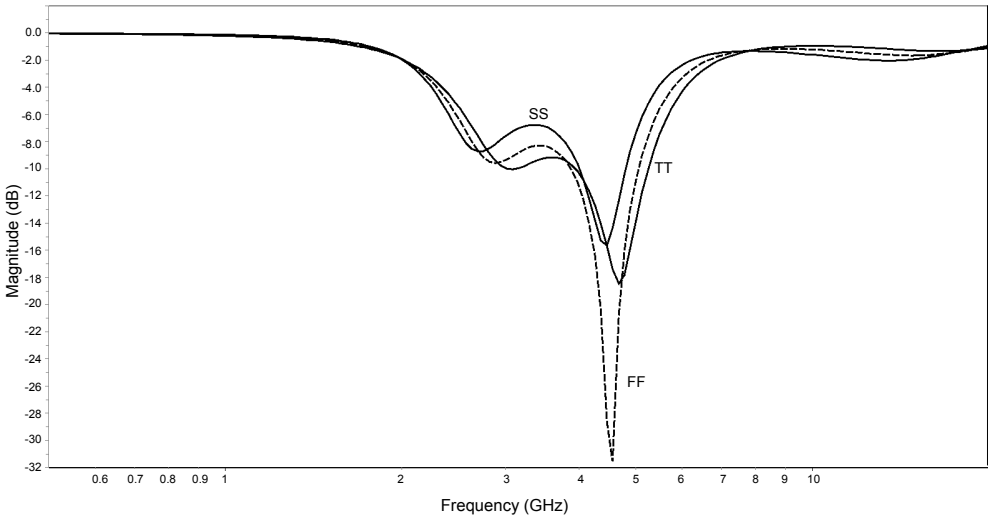

Figure 5.36. Noise Figure of the improved LNA design.

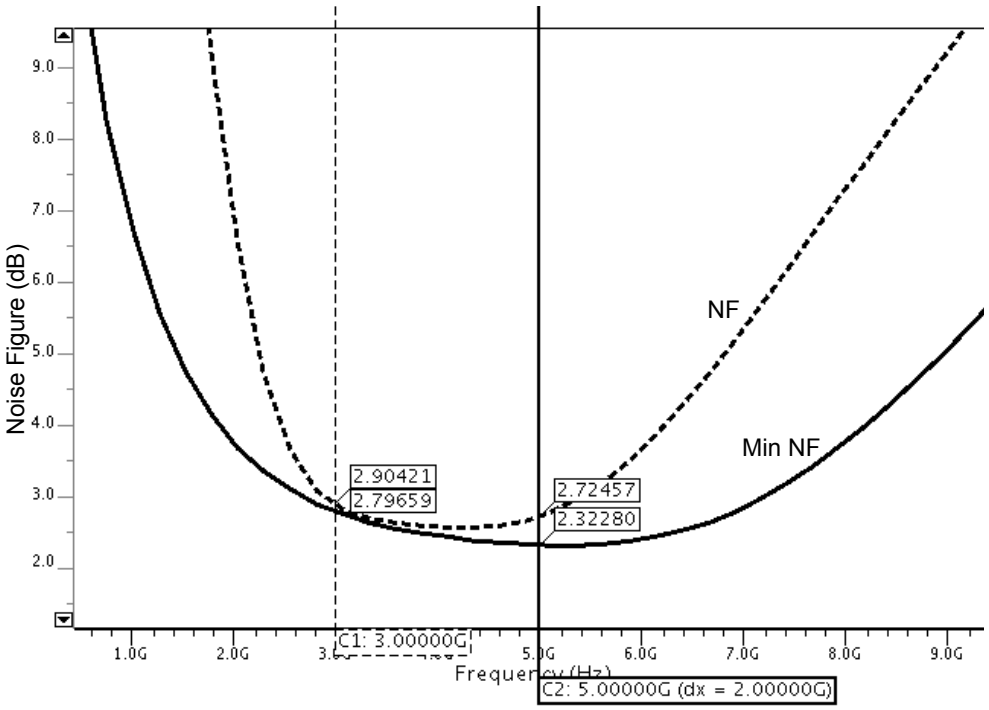

Figure 5.37. Corner simulation of the LNA input reflection.

5.3.2. Flash ADC design

12 levels of thermometer code output flash ADC is designed Figure 5.38. Large capacitors are placed on reference nodes to lower the kick-back noise on the reference

nodes. The flash ADC does not include clock for conversion, since the receiver deals with sub-nanosecond pulse detection. The same hysteresis comparator architecture as the non-coherent receiver is used. The reader is referred to Figure 5.13 for details. The outputs of the ADC connected to FPGA board with buffers.

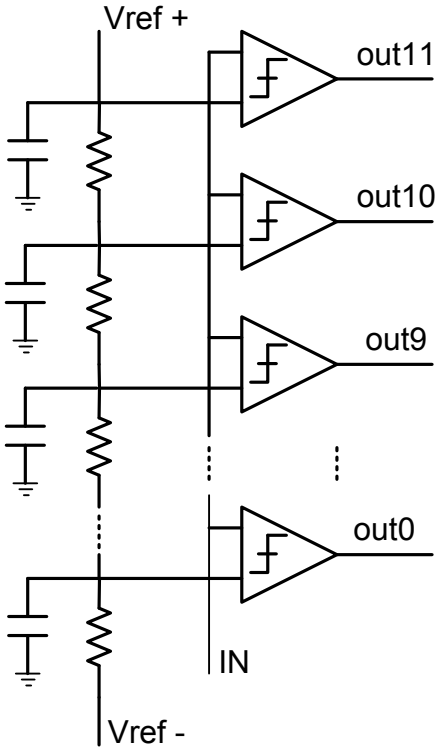

Figure 5.38. Flash ADC.

5.3.3. Active Balun Design

An active balun for template LO input is necessary to minimize the LO-IF leakage in the mixer. The differential LO signal's phase and amplitude must match according to study in [1] in frame 5.39. If an off-chip balun was used, there would be additional mismatch due to PCB, packaging, and wire-bonds apart from the passive balun's own mismatch. Therefore, three stage on-chip active balun is designed for better matching LO differential signals. The active balun design is flexible so that it is also possible to give an already differential signal to the active balun as in Figure 5.40, and Figure 5.41.

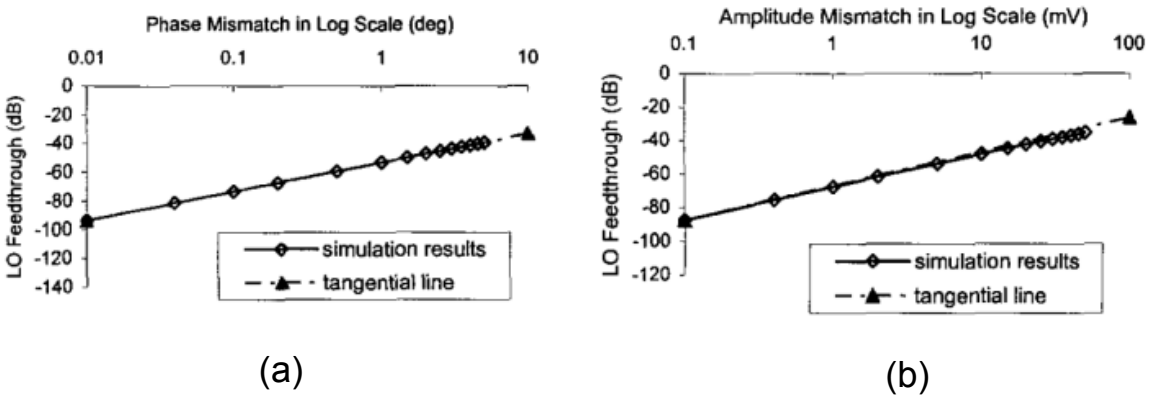

Figure 5.39. (a) Phase mismatch, (b) Amplitude mismatch in a mixer [1].

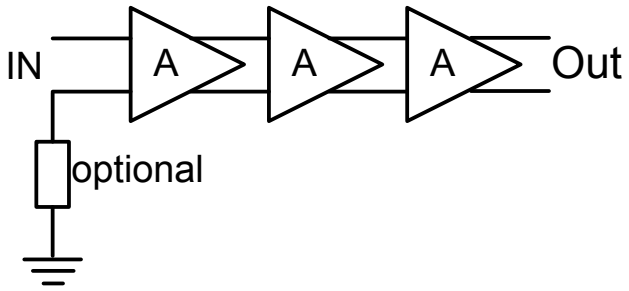

Figure 5.40. Active balun block diagram.

In Figure 5.42, active balun simulations are provided. After two stages, a differential signal is obtained. The active balun is composed of three stages to ensure differential input to mixer to reduce LO-IF leakage.

5.3.4. Configurable Vernier Delay Line

The variable delay line (VDL) has a wide range of applications and is used in many designs. It is mostly employed in phase locked loop (PLL) [110] and delay locked loop (DLL) [111] circuits for synchronization. Digitally controlled delay elements (DCDE) are the basic block of the VDL and they are also utilized in digitally controlled oscillators (DCO) [112], and frequency synthesizers [113]. Another application of the delay cells are time to digital conversion (TDC) circuits [114].

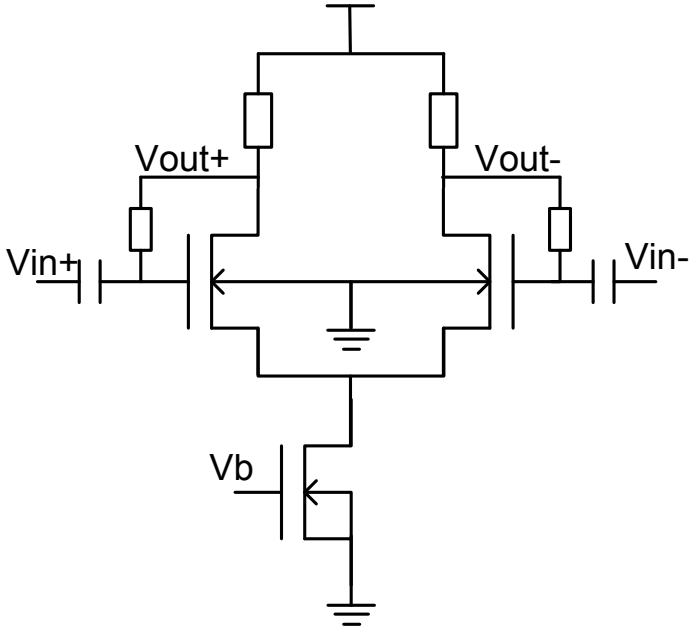

Figure 5.41. Schematic of single active balun stage.

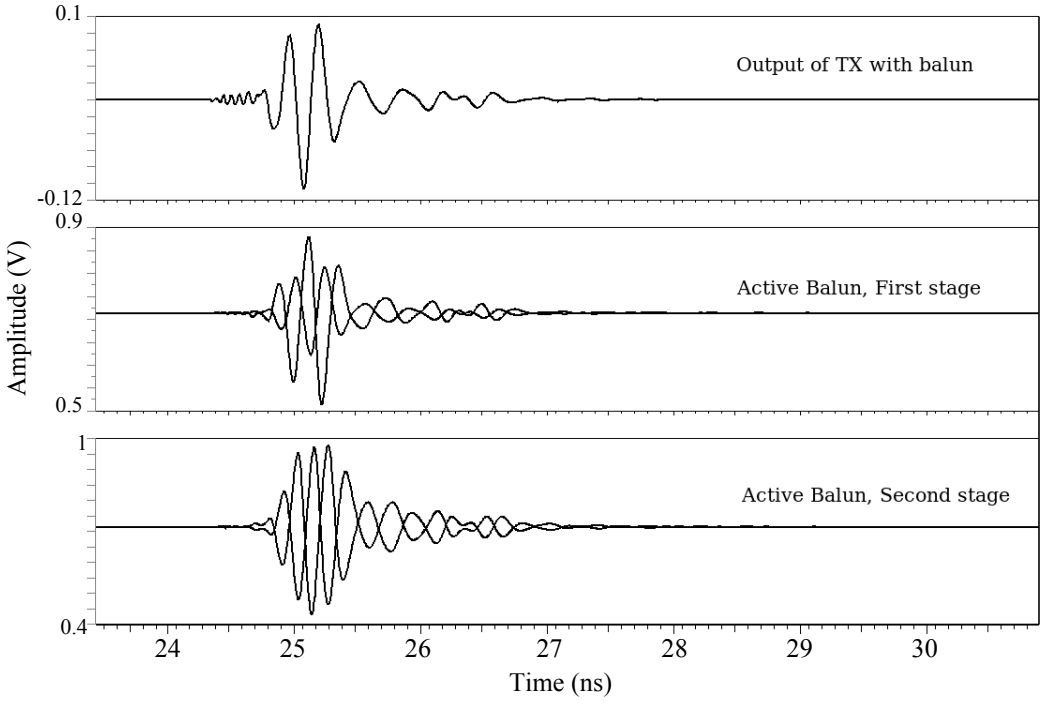

Figure 5.42. Active balun simulation.

Current starving inverter (CSI) [115], [116] and capacitor shunt capacitor approaches [117] are commonly used to construct a delay line. The multiplexer approach is also employed in the literature [118]. In the current steering approach, current is limited through NMOS and PMOS networks of the CMOS inverter as shown at Figure 5.43 a. In the CSI method, differently sized transistors are utilized in the PMOS and NMOS networks to limit the current passing through the inverter and to change the rise/fall times of the inverter. On the other hand, the current is not limited in the shunt capacitor method in Figure 5.43b. Instead, the capacitor load is changed. The fall and rise times are altered by the additional RC delay.

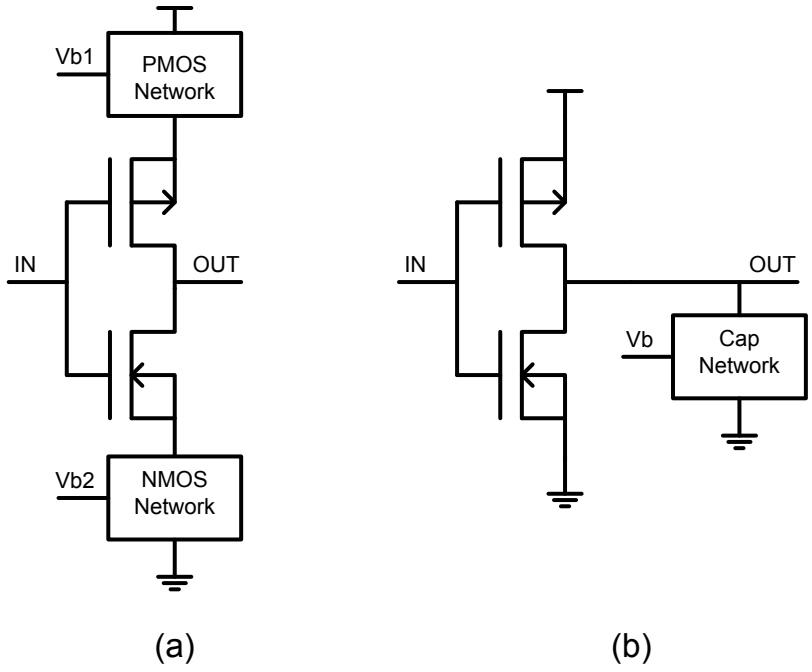

Figure 5.43. Delay cells (a) Current steering, and (b) Shunt capacitor methods.

The shunt capacitor method which has a linear response and lower jitter compared to CSI is preferred in this work [119]. A highly linear and very low jitter delay line with pico-second time steps is required for this specific application. The previous work in the literature mostly focuses on the power consumption. The linearity and jitter is the main objective of this design. To increase linearity, multiples of a unit capacitor are used. A small unit capacitor value is selected and the inverter transistor sizes are kept relatively large to increase the slew rate which also lowers the jitter [120].

5.3.4.1. Delay Cell Architecture. The Vernier delay line is composed of capacitive loaded buffer stages. In a high speed IR-UWB receiver, synchronization must be completed in very short and precise time steps. Therefore, the delay cell must have fast and linear response. The delay of an inverter could be adjusted using the parameters from

$$T_d = \frac{C_{Load} * V_{in}}{I}. \tag{5.1}$$

The configurable load capacitor is the easiest and most effective way to control the propagation delay in constant and linear delay increments. The delay configuration and respective output is expected to be linear as in the Figure 5.44.

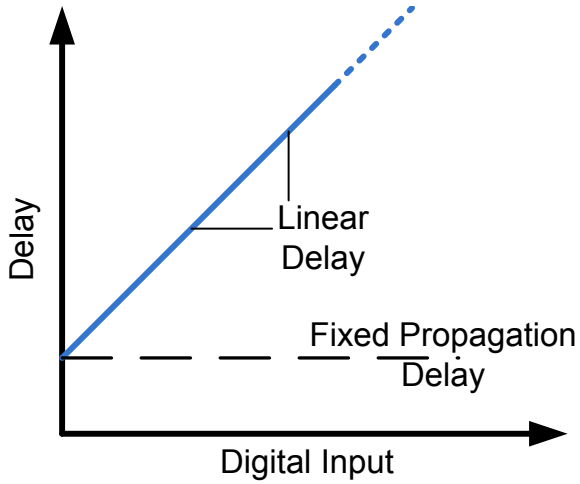

Figure 5.44. Propagation delay vs digital input.

MOS capacitors are used at the output of the inverter stages as shown in Figure 5.45. Triple well floating NMOS devices are exploited to reduce the effect of substrate noise on the jitter. The WL product of the MOS devices determines the value of the capacitor. However, the delay is not increased linearly with the WL product because of the parasitic effects at the drain and source regions. In order to achieve linear delay, a unit size MOS capacitor is selected. Then, instead of increasing the WL product of the MOS capacitor, the number of unit size MOS capacitors is increased in binary

values as shown in Figure 5.45.

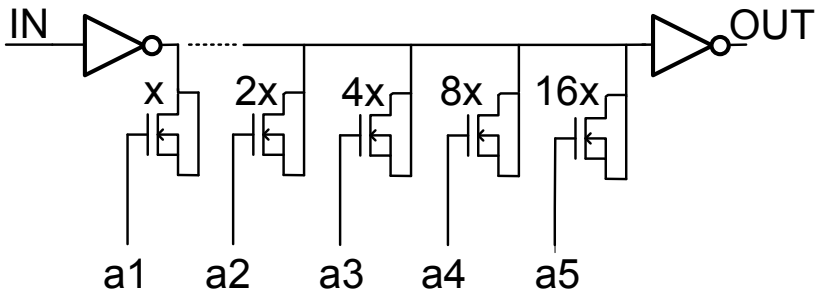

Figure 5.45. Single delay cell.

$$T_d = R \cdot [C_p + C \cdot (a_1 + 2 \cdot a_2 + 4 \cdot a_3 + 8 \cdot a_4 + 16 \cdot a_5] \tag{5.2}$$

represents the total delay, where C_p is the parasitic capacitor of the inverter. The capacitor values are increased in binary increments. Since the output of the counter is also binary, the resulting delay differences between the delay steps becomes a constant value.

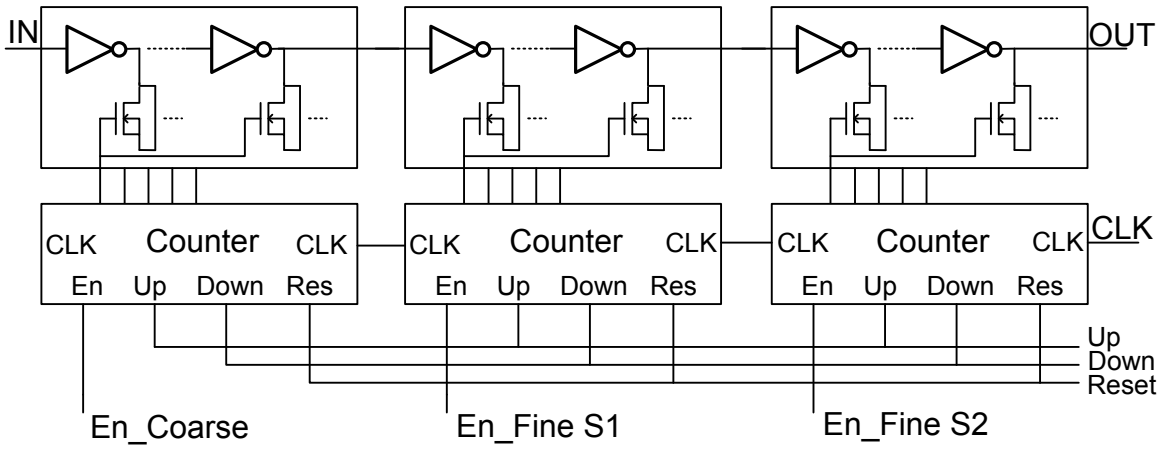

Figure 5.46. Configurable delay line architecture.

The configurable Vernier delay line is given in Figure 5.46. It is composed of 34 cascaded delay cells. The design also includes configuration circuitry. To increase the configuration speed and to reduce the number of pins, 5 bit up-down counter with

asynchronous reset having 1 GHz response time is designed. The delay line is designed to be used in a synchronization search algorithm. The incremental configuration was also desired for synchronization. The fine delay stages are placed towards the output.

5.3.4.2. Measurement Results and Discussion. The variable delay line is manufactured using UMC MMRF 130-nm CMOS process. The designed layout and respective micrograph are given in Figure 5.47a and Figure 5.47b respectively. The core area of the manufactured circuit is 0.58 mm^2.

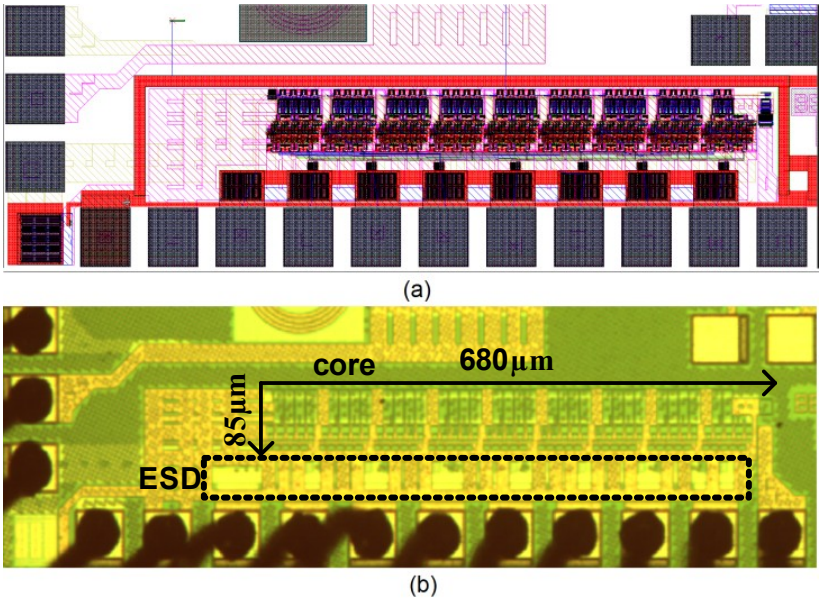

Figure 5.47. Delay line (a) layout design, and (b) micrograph.

The UP/DOWN, ENABLE and asynchronous RESET inputs are present for the configuration of the delay line with clock signal. These configuration signals are created using a Spartan 6 FPGA board with VHDCI interface was depicted in Figure 5.48. ADF 4351 PLL evaluation board is utilized to create the clock signal. The second output of the PLL is used as reference clock to observe the change in delay. Lecroy Waverunner 6100A 1 GHz real time oscilloscope is used in the measurements.

The value of the MOS capacitor and the size of the inverters are carefully selected to improve the jitter performance of the delay line. Larger transistors lead to higher power consumption and hence lower jitter. Capacitors cannot be selected lower than

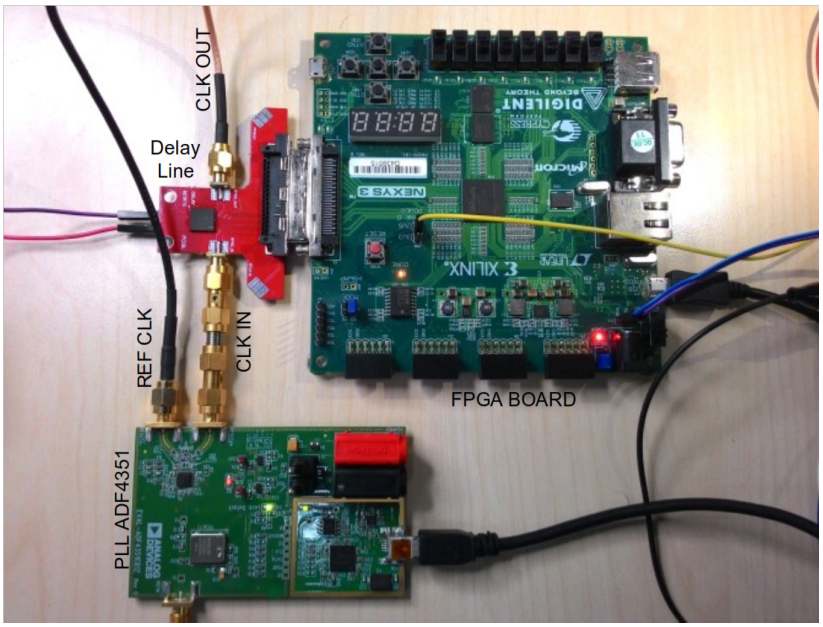

Figure 5.48. Measurement setup.

a certain value, because the parasitic effects start to dominate. Therefore, in order to achieve a linear delay line with low jitter performance, it is necessary to increase the power consumption. The long time total jitter including the PLL is measured as 3.6 ps as depicted in Figure 5.49. The long time jitter of the PLL is 2.8 ps. Therefore, the additive jitter of the delay line is 2.3 ps.

Table 5.3. Impact of Process Variations.

Cases	**Coarse (ps)**	**Fine 1 (ps)**	**Fine 2 (ps)**
TT	61.67	20.55	4.93
SS	75.5	25.28	6.18
FF	53.94	17.91	4.25
SF	58.1	19.36	4.64
FS	66.49	22.16	5.31
Meas.	52	17.5	4.5l

The static power consumption is negligible. The extremely low jitter value is achieved at the expense of dynamic power consumption. The circuit was powered at 1.22 V with the LT1763 low noise voltage regulator. The dynamic current drawn from

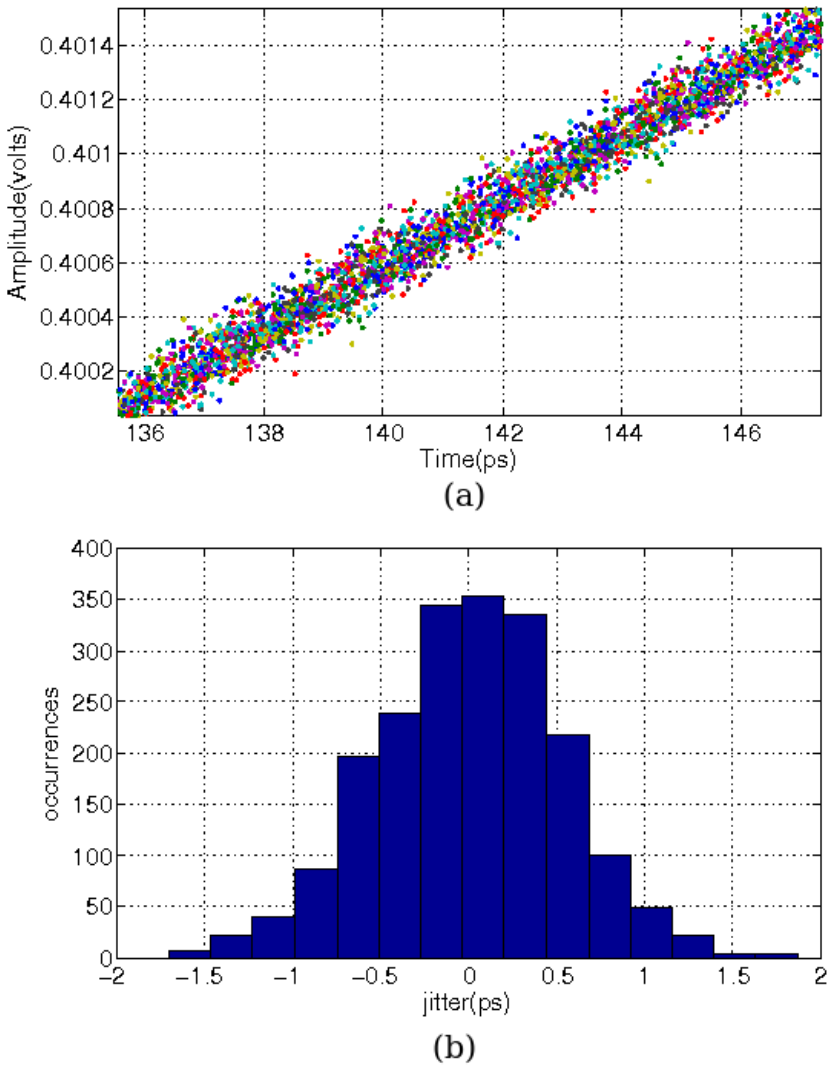

Figure 5.49. Jitter measurements (a) jitter plot, (b) jitter histogram.

the circuit including the output pad driver at 500 MHz input changes from 8.2 mA to 17.8 mA depending on the capacitive loading. The corner case post layout simulations of the delay line are given in Table 5.3. The results in the Table I clearly shows that the manufactured IC is at FF corner case.

Delay measurements are given in Figures 5.49- 5.53. The measured delay increments are highly linear. There is a delay decrease in counting from 15-16. The wiring of 15 individual capacitor blocks (1X, 2X, 4X and 8X) brings additional wiring parasitic compared to the easier combination of a single block of 16 capacitors.

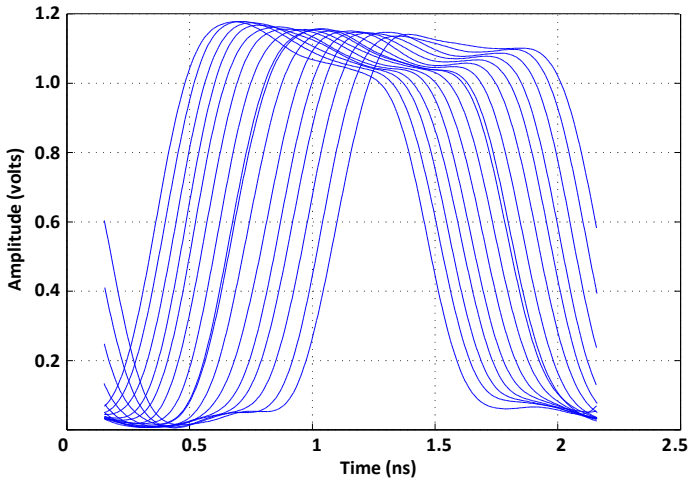

Figure 5.50. 52 ps/step measurement.

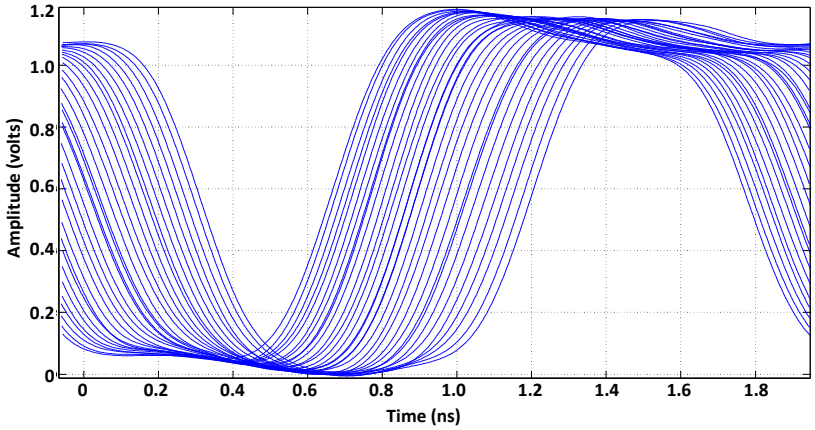

Figure 5.51. 17.5 ps/step measurement.

Table 5.4. Performance Comparison.

Ref.	**Jitter (ps)**	**Precision (ps)**	**Power (mW)**	**Max. Freq. (MHz)**	**Tech (nm)**
Our work	2.3	4.5	10-21.7	0-600	130
[110]	70	5	100	45-510	350
[121]	%3	80	1	170	130
[112]	31	0.53	0.57	550-830	32

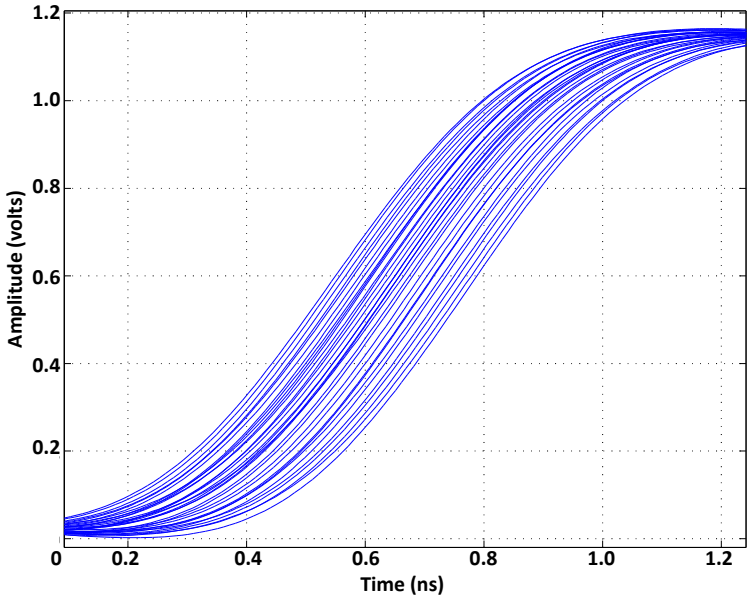

Figure 5.52. 4.5 ps/step measurement.

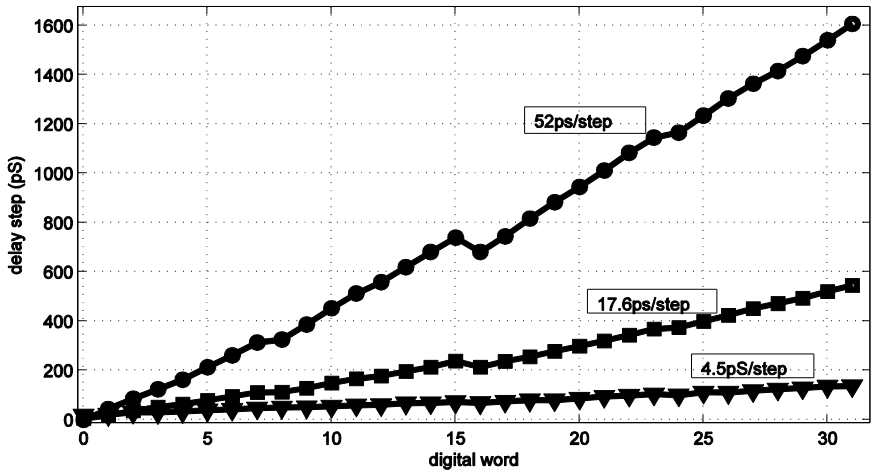

Figure 5.53. Delay vs digital word measurements.

A comparison with the literature is given in Table 5.4. As can be seen from the table, the proposed architecture has a superior jitter performance compared to previous work. The low jitter, high precision and linearity are the important parameters for IR-UWB receiver systems. In our work these objectives are accomplished and demonstrated through the measurement results [119].

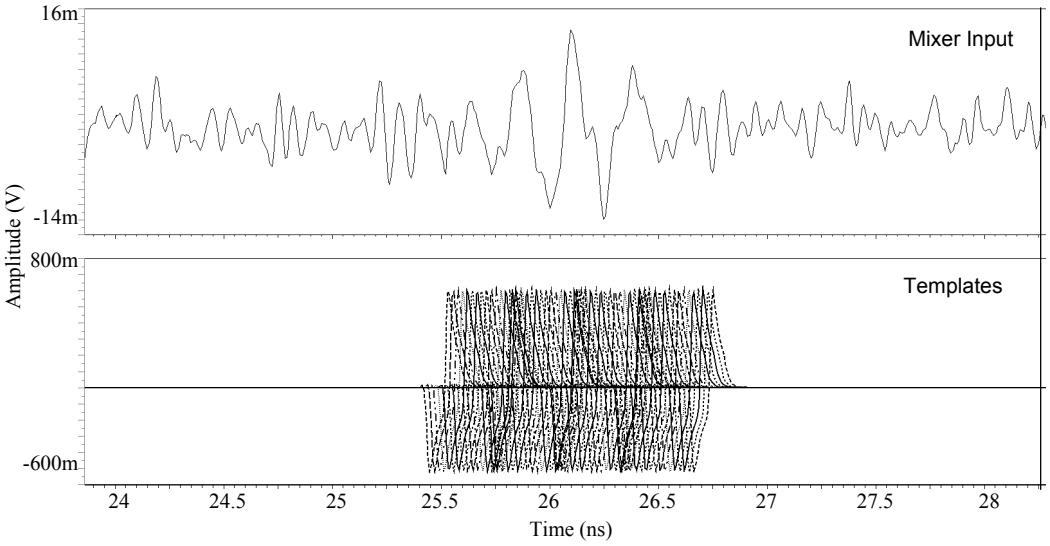

Figure 5.54. Shifted templates with delay line.

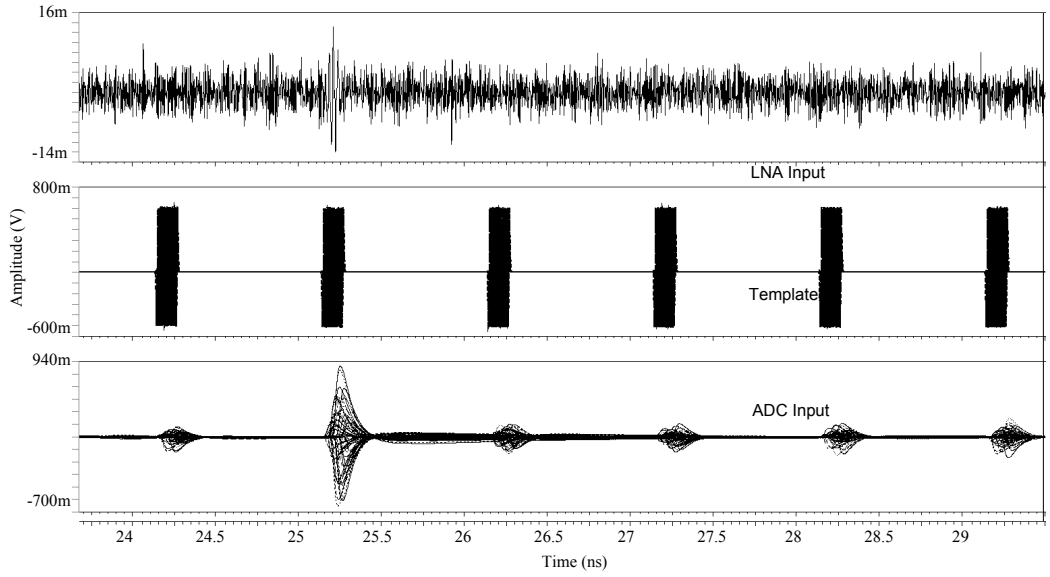

Figure 5.55. Template correlation simulations under noisy channel.

5.3.5. Coherent Receiver Simulations

The receiver simulations are mostly based on template synchronization results. The template is shifted in time with the digital configuration of the delay blocks. Therefore, the template signal shifts in time. Figure 5.54 shows these shifted Gaussian

mono-cycle templates. It was not necessary to use Gaussian mono-cyle, higher order pulses could also be used on the template input of the receiver. The simulations of the coherent receiver are given in Figures 5.55- 5.57.

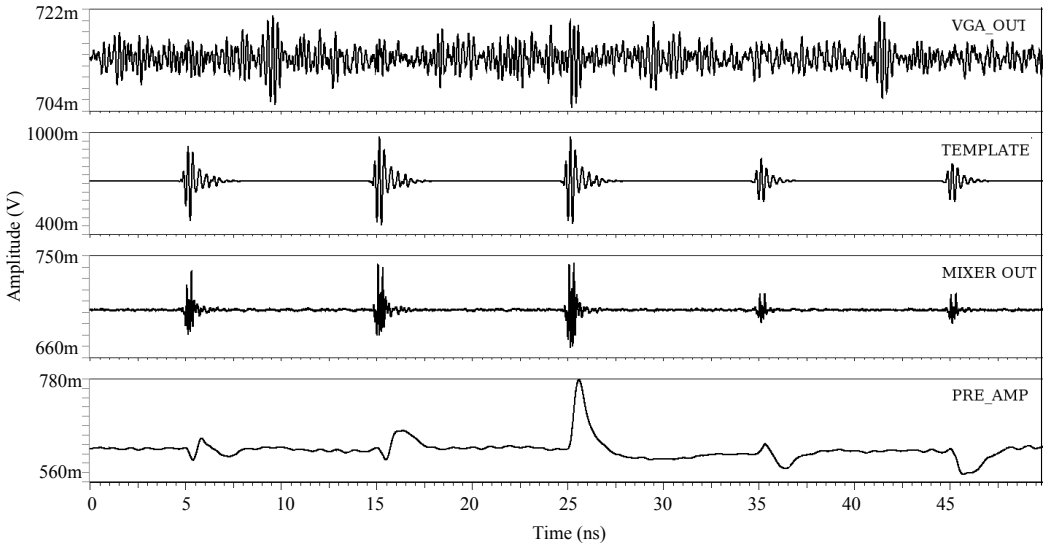

Figure 5.56. Template receiver simulation.

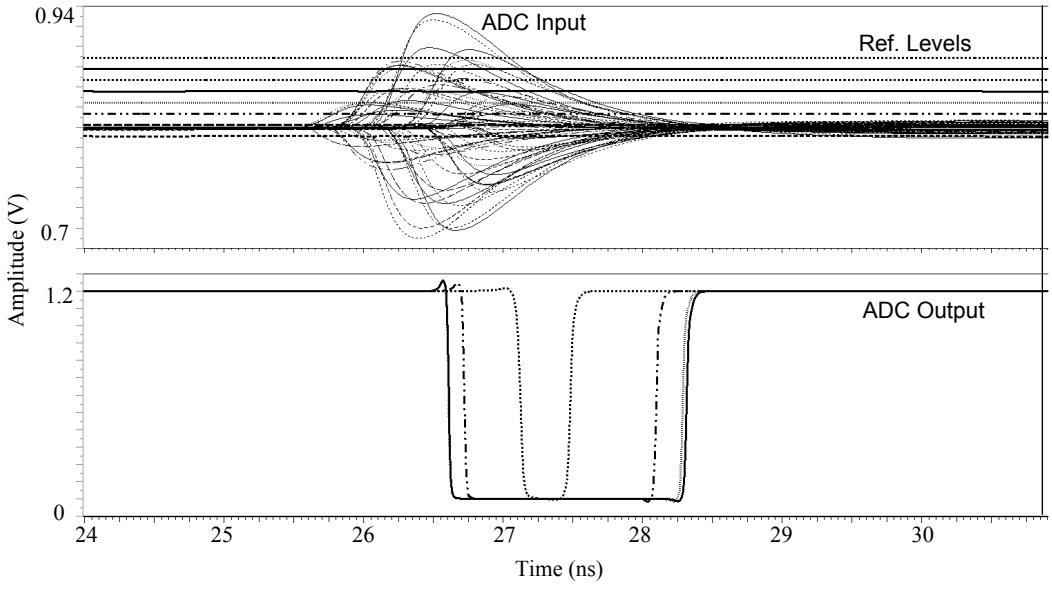

Figure 5.57. ADC inputs and outputs of the coherent receiver.

5.4. ESD Designs

ESD is neccessary in ICs to protect them from static electricity both from mechanical and human static discharge. ESD protection circuitry is placed in the gate inputs of the chip as well as between the VDD-GND line which is also called clamping ESD as shown in Figure 5.58.

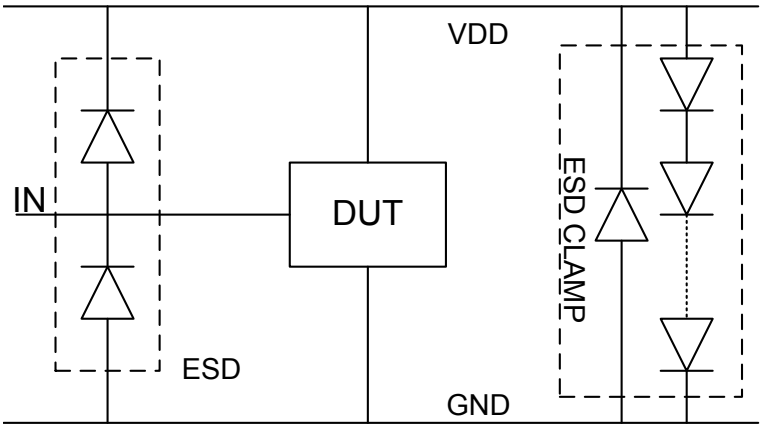

Figure 5.58. ESD placement.

According to [93], there is a simple approximation to find the maximum voltage that the MOS gate can take before the gate oxide breaks down. The breakdown voltage is dependent on technology node as expressed in

$$V_{\text{BREAKDOWN}} = 20\frac{V}{nm} * \text{Technology (nm)}. \tag{5.3}$$

The minimum gate length is 120 nm in UMC 130 MMRF technology. Therefore, the maximum gate voltage is 2.4 V, which is also confirmed by measurements performed in our laboratory. The gate oxide in UMC 130 MMRF brakes down at around 2.35-2.4 V in our experiments.

The ESD designs and simulations are based on Class II human body model(HBM) as described in [93]. In Class II HBM, the ESD diodes are required to absorb the 1.33 A current, while 2000 V static voltage discharges with rise time is 2 ns and fall time

is 170 ns. Under the electrical stress pulse, the internal voltages must be maintained at a safe level. The ESD design is done using circuit in Figure 5.59.

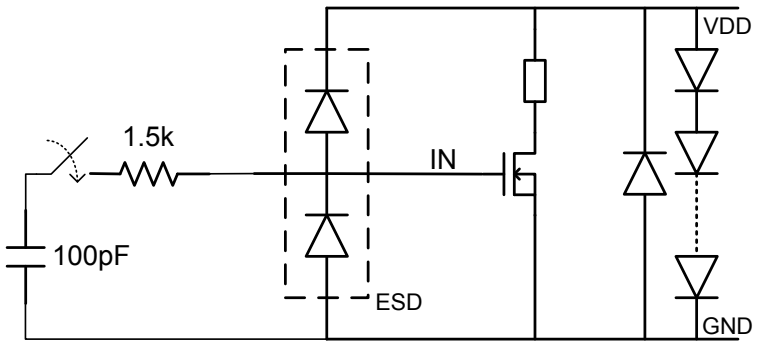

Figure 5.59. ESD test circuit.

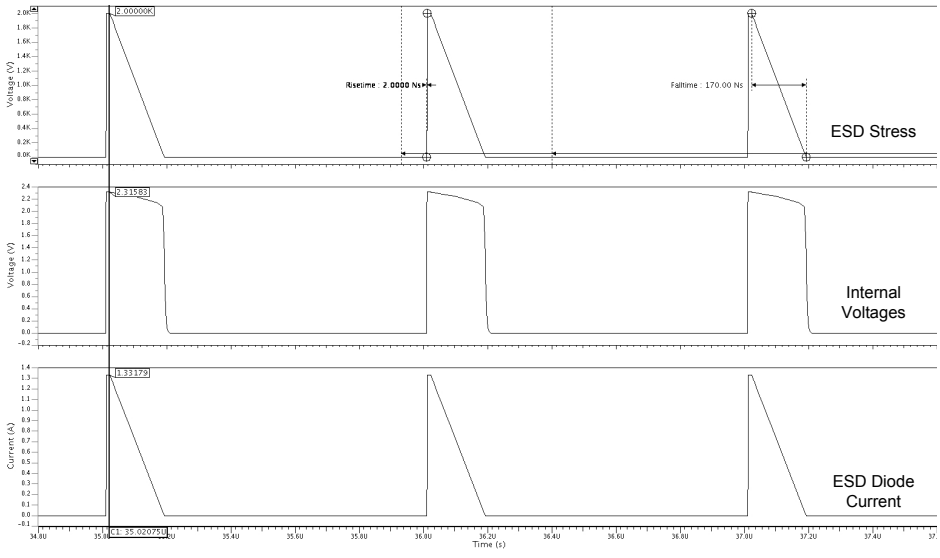

Figure 5.60. ESD simulations.

The simulations in Figure 5.60 show that the designed ESD can withstand 2 kV of static electricity while maintaining internal voltages below 2.4 V of breakdown voltage. However, it has been seen that the a single 2 kV ESD protection circuit occupies 120μm $\times$120μm of die area which is very large area compared to total die size of 1525μm $\times$1525μm. Therefore, the ESD protection is reduced to 800 V to have a reasonable ESD layout. Smaller ESD size also reduces the noise on LNA input caused by the junction capacitances of the diodes.

5.5. Conclusion

In this section, both coherent and non-coherent IR-UWB transceiver architectures are realized at UMC 130 MMRF technology.

Most non-coherent architectures in the literature are designed for low data-rate applications below 20 Mbps. The method of using envelope detector together with the energy detector is introduced and the clocking circuitry is avoided which makes it possible to achieve high data rate circuitry with a non-coherent architecture in short range applications. In our work, 240 Mbps data rate is achieved with 0.2 nJ/bit power consumption over 1 meter range. To the best of our knowledge, this makes the receiver unique in the literature. Three baseband demodulation architectures are proposed for non-coherent receivers. Although baseband digital demodulation architectures are present in the literature, such methods with high throughput have not been presented before.

On the other hand an ultra low power template based coherent receiver is designed and implemented. At the time of writing, the measurements of the transceiver are underway. The template based receiver has additional blocks such as template pulse generator, configurable delay line, FPGA for synchronization control. The template based IR-UWB transceivers require precise delay architectures with low jitter response. A 600 MHz linear Vernier delay line with pico-second jitter response that can be used in synchronization of IR-UWB is designed and measured. Although configurable delay lines are present in the literature, such low jitter delay lines have not been presented before to the best of our knowledge.

6. ANTENNA AND PCB DESIGNS

6.1. Introduction

The choice of external components and materials is a challenging task for high frequency UWB systems. There are commercially available materials that are designed to have better performance in high frequency applications compared to the commonly employed FR4 material. However, the simple FR4 material is selected for this project, since the material selection does not have much of an effect on 3-5 GHz designs in a laboratory environment. Transmission line theory has to be used in the design of PCBs and antennas because of the wideband nature of the impulse radio transceiver system. This chapter gives details about designed antenna and PCB designs with measurement results. Antenna and some PCB designs are completed with collaboration of a graduate student [122].

6.2. Antenna Design

The first step in choosing an antenna is to determine the required communication distance and hence the gain. This requirement will determine the size of the antenna. The wavelength is in the order of a few centimetres in 3-5 GHz UWB systems. The most commonly type of a UWB antenna is the patch antenna patterned on PCB. The reason is that the wideband characteristic is more easily maintained with the patch antenna. In addition, they can be easily fabricated with relatively low cost. From this point of view, the design process of UWB antenna starts with a literature survey. An UWB antenna is selected from the literature [27] for comparison. It is fabricated and measured to observe the difference with the proposed antenna. This antenna in Figure 6.1 is referred as reference antenna for the rest of the thesis.

To achieve an UWB operation for this antenna, firstly a trapezoid shaped feed line is used in microstrip line form with ground plane on the back side for the purpose of having better impedance matching. Then, the feed line and the main patch is

Figure 6.1. The fabricated reference antenna.

put together with tapered intermediate connection which provides wider impedance bandwidth [27].

The second analysis is on a commercial antenna named In4Tel patented Wisair antenna as shown in Figure 6.2. This antenna has an additional property of including a microstrip bandpass filter different from the others as a solution for limiting the band [28]. This compact design combining the filter with the radiating patch, shows a considerable performance improvement in terms of band rejection. Furthermore, the substrate on which the the patch is patterned is a special material providing low loss and high efficiency.

Figure 6.2. The commercial antenna.

As a conclusion, the UWB antenna is designed (referred as 1st antenna) in the light of simulation results and the antenna proposed in [29]. The sections of both designed antennas is given in Figure 6.1. The feed line has a length of 4 cm which is the same as the wavelength of the received RF signal at 4 GHz. A longer feed line corresponds to a higher loss and more attenuation on the signal transmitted or received. In this context, the feed line may be kept as short to reduce the attenuation.

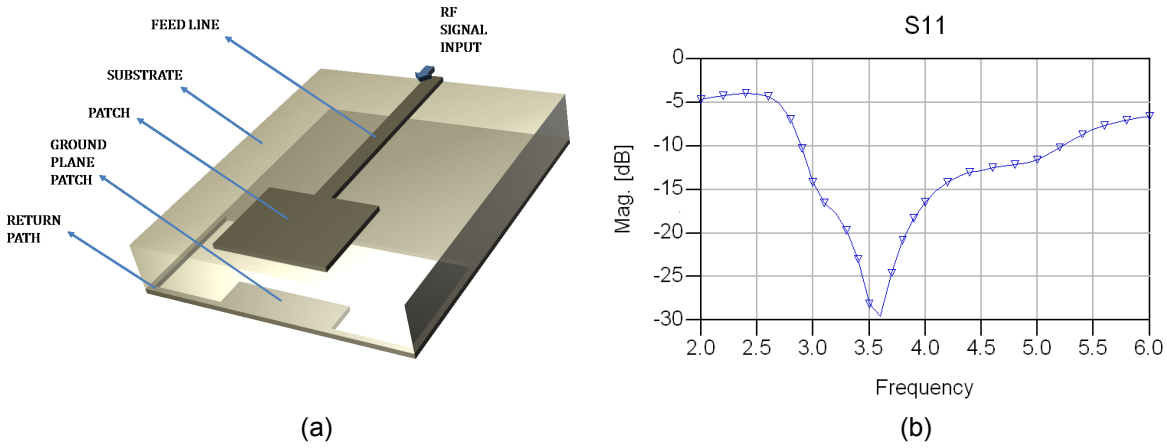

Figure 6.3. Proposed antenna; (a) Geometry (b) S11 simulation results.

The dimensions of the patch, and ground plane patch, the distance from the ground plane to the bottom edge of the radiating patch are initially taken from [29]. Then, the optimization process starts by adjusting the position of the feed line in the horizontal axis. The ground plane patch is relocated to have the desired response. The return path covering the patch from the back side, is connecting the ground plane patch to the ground. After some improvements, the S11 response turns out to be as shown in Figure 6.3b.

The manufactured antenna is given in Figure 6.4. The measurements are performed using a network analyzer with the established test setup which can be seen in Figure 6.5a. The simulation and the measurement results of the antenna are depicted in Figure 6.5b, which satisfies the -10 dB S11 reflection coefficient criterion in the band of interest.

Figure 6.4. Proposed antenna; (a) top view (b) bottom view.

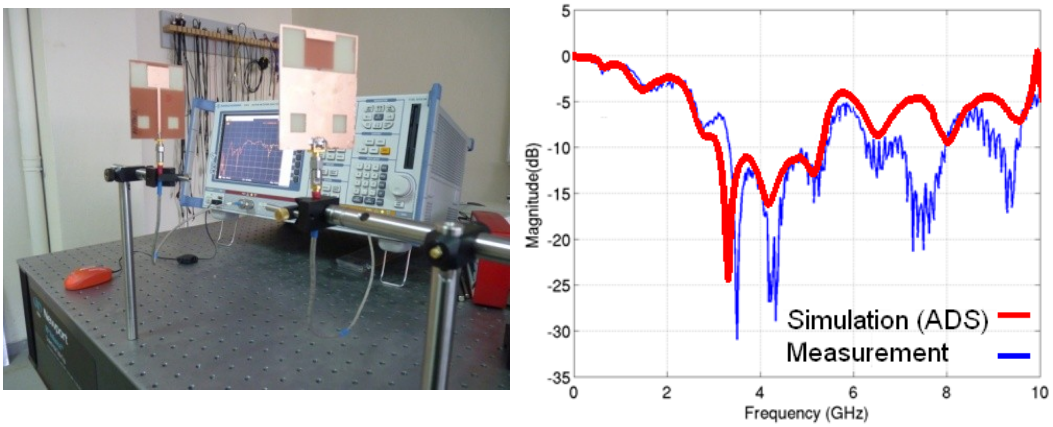

Figure 6.5. Proposed antenna; (a) Measurement setup (b) Simulation and measurement results.

It is also stated in the literature that the ground plane shape can effect the overall performance [30]. Hence, in order to observe the behaviour of the antenna when the ground plane is patterned, an additional antenna (referred as 2nd antenna in the plot) is designed. The substrate thickness is the half of the 1st antenna. The performance of these antennas are measured from various distances.

Following the characterization of the antennas, measurements are taken to find

a comparison between the designed antennas, reference antenna, and the commercial antenna (referred as Wisair antenna in the plots). The comparison between the designed antennas and the reference antenna is given in Figure 6.6a. Similarly designed antennas are compared with the commercial antenna in Figure 6.6b.

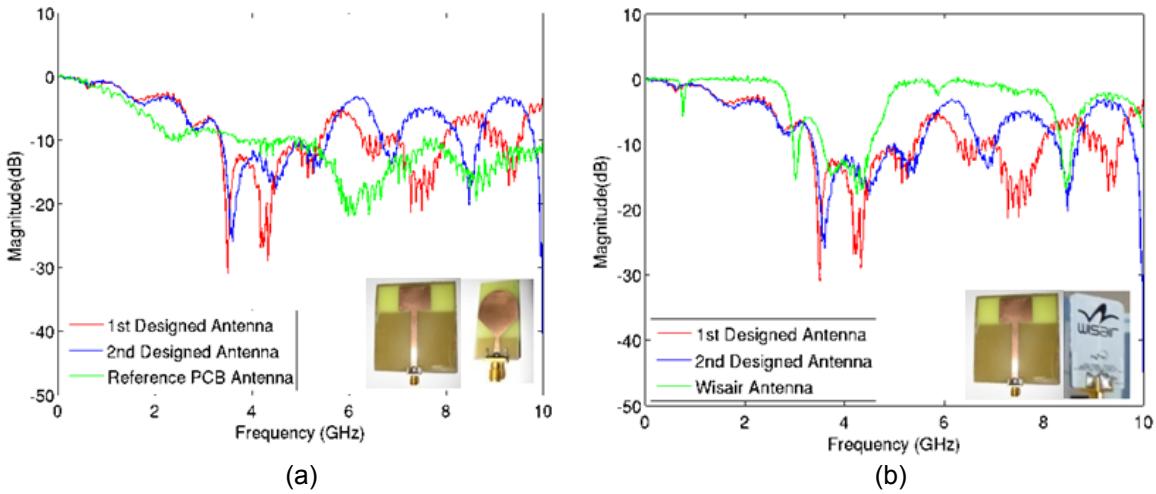

Figure 6.6. S11 comparisons (a) designed antenna vs. reference antenna (b) designed antenna vs. commercial antenna.

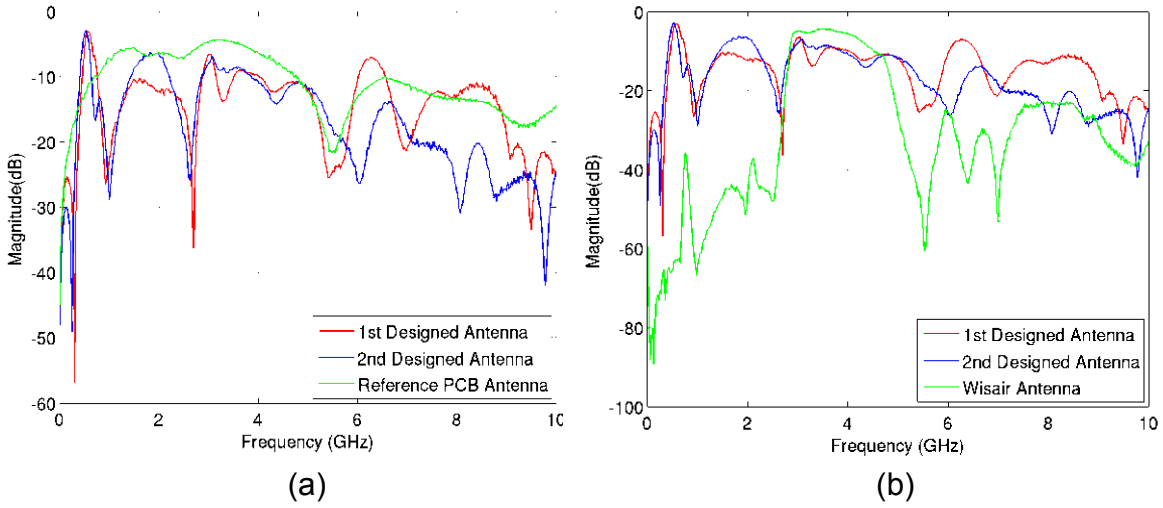

Figure 6.7. S21 comparisons for 1cm distance (a) designed antennas vs. reference antenna (b) designed antennas vs. commercial antenna.

As a conclusion, the performance of the antennas are measured from various distances. When antennas are close to each other by approximately 1 cm, from Fig-

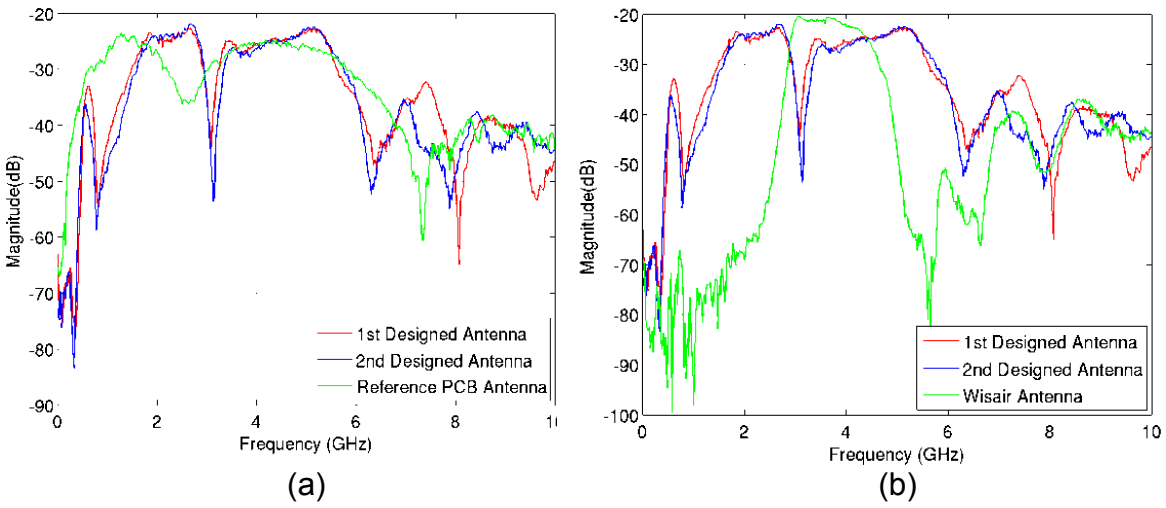

Figure 6.8. S21 comparisons for 10cm distance (a) designed antennas vs. reference antenna (b) designed antennas vs. commercial antenna.

ure 6.7a, the reference antenna seems to work with less loss but there is no bandpass response. Besides, the commercial antenna has a better performance in-band operation. However, the designed antennas have the intended bandpass characteristics as observed in Figure 6.7b.

From a longer distance, around 10 cm, the behaviours of all antennas are measured. In the light of the results presented in Figure 6.8, similar interpretations can be obtained. The loss of the designed antennas reduce to -25 dB roughly only 5 dB less than commercial antennas.

6.3. FR4 PCB Designs

Transmission line theory is used in the design of the PCBs in order to maintain matching, minimize the PCB loss, and prevent the coupling of the signals. Micro-strip lines are well known and easy to design for rapid prototyping, because they do not involve through-hole paling process. However, they have coupling problem especially in dense designs. Coplanar wave-guide technique is a better choice to reduce the coupling at high frequencies as shown in Figure 6.9 and Figure 6.10.

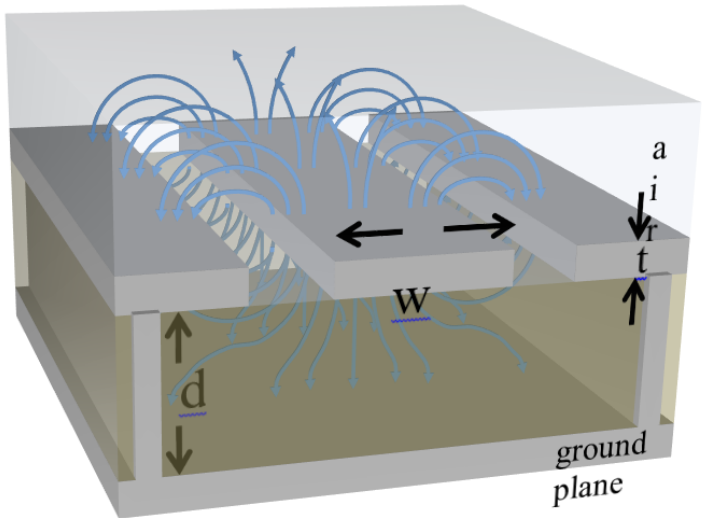

Figure 6.9. Coplanar waveguide.

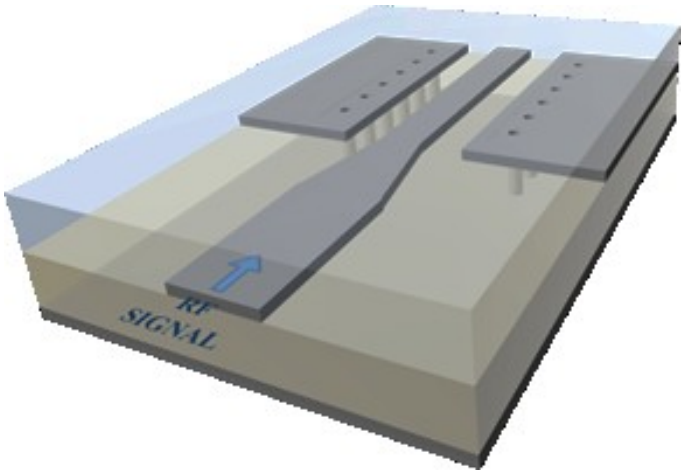

Figure 6.10. Coplanar waveguide.

The coplanar waveguide works like coaxial cable. The signal path is surrounded by ground and the signal travels in a bounded path. Thus, the coupling is much less compared to a microstrip waveguide. The simulation and measurement results are given in the following sections.

6.3.1. Transceiver PCB

Coplanar waveguide technique is applied in all transceiver PCB designs. The picture of the first generation non-coherent transceiver PCB is shown in Figure 6.11. The inputs and outputs of the PCB are labelled. The transmitter output and receiver inputs are placed far away from each other to enable single board operation. 48 pin QFN packaged chip layout is placed at the center of the PCB. The QFN chip is soldered to avoid additional socket parasitics.

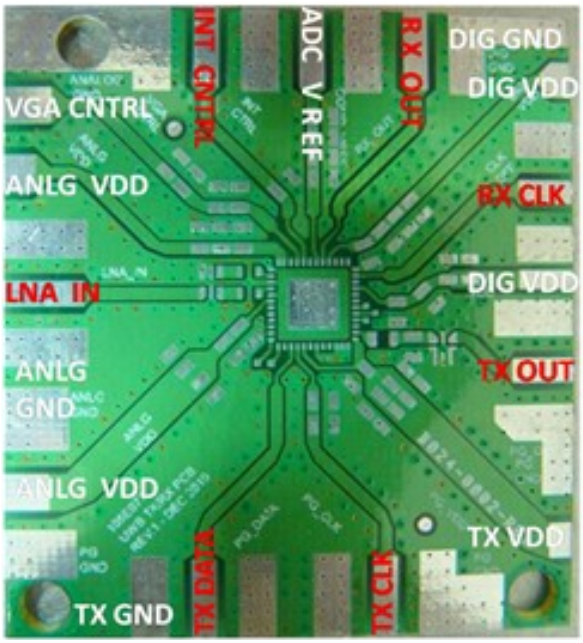

Figure 6.11. Non-coherent transceiver PCB design.

The space between the consecutive vias is determined by the wavelength and hence is a function of the signal frequency. The trace width and the spacing between the signal path and ground are also found by inserting the signal frequency to coplanar waveguide formulas. Measurement results of the designed RF PCB are given in the Figures 6.12- 6.14. The coupling between the inputs and input losses are measured.

The greatest concern during the operation of the IC is coupling of the switching noise from the clock signal to the LNA input. Because the signal received by the antenna is single ended on the PCB, coupling can not be tolerated. Figure 6.12a and

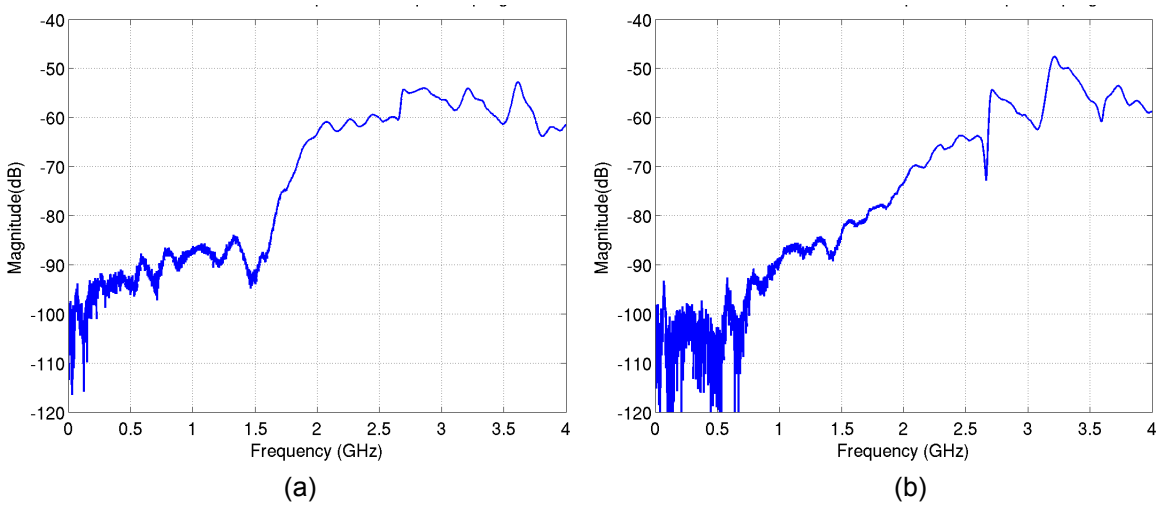

Figure 6.12. Measurements; (a) Coupling between TX DATA and LNA IN. (b) Coupling between TX CLK and LNA IN.

Figure 6.12b show the coupling between the LNA input and the applied data and clock signals, respectively. Maximum applied clock frequency is about 1 GHz and measurements show that coupling is about -90 dB in the 0-1 GHz band. -90 dB is too low to be considered as coupling. Therefore, the coupling problem is resolved by the coplanar waveguide technique.

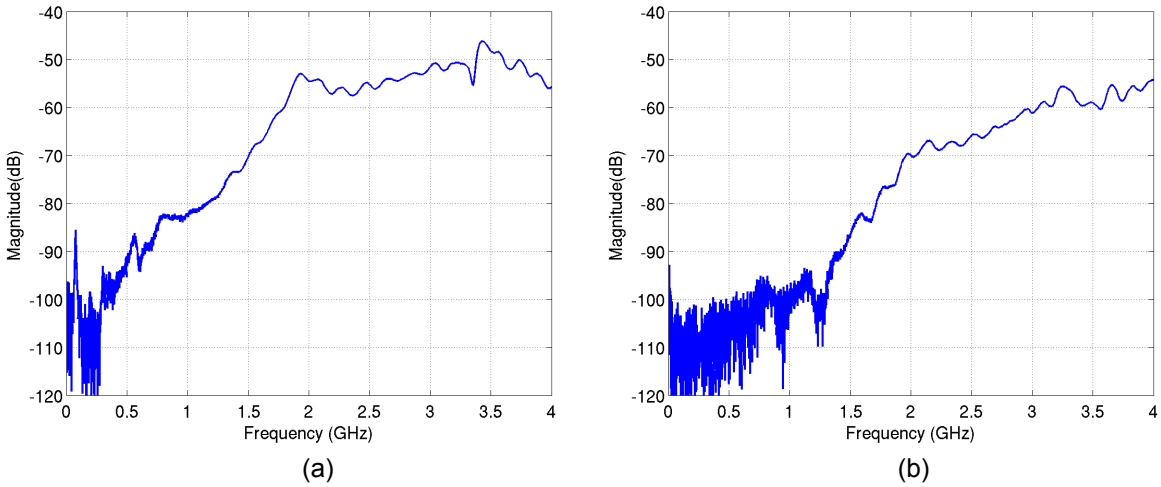

Figure 6.13. Measurements; (a) Coupling between RX OUT and LNA IN. (b) Coupling between TX OUT and LNA IN.

The second consideration is coupling of the pulse generator and receiver output to the LNA input. This is especially critical since the receiver output is closer to the LNA input and it has a fast switching characteristic, creating most of the coupling problem. However, it can be observed from Figure 6.13a and Figure 6.13b that the coupling is less than -50 dB which is still an acceptable value.

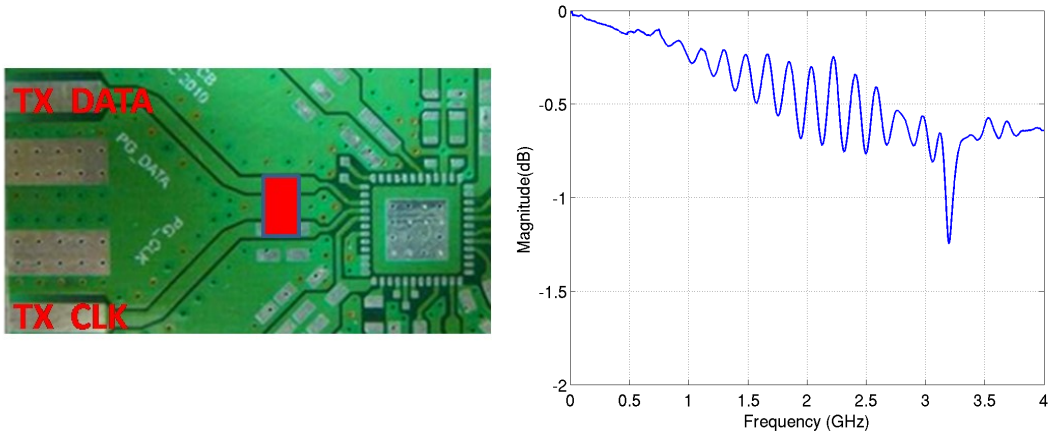

Figure 6.14. (a) Test setup of the short connected traces . (b) Total insertion loss of the short connected traces.

The measurement setup is shown in Figure 6.14a. The traces are connected with a short circuit in order to measure the insertion loss of the coplanar waveguide including the connectors. The results are depicted in Figure 6.14b and the total loss measured is less than 1 dB, which is a good value considering the included loss caused due to the SMA connectors.

6.3.2. Power Board PCB

In the coherent transceiver, there are many bias circuits and V_{DD} supply voltages are placed for low noise operation of the circuit. Thus, a low noise supply is necessary. A commercially available LT 1763 voltage regulator is utilized in the PCB design of the coherent receiver. A power board design is completed including all the bias ports of the receiver. The board also includes a VHDCI port for FPGA connection. The detailed photos are given in the Figures 6.15 and 6.16

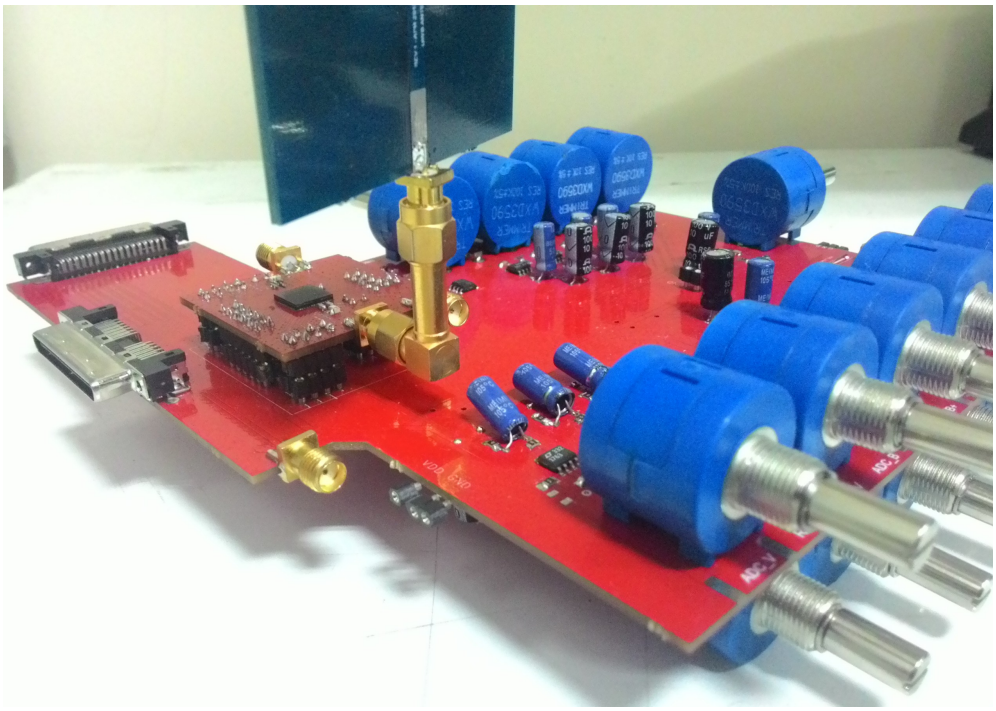

Figure 6.15. Coherent transceiver power board.

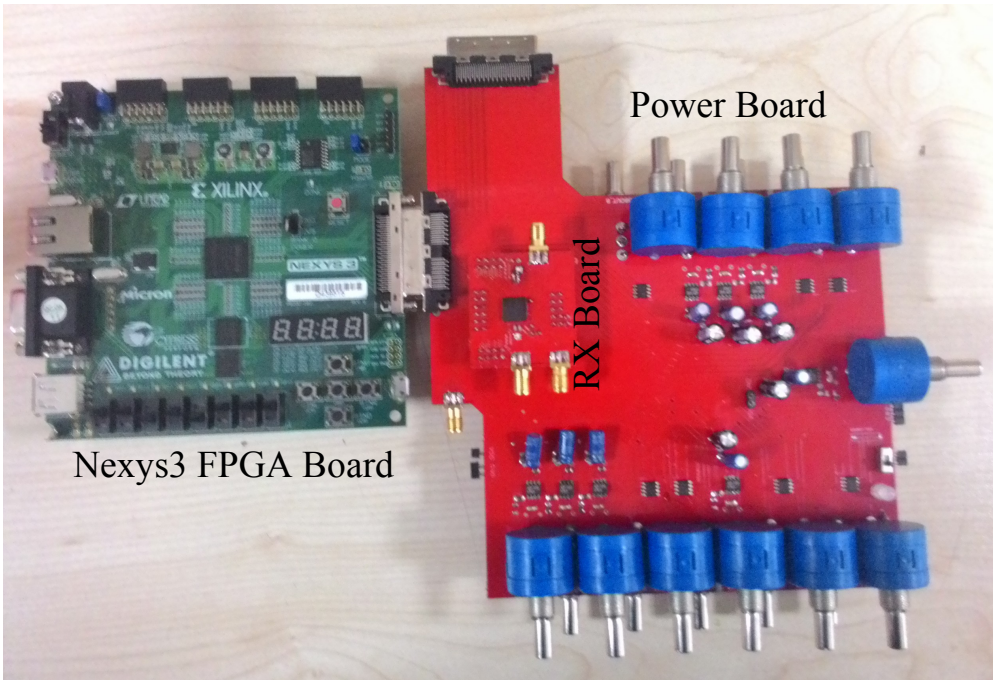

Figure 6.16. Coherent transceiver power and FPGA boards.

6.4. Conclusion

PCB design at high frequency and wide-band applications is a difficult task. The characteristic impedance must be maintained in a wide frequency range and the parameters such as insertion loss and reflection coefficient should match to the specifications of the design. Utilizing QFN package increased the frequency response of the IC. The PCB designs employ co-planar wave-guide technique which minimizes the coupling and satisfies the specifications set by the user in a wide frequency range.

A patch antenna is designed to conduct wireless experiments. The designed antenna has a band pass reflection coefficient characteristics with the help of additional ground back plane patch design. The size of the antenna is designed larger compared to commercial and literature counterparts in order to increase the antenna gain. The measurement results match the simulation results and it is well suited to be used in IR-UWB applications.

7. UWB DEVELOPMENT BOARDS MEASUREMENT RESULTS

7.1. Introduction

Two different UWB approaches were explained in the introduction. As mentioned, OFDM based UWB transceiver systems employ multi-band hopping sinusoidal signalling, whereas pulse based UWB transceivers use very narrow pulses that are in the order of nanoseconds.

Evaluation boards are used to test the performance of both modulation systems under various environment setups. Wisair's development kit DVK 9110 uses the MB-OFDM system with multi-band hopping. On the other hand, Timedomain's PulseON 220 development board is used to test IR-UWB performance.

Spectrum analayzer is used to determine the output power of the development kits (DVKs). Data speed vs distance measurements are also taken. Performance of the DVKs are measured under different environment scenarios.

7.2. Wisair MB-OFDM UWB Development Board

Wisair decelopment kit consists of two printed circuit boards (PCBs) where the bottom PCB acts as a controller for inputs. Radio frequency PCB (RF-PCB) hosts the RF chips and antenna which can be seen in Figure 7.1. Tests are accomplised by using Wisair DV programming environment, where the DVKs can be set to communicate or simply generate UWB signals for user to observe the spectrum. In the following sections, the power and data measurements are given.

Figure 7.1. Wisair Development Board.

7.2.1. Output Power

In order to measure the output power vs. distance, one of the DVKs is programmed to generate a sinusoidal signal in the 3-5 GHz band. The maximum allowed power set by FCC is -41 dBm/MHz. The measurements confirm that this limit is present at 1-2 cm distance with the DVK in test. The distance vs the received power measurements are given in Figure 7.2. Noise level was around -66 dBm, which indicates that the maximum distance can be around 5 m for communication.

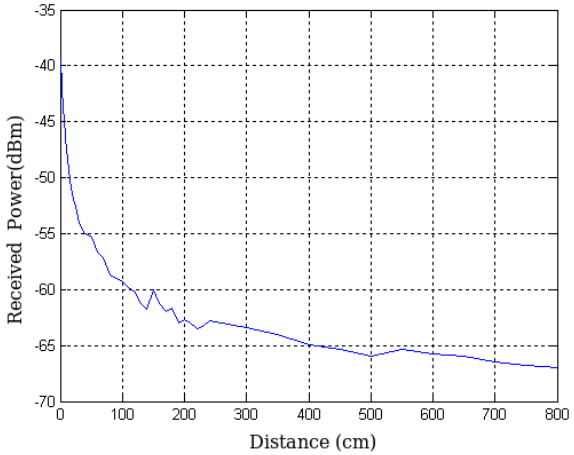

Figure 7.2. Output Power of Wisair Development Board.

7.2.2. Data Speed Performance

In general, the reliable communication distance is around 10 m in MB-OFDM UWB transceivers. However, in the measurements for Wisair DVK 9110 a maximum 4.3 meters distance is observed. These results comply with the power measurements of the previous section.

There are 7 rates (53.3, 80, 106.7, 160, 200, 400, and 480 Mbps) which are selectable in Wisair DVK for communication. The output power changes in order to comply for the spectrum. The output is power reduced in higher data rates which results in short distance.

Measurements are taken using ethernet inputs of the kits. Two notebooks are connected with wireless using ethernet ports and UWB DVKs. In order to achieve maximum data rate, the random access memory (RAM) of the notebooks are used for data transfer storage which are faster than the hard disks. Achievable data rate measurements have been taken for these modes. Since notebooks have 100 Mbps ethernet hardware, data rate will be limited. As a reference, maximum data rate measured was 11.18 MBps (94.4 Mbps) in cable communication. Figures 7.3-7.7 depict data rate versus distance measurements in different DVK data-rate modes.

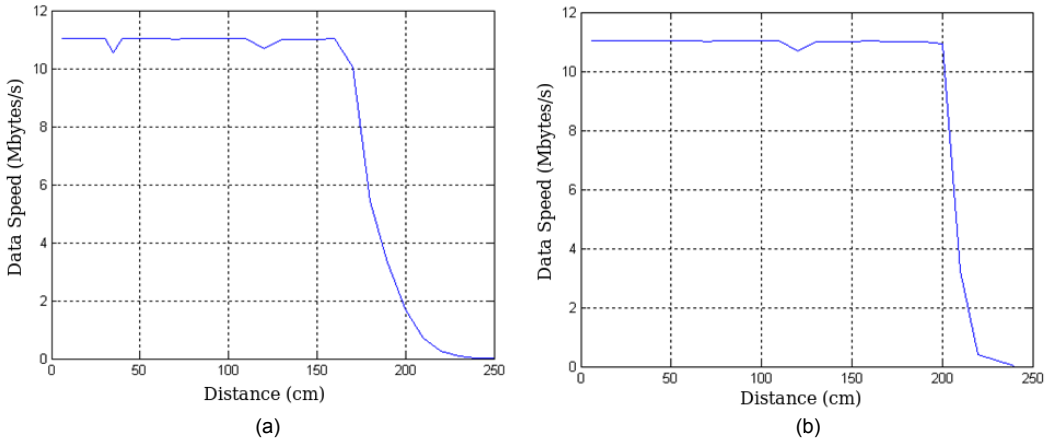

Figure 7.3. Performance of Wisair Board; (a) 480 Mbps mode, (b) 400 Mbps mode.

Maximum data rate at UWB wireless link is measured as 11.05MB/s (88.4Mbps) in Figure 7.3a. Measured data rates versus distance for the remaining speed modes of

the DVK are given in the following figures. One can see that as the speed decreases, the distance increases.

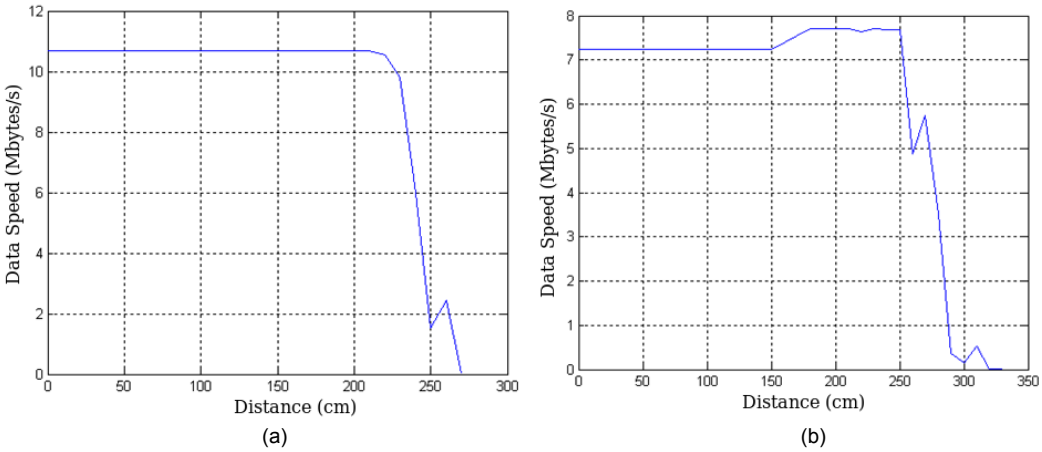

Figure 7.4. Performance of Wisair Board; (a) 320 Mbps mode, (b) 200 Mbps mode.

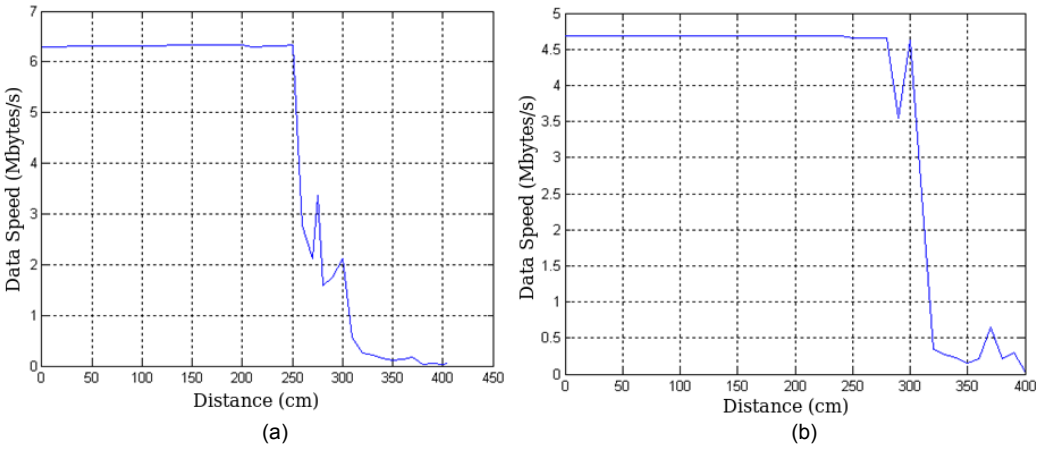

Figure 7.5. Performance of Wisair Board; (a) 160 Mbps mode, (b) 106.7 Mbps mode.

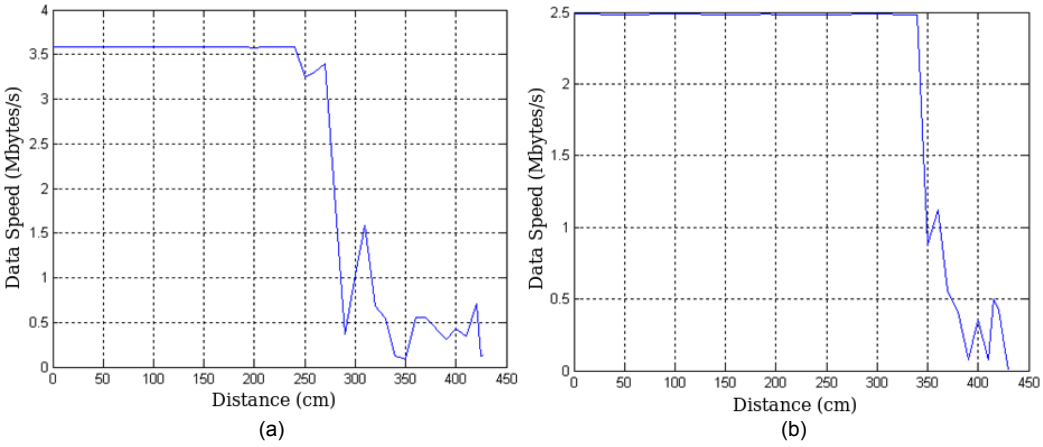

Figure 7.6. Performance of Wisair Board; (a) 160 Mbps mode, (b) 106.7 Mbps mode.

Figure 7.7 gives the overall performance of the DVK. The data is avaliable up to 4.5 meters of distance which is consistent with the spectrum measurements. The

signal level drops down to noise level at around 5m in spectrum measurements as can be seen from Figure 7.2

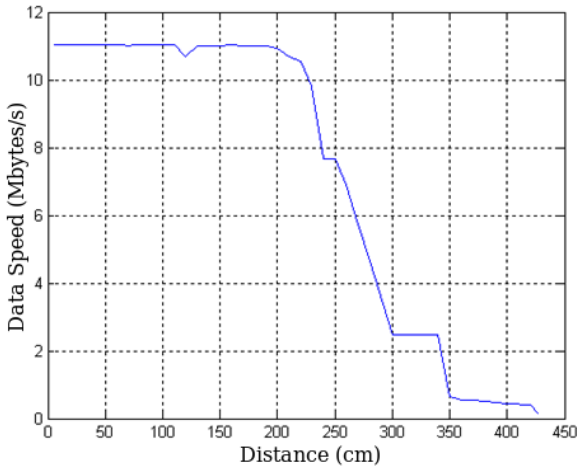

Figure 7.7. Maximum performance of Wisair Board.

7.2.3. Environment Tests

The purpose of the environment tests is to see how well the MB-OFDM UWB signals penetrate through different materials. Measurements are taken with a spectrum analyzer with different objects including concrete, wooden wall and human. At 2 cm distance, the maximum output power of -41 dBm/MHz was measured with Wisair DVK. Measurement results are summarized in Table 7.1.

Table 7.1. Wisair Board Measurements in dBm.

Distance	**No Object**	**Concrete 7 cm**	**Concrete 14 cm**	**Wooden Wall 8 cm**	**Human**
33 cm	-53	-68	-70.2	-	-
66 cm	-57	-68.7	-70.2	-62.6	-70.5
100 cm	-59	-69.4	-70.5	-61.8	-68.5
200 cm	-62.5	-70	-71	-65	-71.8

In the previous measurements, the data transmission was not possible under -66dB signal level. Therefore, it can be observed that communication is possible only

through wooden wall objects. This is an expected result, because MB-OFDM UWB system is using sinusoidal signals, which can not penetrate well through objects.

7.3. Time-Domain Impulse Radio UWB Development Board

The IR-UWB tests are performed with the PulseON P220 Evaluation Kits (EVK) developed by Time Domain Corparation. The IR signals are used as radar signals and they can travel through objects. Similar tests are performed on these IR-UWB EVKs.

In the measurements, maximum data rate of 9.6 Mbps mode is used. Measurements are performed using a software package that is shipped with EVK which is capable of displaying BER and packet error rate (PER). The packet rate is 180 packets/s in 9.6Mbps mode. Measurement results can be found in Table 7.2.

Table 7.2. Obstacle measurements at 1 m with PulsON DVK.

Object	**Packets Sent**	**Packets Received**	**%Rx**
Concrete	109747	106142	97
Human	110799	109614	98.9
Concrete + Human	109758	106164	96.7

Table 7.3. BER vs Distance measurements.

Distance	**Packets Sent**	**Packets Received**	**%Rx**	**BER**
0.3 m	129159	127342	98.6	8.1×10^{-8}
0.6 m	129194	127295	98.5	1.4×10^{-7}
1.2 m	129159	127394	98.6	1.6×10^{-7}
1.8 m	131204	129304	98.5	1.6×10^{-6}
2.4 m	129102	127305	98.6	8.1×10^{-6}
3 m	129076	127274	98.6	8.1×10^{-6}

The communication distance is given around 7 meters in office environment and

20 meters in free space. BER vs distance measurements are performed and results are tabulated in Table 7.3.

Table 7.4. BER vs Distance measurements.

Distance	**Packets Sent**	**Packets Received**	**%Rx**	**BER**
5 m same room	109656	109004	99.4	4.7×10^{-4}
10 m same room	108078	107156	97.7	1.3×10^{-3}
10 m next room	105431	40118	38	2.2×10^{-2}

As can be seen from Table 7.3 the packets are received at each distance with a high reception rate. The BER gradually decreases with distance. It is observed that the BER rapidly increases when the two kits are brought closer then 0.3 meters. Table 7.4 gives office environment measurements up to 10 meters.

7.4. Conclusion

Both IR-UWB and MB-OFDM development kits are tested and compared against data rate, distance and obstacles. The MB-OFDM development boards show superior data-rate performance compared to IR-UWB boards. However, the communication range is only limited to around 5 meters and the reception link is broken in the obstacle measurements. In the case of IR-UWB, the maximum data-rate is limited to 9.6 Mbps. However, the range between the transceiver boards can go upto 100 meters with very good object penetration capabilities. The IR-UWB development board also enables the radar operation. The distance between the transceivers can be measured by time of flight technique using the dedicated software.

8. CONCLUSION AND FUTURE WORKS

In this thesis, two computer aided co-simulation environments have been created for the automated design of MB-OFDM and IR approaches for UWB transceiver designs. The designed CAD tools help designer to manage the system level circuit coefficients and identify their effects on the system performance. Hence, it will shorten the overall design time and help designer to build better transceiver. System and circuit level non-idealities are studied. The effect of the circuit parameters such as linearity and matching on circuit performance are found by the co-simulation environment and circuit designs are revised. Since all of the work is done automatically, the effect of changing a system or a block parameter can be quickly observed.

Existence of impulsive noise is shown in wideband and ultra-wideband channels. Indoor and outdoor EMF measurements are taken and Middleton's Class-A noise models are constructed. Class-A mathematical models and measurement results are in good correspondence. The measurements well fitted to the Middletons's class A impulsive noise model. It has been shown with the extensive noise measurements and models that the effect of impulsive noise over the channel must be considered, while designing a communication hardware for broad-band wireless systems. Therefore, the receiver designed robust to impulsive noise by placing on chip BPF that works both as a matching circuit and as a clipper. High impulsive noise signal's energy is clipped by the BPF. System simulations show that even at the high density of impulsive noise, the receiver successfully detects the transmitted signals.

The VLSI designs of the both coherent and non-coherent IR-UWB transceivers are fabricated using UMC 130 MMRF technology. Two ultra-low power transmitters are designed that can work with solar energy. First transmitter is a dual band design that can also be used in biomedical applications. This transmitter contains a smaller number of components and thus consumes less power than its counterparts such as pulse-combining and oscillator-aided approaches in the literature. Second transmitter is an improved version of the first design. This design is highly configurable with wide

range of operation and dissipates less power compared to the first design. The proposed configurable transmitter can precisely adjust both positive and negative pulse widths as well as the delay between the pulses. Therefore, the proposed transmitter not only has a reasonably good EPP performance but also operate with a wider center frequency range than previous state-of-the-art as demonstrated by extensive measurement results.

In the non-coherent receiver design, a high data-rate low-power IR-UWB architecture is presented with improved range capabilities. Most non-coherent architectures in the literature are designed for low data-rate applications below 20Mbps. The method of using envelope detector together with the energy detector is introduced and the clocking circuitry is avoided which makes it possible to achieve high data rate circuitry with a non-coherent architecture in moderate range applications. The receiver of the proposed non-coherent system employs a mixture of energy and envelope detection. The receiver does not require any synchronization scheme, which helps the receiver to achieve 240 Mbps with 0.2 nJ/bit energy. To the best of our knowledge, this makes the receiver design unique in the literature. Furthermore, three baseband demodulation architectures are proposed for non-coherent receivers. Although baseband digital demodulation architectures are present in the literature, such methods with high throughput have not been presented before.

On the other hand, an ultra low power template based coherent receiver is designed and implemented. The coherent receiver have a better RF-front-end performance compared to non-coherent design both at matching and at the noise figure. The template based receiver has additional blocks such as template pulse generator, configurable delay line, FPGA for synchronization control. The transmitter itself is used as a template generator. A high precision and low jitter Vernier delay line is designed for pulse synchronization. The low jitter, high precision and linearity are the important parameters for IR-UWB receiver systems. In this regard, the proposed delay line architecture has a superior jitter performance compared to the previous work in the literature. Additionally, an active on-chip balun is also designed to reduce the LO-IF leakage. 12 level flash ADC design is constructed to better differentiate signal

from noise. The chip size was limited to 1.5 mm by 1.5 mm. Therefore, the demodulation and digital control is to be controlled by Spartan 6 FPGA which has VHDCI interface that works up to 1 GHZ. The measurements of the coherent architecture are underway by the time of writing the thesis.

PCB design at high frequency and wide-band applications is an daunting task. The characteristic impedance must be maintained in a wide frequency range and the parameters such as insertion loss and reflection coefficient should match to the specifications of the design. Utilizing QFN package increased the frequency response of the IC. The PCB designs utilize co-planar wave-guide technique which minimizes the coupling and satisfies the specifications set by the user in a wide frequency range. Moreover, a power biasing board design has been made for low noise biasing of the test PCB using voltage regulators.

A patch antenna is designed to conduct wireless experiments. The designed antenna has a band pass reflection coefficient characteristics with the help of additional ground back plane patch design. The size of the antenna is designed larger compared to commercial and literature counterparts in order to increase the antenna gain. The measurement results match the simulation results and it is well suited to be used in IR-UWB applications.

The thesis covers most of the topics that is related to IR-UWB transceivers and successful implementations are done with some novel methods and present better performance results compared to the literature.

As a future work, the transmitter design can be revised by utilizing high voltage transistors at the output stage to obtain larger output swing, which helps transceiver to achieve longer communication ranges. This is an important property for the low data rate wireless sensor networks. The transmitter can be configured by the user. A spectrum sensing circuit can be designed for automatically adjusting the configuration registers to obtain robustness.

On the receiver side, more aggressive power reduction can be obtained by utilizing a wake-up circuitry that is applicable both for coherent and non-coherent designs. RF front-end is the most power consuming block. Therefore, the receiver can be put to sleep mode in between the reception of data. The coherent receiver is capable of being operated as a radar, since it utilizes template pulses that are generated at the receiver with the same transmitter architecture. Through-wall imaging and ranging applications are possible with configurable delay line. The minimum delay of the designed Vernier line is around 5 ps, which results in centimetre resolution in radar applications.

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