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MICROPROCESSOR CONTROLLED DETECTION AND DRILLING OF PCB HOLES UTILIZING AN X-Y STAGE SCANNER

by

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To My Mother

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ABSTRACT

The purpose of the thesis is to design and realise a system to detect and simulate the drilling of drilling-hole positions in printed circuit board masks making use of a stepper motor driven mechanical moving stage scanner under the control of microprocessor.

Determination of the print outline and the effective frame length, detection of the dots at proper drilling-hole positions, scanning of the dot mask in a meander pattern, generation of switching sequence of the unipolar stepper motors are under the control of software and achieved by interfacing the stage scanner, drive circuitry of the steppers and the detection system to a Z-80 microprocessor card.

Since all the control actions are performed by the microprocessor, the prototype can be considered as an intelligent system. The drilling part of the software minimizes the drilling process time making use of optimum path algorithm.

ÖZETÇE

Günümüzde, baskılı devrelerin delik delme işlemi devreler deneme safhasındayken miktarların azlığı nedeniyle önemli bir problem oluşturmakta ve kalıp-pin yöntemi masraflı olduğundan delikler el ile delinmektedir. Tezin amacı bu soruna çözüm getirmektir.

Yapılan prototipte baskılı devre üzerindeki delik yerleri işik geçiren bir filme işaretlenerek bu filmin mikro işlemci denetiminde optik yöntemle taranmasıyla saptan makta ve delme işlemi bir ışıkla simüle edilmektedir.

Sistemde kullanılan mekanik tezgah X ve Y yönlerinde adımlayıcı motorlarla hareket ettirilmekte ve tarama işleminde satır yöntemi kullanılmaktadır. Optik sistemin ve motorların tüm kontrolu Z-80 mikroişlemcisi ile gerçekleştirilmiş bir kart tarafından sağlanmaktadır. Geliştirilen sistemde yazılım, delme işleminde zamanı kısaltmak için optimum yol algoritmasını içermektedir.

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The automatic drilling machines for drilling holes in printed circuit boards at positions stored on cassettes are widely used, but the determination of the hole positions often has to be done by hand. For a small series of printed circuit boards, generating the list of drilling positions is a very substantial part of the total production time. Another method but far more primitive, is drilling holes manually, which consumes more time and is less accurate than the aforementioned.

On the other hand, in the near future, Computer Aided Design will become very important, at which time the drilling positions will be known from the design process. However presently many of the layouts are made by hand. So the best way of handling holes of printed circuit boards is by the automatic determination of drilling positions, which is very cost-effective, where a small series of boards is concerned.

The developed prototype has mainly two aspects: One of them is the automatic scanning of the transparent layout with an optic sensor. The other is the simulation of the drilling procedure. For this purpose, a LED is used instead of a drill. Software provides all controls i.e, scanning, detection, the driving of the stepper motors and simulation of the drilling operation. Thus the system does not need any manual work for operation except pushing the start button and provides high accuracy due to precision stepper motors and high resolution optic sensor.

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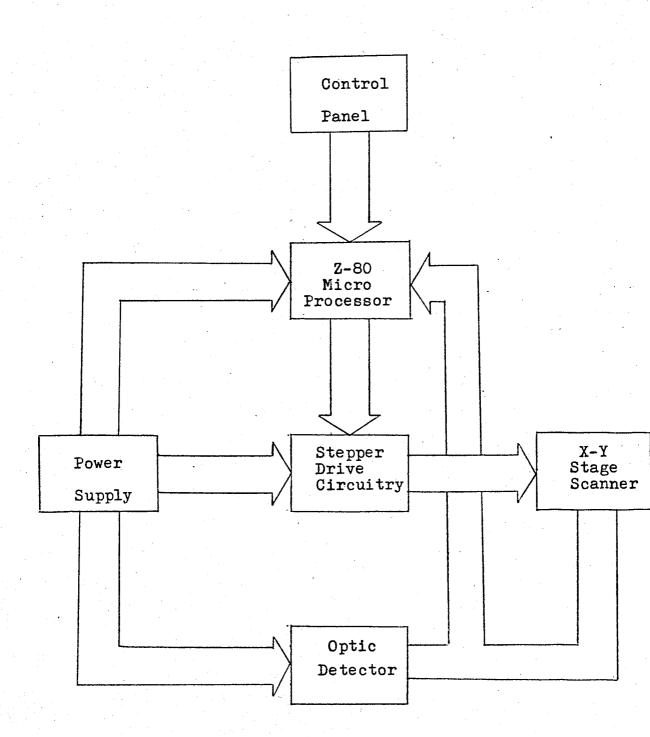


Figure 1.1

System has six main units. Those are:

- 1. Control panel
- 2. Z-80 microprocessor based card
- 3. Stepper drive circuitry
- 4. Mechanical assembly
- 5. Power supply unit
- 6. Optic detector

The above units will be explained in detail in the system hardware section.

II. STEPPER MOTORS

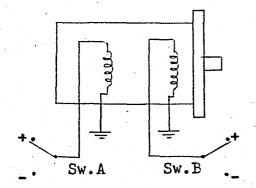
The stepping motor is a device which translates electrical pulses into mechanical movements. The output shaft rotates or moves through a specific angular rotation per each incoming pulse or excitation. This angle or displacement per movement is repeated precisely with each succeeding pulse translated by appropriate drive circuitry. The results of this precise, fixed and repeatable movement is the ability to accurately position. As opposed to a conventioal motor which has a free running shaft, the step motor shaft rotation is in fixed, repeatable, known increments. The stepping motor therefore allows load control ability of velocity, distance and direction. Initial positioning accuracy of a load being driven by a stepping motor is excellent. The repeatability(the ability to position through the same pattern of movements a multiple number of times) is even greater. The only system error introduced by the stepping motor its single step error, and this is generally less than percent of one step. Most significantly this error is cumulative, regardless of distance positioned or number of times repositioning takes place.

A. Construction and Operation

In a typical motor, electrical power is applied to two coils. Two stator cups formed around each of these coils with pole pairs mechanically displaced by half a pole pitch, become alternately energized north and south magnetic poles. Between the two stator-coil pairs the displacement is one fourth of a pole pitch.

The permanent magnet rotor is magnetized with the same number of pole pairs as contained by one stator-coil section. Interaction between the rotor and stator (opposite poles attracting and likes repelling) causes the rotor to move one fourth of a pole pitch per winding polarity change. A two phase motor with 12 pole pairs per stator-coil section would thus move 48 steps per revolution or seven and a half per step.

The normal electrical input is a four step switching sequence as shown in figure 2.1



CW ROT.

STEP	COILA	COILB
1	+	. +
2	+	_
3	-	-
4		+
11	+	+

CCW ROT.

Figure 2.1

Continuing the sequence causes the rotor to rotate forward. Reversing the sequence reverses the direction of rotation. Thus, the stepper motor can be easily controlled by a pulse input drive which can be a two flip-flop logic circuit operated either open or closed loop.

Hereafter some specific names will be used for the stepper motors, so the below terminology will be needed:

1. Step Angle

The motor shaft rotates its specific angular increment each time the winding polarity is changed. This specific degree of rotation or increment is called the step angle. It is specified in degrees.

2. Step Accuracy

Defined as positional accuracy tolerance. This figure is generally expressed in percent and indicates the total error introduced by the stepping motor in a single movement. The error is noncumulative i.e it does not increase as additional steps are taken. In a linear positioning, with a resolution of .001 inches a three percent motor would introduce a maximum of .00003 inches error into the system. This total error would not accumulate nor increase with total distance moved or number of movements made. A particular step condition

of the four step sequence repeatedly uses the same coil, magnetic polarity and flux path. Thus the most accurate movement would be to step in multiples of four since electrical and magnetic inbalances are eliminated. Increased accuracy also results from movements which are multiples of two steps. So, in positioning applications it is better to use two or four steps or multiples thereof for each desired measured increment.

3. Torque

The torque produced by a specific stepper motor depends on several factors:

- i. The step rate
- ii. The drive current supplied to the windings iii. The drive design
- a. Holding Torque. At standstill (i.e zero steps per second and rated current) the torque required to deflect the rotor a full step is called the holding torque.Normally the holding torque is higher than the running torque and thus acts as a strong brake in holding a load. Since def lection varies with load, the higher the holding torque the more accurate the position will be held.
- b. Residual Torque. The non-energized detent torque of a PM stepper motor is called residual torque. A result of the permanent magnet flux and bearing friction, it has a value

of approximately one tenth the holding torque. This characteristic of permanent magnet steppers is useful in holding a load in the proper position even when the motor is deenergized. The position, however will not be held as accurately as when the motor is energized.

4. Step Response

When given a command to take a step, the motor will respond within a specific time period. This step response or time for a single step is a function of the torque to inertia ratio of the motor and of the characteristics of the electronic drive system. Ratings are given for no-load conditions with time generally expressed in milliseconds. Single step response is shown in figure 2.2

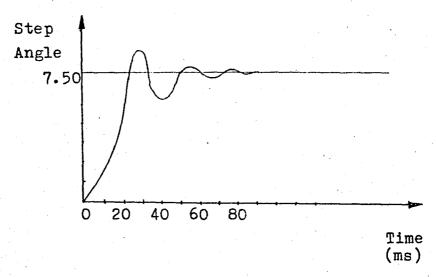


Figure 2.2

5. Resonance

Stepper motors are a spring-mass system and, as such, have certain natural frequency characteristics. When a motor's natural frequency or resonance is reached, an increase in the audible level of the motor's operation can be detected. In cases of severe resonant condition, the motor may lose steps and/or oscillate about a point. The frequency at which this resonance occurs varies, depending on the motor and the load. In many applications it may not occur to any perceptible degree; however, it is felt that the designer should realize that this condition can exist and specific facts about resonant characteristics of an individual motor should Ъe obtained from the manufacturer.

6. Translator

An electronic control with circuitry to convert pulses into the proper switching sequence, resulting in one motor step taken for each pulse received.

7. Preset Indexer

An electronic control which includes the translator function plus additional circuitry to control the number of steps taken as well as direction and velocity.

8. Ramping

The process of controlling pulse frequency to accelerate the rotor from zero speed to maximum speed as well as to decelerate the rotor from maximum speed to zero speed. Ramping increases the capability of driving the motor and load to higher speed levels, particularly with large inertial loads. A typical acceleration control frequency plot for an incremental movement with equal acceleration and deceleration time would be as shown in figure 2.3

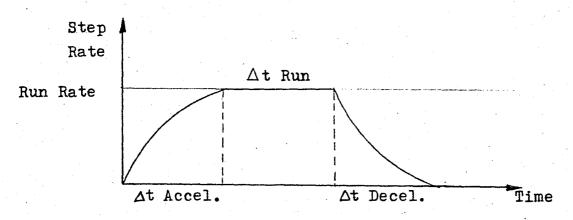


Figure 2.3

Ramping acceleration or deceleration control time allowed:

$$T_j$$
 (Torque mNm) = $J_t \cdot \Delta V \cdot K$

Where $J_t = Rotor inertia (g.m²) plus load inertia$

 $\triangle V$ = Step rate change

 Δt = Time allowed for acceleration in sec.

 $K = \frac{2\pi}{\text{Steps/rev}}$

9. Start / Stop Without Error

The start without error curve shows what torque load the motor can start and stop without loss of a step when started and stopped at a constant step or pulse rate. The running curve is the torque available when the motor is slowly accelerated to the operating rate. It is thus the actual dynamic torque produced by the motor. This curve is sometimes called the slew curve. The difference between the running and the start without error torque curves is the torque lost due to accelerating the motor rotor inertia. A typical torque versus step rate characteristics curve is shown in figure 2.4.

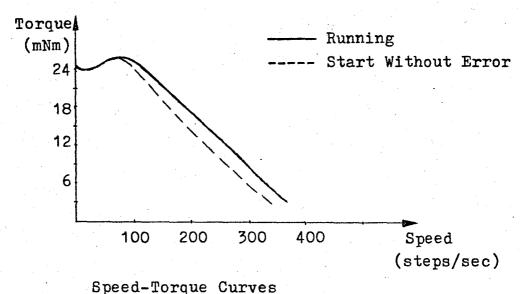


Figure 2.4

10. Slew Rate

An area of high speed operation where the motor can run unidirectionally in synchronism. However it cannot instantaneously start, stop or reverse. A stepping motor is brought up to a slewing rate using acceleration and is then decelerated to a stop under conditions where no step loss can be tolerated.

11. Damping

The reduction or elimination of step overshoot is defined as damping. It is used in applications where settling down time is important. In figure 2.5 electronically damped response is shown.

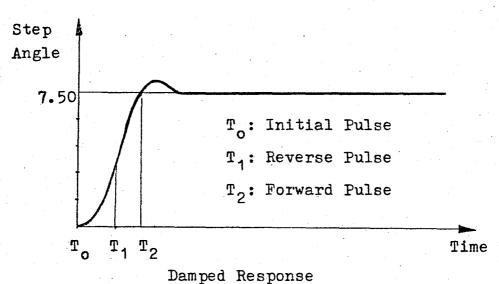


Figure 2.5

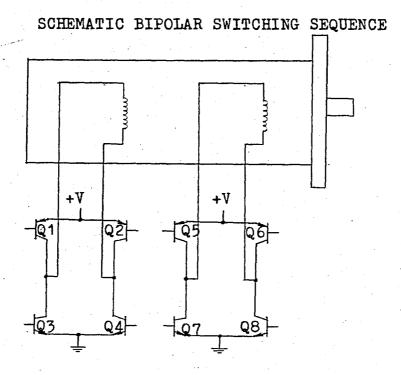
B. Drive Methods

1. Bipolar

The stator flux with a bipolar winding is reversed by reversing the current in the winding. It requires a push-pull bipolar drive. Care must be taken to design the circuit so that the transistors in series do not short the power supply by coming on at the same time. Properly operated, the bipolar winding gives the optimum motor performance at low to medium step rates.

2. Unipolar

A unipolar winding has two coils wound on the same bobbin per stator half. Flux is reversed by energizing one coil or the other coil from a single power supply. The use of a unipolar winding, sometimes called a bifilar winding allows the drive circuit to be simplified. Not only are half as many power switches required (four vs. eight) but the timing is not as critical to prevent a current short through two transistors as is possible with bipolar drive. For a unipolar motor to have the same number of turns per winding as a bipolar motor, the wire diameter must be decreased and therefore the resistance increased. As a result unipolar motor have 30 percent less torque at low speeds. However at higher rates the torque outputs are equivalent.



Step	Q ₁ -Q ₄	Q ₂ -Q ₃	Q ₅ -Q ₈	Q ₁ -Q ₇
1	ON	OFF	ON	OFF
2	ON	OFF	OFF	ON
3	OFF	ON	OFF	ON
4	OFF	ON	ON	OFF
1	ON	OFF	ON	OFF

Normal
4 Step Sequence

		CW
ROT	AT:	ION

1	ON	OFF	ON	OFF
2	ON	OFF	OFF	OFF
3	ON	OFF	OFF	ON
4	OFF	OFF	OFF	ON
5	OFF	ON	OFF	ON
6	OFF	ON	OFF	OFF
7	OFF	ON	ON	OFF
8	OFF	OFF	ON	OFF
1	ON	OFF	ON	OFF

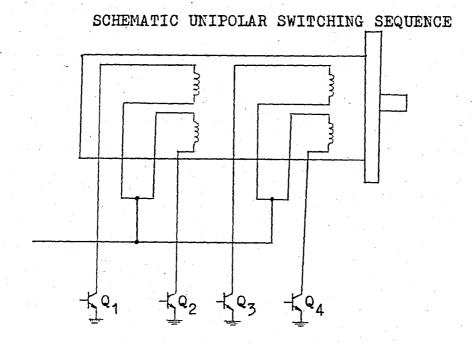
ROT. 1/2 Step 8 Step Sequence

CCW

1	ON	OFF	OFF	OFF
2	OFF	OFF	OFF	ON
. 3	OFF	ON	OFF	OFF
4	OFF	OFF	ON	OFF
1	ON	OFF	OFF	OFF

Wave Drive 4 Step Sequence

Figure 2.6



Step	Q ₁	Q ₂	Q ₃	Q ₄
1	ON	OFF	ON	OFF
2	ON	OFF	OFF	ON
3	OFF	ON	OFF	ON
84	OFF	ON	ON	OFF_
1	ON	OFF	ON	OFF

Normal
4 Step Sequence

	1	ON	OFF	ON	OFF
	2	ON	OFF	OFF	OFF_
	3	ON	OFF	OFF	ON
	4	OFF	OFF	OFF	ON
CW	5	OFF	ON	OFF	ON
ROTATION	6	OFF	ON	OFF	OFF
	7	OFF	ON	ON	OFF
	8	OFF	OFF	ON	OFF
	1	ON	OFF	ON	OFF

1/2 Step 8 Step Sequence

CCW ROT.

ON OFF OFF OFF OFF OFF 2 OFF ON OFF ON OFF OFF 3 4 OFF OFF ON OFF ON OFF OFF OFF

Wave Drive
4 Step Sequence

Figure 2.7

3. L / R Drive

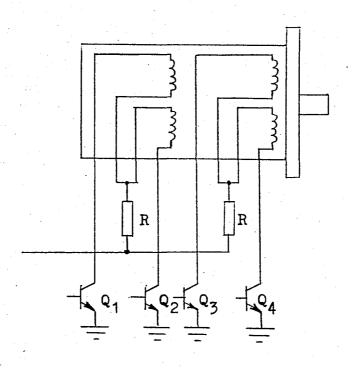
A motor operated at a fixed rated voltage decreasing torque curve as the frequency or step rate increases. This is due to the fact that the rise time of the coil limits the percentage of power actually delivered to the motor. This effect is governed by the inductance to resistance ratio of the circuit (L/R). Compansation this effect can be by either increasing the power supply voltage to maintain a constant current as the frequency increases, or by raising the power supply voltage and adding a series resistor as is shown in Fig. 2.8. As the L/R changed, more total power is used by the system. The series resistors, R, are selected for the L/R ratio desired. L/4R they are selected to be 3 times the motor winding resistance with a:

Watts rating = (Current per winding)² x R The power supply voltage is increased to 4 times motor rated voltage so as to maintain rated current to the motor. The power supplied will thus be 4 times that of a L/R drive. The unipolar motor which has a higher coil resistance thus has a better L/R ratio than a bipolar motor.

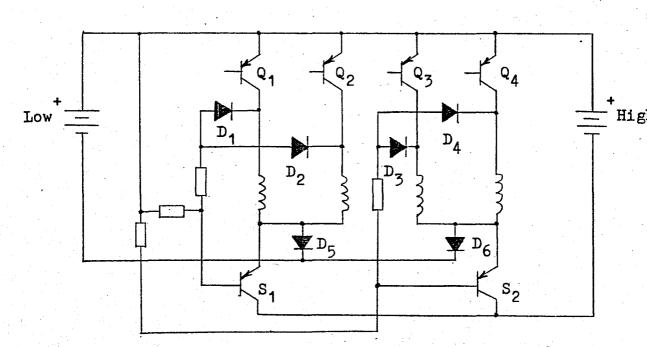
4. Bi-Level Drive

The bi-level drive allows the motor at zero step per second to hold at a lower than rated voltage, and when stepping to run at a higher than rated voltage. The high voltage may be switched on through the use of a current

sensing resistor or a circuit which uses the inductively generated turnoff current spikes to control the voltage, is used.



L/R Drive Figure 2.8



Unipolar Bi-Level Drive
Figure 2.9

5. Chopper Drive

A chopper drive maintains an average current level through the use of a current sensor which turns on a high voltage supply until an upper current value is reached. It then turns off the voltage until a low level limit is sensed where it turns on again. A chopper is best for fast acceleration and variable frequency applications. It is more efficient than a constant current amplifier regulated supply. The supply voltage of choppers is generally five to ten times the motor voltage rating.

6. Wave Drive

Energizing one winding at a time is called wave excitation. It produces the same increment as the four-step sequence. Since only one winding is on, the hold and running torque with rated voltage applied will be reduced thirty percent. Within limits, the voltage can be increased to bring output power back to near rated torque value. The advantage of this type of drive is increased efficiency while the disadvantage is decreased step accuracy.

C. Characteristics of Steppers Used In The System

In the prototype system stepper motors are supplied

from Oriental Motor Company. Specifications of the motors are as follows:

Type : PH296-03

Voltage : 14 V

Current per phase : 0.7 A/phase

Holding Torque : 123 N-cm

Resistance per phase : 20 ohm/phase

Inductance per phase : 60 mH/phase

Rotor Inertia : 560 g-cm²

Weight : 1.5 kg

Step Angle : 1.8

Construction Type : Hybrid

No. of phase : 2

Shaft Type : Single

Temperature Range : -10°C to 50°C

Temperature Rise : 80 C or less

Insulation Type : Class B

Insulation Resistance : 100 Mohm at 500 VDC

Dielectric Strength : Withstands in normal when

impressing 0.5 kV at 60 Hz

between the windings and

the frame for one minute.

The other characteristics and graphs are in Appendix B.

III. SYSTEM HARDWARE

The developed system mainly consists of five units:

- 1. Mechanical assembly
- 2. Stepper motor drive circuitry
- 3. Z-80 Microprocessor based card
- 4. Power supply unit
- 5. Optic detector system

A. Mechanical Assembly

The realization in recent times of the need to implement efficient usage of manpower through improvement in production processes by automation has led to the development of devices such as the X - Y table.

The X - Y stage scanner facilitates the motion of the object to be positioned in either or both the X and Y axes. Obviously there are many methods to design a right angled motion table. Many factors need becarefully considered before deciding on a particular design. The factors are important in the sense that they determine the accuracy and reliability of the equipment. The motions are controlled by motors and the precision required in this application is obtained by using stepper motors which are driven by pulses that can easily be

generated by drive circuits receiving single pulses from Z-80 microprocessor card.

Stepper motors give a very high precision motion depending on the lead - screw used to drive the table. The pitch of the lead - screw determines the amount of linear motion of the table per step of the motor. The main disadvantage of using lead - screw mechanism is backlash. Of course there are some methods to prevent this disadvantage e.g using adjustable nut or spring system.

In the developed system backlash did not cause any problem so compensating methods were not applied.

B. Mechanical Design

1. Base Plate

The base plate supports the entire assembly. Aluminium is preferred due to strength and light property of this metal. Dimensions of this plate are: 260mm x 350mm x 4mm. The base plate supports two other plates at right angles and those plates have shafts and lead-screw mounted on them.

2. Intermediate Y - Plate

This is also made of aluminium. Its dimensions are as follows:

330 mm x 110 mm x 4 mm. This plate is placed on the linear motion bearings and the nut which are in turn mounted on shafts and lead-screw. This intermediate plate supports the other plate (Y - Table) which has dimensions: 420 mm x 195 mm x 4 mm and this supports the other two plates at right angles which are connected to the shafts and the lead screw.

3. Intermediate X - Plate

This plate is supported on the nut and the linear motion bearings which are mounted on shafts and the lead-screw. The dimensions of this plate are: 110 mm x 195 mm x 4 mm. This plate supports the top X-Plate which has dimensions 290 mm x 220 mm x 4 mm.

4. Linear Motion Bearings with Cylindrical Shafts

The best way is to use linear bearings to provide smooth movements. These bearings move along their shafts and are designed to give a smooth movement, which has extremely low friction. The X and Y tables are straight away mounted on these bearings and the lead-screws move the tables on those bearings giving perfect motion.

In order to have a robust system two shafts for the Y - table and two shafts for the X - table are used. Four bearings support each table. This means two bearings on

each shaft. The shafts are made out of steel. The length of the X-table shafts is 400 mm and that of the Y-table is 320 mm. The diameter of both shafts is 16 mm.

Iko linear motion bearings (No. D-16) were selected and placed inside of aluminium blocks to support the X and Y tables. The shafts of both the X and the Y tables are supported by two other blocks at each end.

5. Lead - Screw and Its Nut

The most significant part of the X - Y table is the realization of the lead-screw and its nut. The pitch of the lead-screw determines the linear distance through which the X - Y stage scanner moves. The lead-screw moves in a nut and in the prototype, together they have virtually no back-lash. The lead-screw has eight threads per inch, therefore the motor shaft needs to make eight revolutions to linearly displace the given X-Y table by one inch. Every revolution of the motor is made as a series of 200 steps i.e 1600 steps of the motor produce a linear displacement of one inch or one step produces 1/1600 inch displacement of the table i.e 0.015875 mm. This is the resolution of the prototype X-Y positioning table.

The nut is fixed under both the X and Y tables and the rotating lead-screw will move through the nut. Since the lead-screw motion is restricted to rotation only, it will cause the nut and hence the table to move linearly along the axis of the lead-screw. Since the length of the lead-screw is too long it is safer to give it some kind of radial bearing

support. These bearings allow the lead-screws to rotate within them i.e the lead-screw will move within the bearing and at the same time will be supported by the bearing support. The lead-screw is suitably machined so that the support bearing fits on to the lead-screw perfectly. These bearings are fixed with some supports that are produced in the workshop of the university.

6. Motor Shaft, Lead - Screw Couplings

The power from the motor is transmitted to the leadscrew by coupling the motor shaft into the lead-screw and the combination is tightened by two screws which have housings on the lead-screw shaft.

The X and Y table motors are mounted to the block where two shafts and lead-screw are mounted. For this purpose four screws for each motor are used through the metal spacing units. At this point the important thing is the adjustment of the levels of the motor shaft and the lead-screw. In the developed system this levelling did not cause any problem due to design.

7. Glass Plate

This is the top part of the X-Y table which is placed on the X plate by using metal spacing units at all the four corners of the X-table. The aim of this spacing is to install the light source under the sample film to be scanned. So, the order of the units from top to bottom is: optic detector, sample film, glass plate and the X-plate. The distance between the glass plate and the X-table is 32 mm. The dimensions of the glass plate are 270 mm x 220 mm x 4 mm.

8. Operation

Every pulse input from the microprocessor card to the drive circuit makes the stepper motor rotate through one step or 1.8 degrees. Hence a total of 200 pulses, input to the drive circuit cause the motor shaft to make one revolution.

The scanning area of the X-Y table is defined by the length of the shafts. The developed system can scan an area which has an X-length of 220 mm and a Y-length of 150 mm.

The details related to the mechanical assembly are given in the appendix C.

C. Stepper Motor Drive Circuitry

The drive methods for stepper motors are explained in chapter 2. It the second chapter. It can be easily understood that the drive circuitry affects the speed-torque characteristics of the steppers.

In order to have a proper drive, first the mechanical characteristics of the system must be considered, and then the selection of right stepper motors drive circuitry.

The best way to approach this problem, is to examine the speed-torque characteristics curves, and then settle the load specifications. If no acceleration is needed and the load is frictional, start-without-error curve should be used. The running curve, in conjunction with the equation:

 $T = I \propto$

where

T = Torque

 α = Angular acceleration

I = Inertia

must be considered when the load is inertial and/or acceleration control is needed.

In the prototype system, X-Y stage scanner moves on linear motion bearings which have very little friction, hence the system does not need large amount of torque output from the motor, except that it needs high speed due to time consuming high resolution scanning.

Since the stepper motors are supplied before the realization of X-Y stage scanner, they are ordered from the powerful series. Thus it was a must to have a powerful drive

stage to run these steppers at the required high speed.

The speed versus torque characteristics show that the steppers used in this project have the highest torque output at approximately hundred pulses per second. In addition to this, from the inertia versus starting-pulse-rate characteristics, it is seen that the maximum starting-pulse-rate is around two hundred pulses per second, and sometimes it is advisable to start with half of this speed in order not to lose any steps.

Under these circumstances, when all the drive methods are examined, the most suitable drive type seems to be the chopper drive.

In the chopper drive, current is sensed by a current sensing resistor which turns on a high voltage supply as soon as the current reaches 0.7 amperes and turns it off when the current falls below this value.

The prototype system as mentioned above needs acceleration, high speed and deceleration to save time. For this purpose it is appropriate to give some explanation about stepper's behaviour at variable frequency applications.

The torque output of the stepper motors needed to move the X-Y table is directly proportional to the current that passes through the coils of stepper motor. So, at high speed applications current cannot easily reach its rated value when normal supply voltage is used. It is very logical from the basic equation V = I Z that, in order to have high currents through a coil showing an impedance Z, voltage must attain higher values.

The rise of current depends on the L/R time constant. This can be expressed by the following formula:

$$I = I_f (1 - e^{-\frac{t_1 R}{L}})$$

where

I shows the value of current at time $\mathbf{t_1}$, and $\mathbf{I_f}$ represents the final value of current

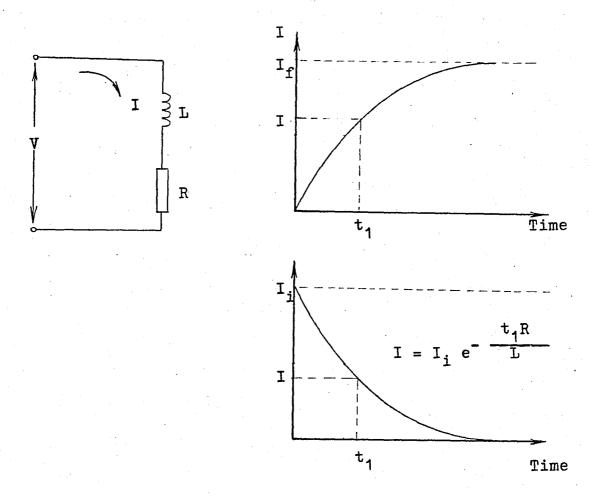


Figure 3.1

Current reaches around 60 percent of its final value at time t=L/R during charging. Discharge process can be viewed as the opposite of charging process. For example in the prototype the rated voltage of stepper motors is 14 V and their resistance per phase is 20 ohms and inductance per phase is 60 mH.

According to these data, the current reaches its 60 percent of its final value at time t=L/R.

$$I_f = \frac{V}{R} = \frac{14}{20} = 0.7 A$$

$$I = 0.42 A$$
 at $t=L/R$

On the other hand, if high voltage (e.g 42 V in the prototype) supply is used:

$$I_{f} = \frac{42}{20} = 2.1 \text{ A}$$

$$I = 1.26 A at t=L/R$$

It can be seen from these rough calculations that the current can reach three times high a value when it is driven from the higher voltage supply in spite the fact that the time interval does not change i.e t=L/R.

Considering all these advantages a modified version of chopper drive is used. It somewhat behaves like a bi-level drive which is also mentioned in chapter two.

In the developed system:

$$V = 42 V$$

R = 20 ohm

L = 60 mH

I = 0.7 A

So the time required to attain a current of 0.7 A is 0.0012 s. As a result, a speed of 835 pulse per second is obtained.

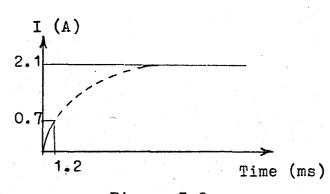


Figure 3.2

Referring to the figure 3.3 where two different supply levels are seen, the high voltage supply (42 V) is connected to the stepper motor windings through Q_1 and Q_2 power transistors. These transistors stay on, till the final value of winding current (0.7 A) is reached. Then Q_{11} , Q_{12} conduct and Q_1 and Q_2 go into cut off and some power is dissipated through the R_1 and R_2 . At this time, the second low voltage (18 V) supply takes over the current and dissipation of Q_1 and Q_2 is avoided.

The diodes D_1 and D_3 are used to prevent the reverse biasing of Q_1 and Q_2 . There can be seen two fuses (F_1,F_2) to protect the system. D_2 (zener), D_4 (zener), D_5 , D_6 , D_7 , D_8 are used for voltage suppression. Also D_9 , D_{10} , D_{11} , D_{12} prohibits the negative pulses that may come from the windings due to the magnetic field created by the rotating permanent magnet rotor. Whenever winding current is turned off, a high voltage inductive spike will be generated which could damage the drive circuit switching transistors.

The above mentioned inductive spike results as per the inductor voltage equation :

$$V = L \frac{dI}{dt}$$

where a high value of rate of change of current is encountered due to an extremely small switching time interval.

The normal method used to suppress these spikes is to put a diode (Free Wheeling diode) across each winding. This, however, will reduce the torque output of the motor unless the voltage across the switching transistors is allowed to build up to at least twice the supply voltage. The higher this

voltage the faster the induced field and current will collapse and thus the better performance. In the prototype circuit 120 V zener diodes are used for this purpose. Diodes D_{13} and D_{14} avoid the reverse currents to the low level supply (18 V).

The second supply is set to 18 V, since there will be a 14 V drop on the motor windings, 0.7 V on the diodes (D_{13} and D_{14}), 2.5 V collector to emitter voltage drop on the transistors (Q_4 , Q_5 , Q_8 , Q_9) and 0.7 V on the current sensing resistors (R_9 and R_{10}).

The pulse sequence from the microprocessor card taken as output from the peripheral device (PIO) is fed to the bases of Q_3 , Q_6 , Q_7 , Q_{10} through the base resistors R_3 , R_4 , R_5 and R_6 .

Ofcourse there are some limitations due to the stepper motor characteristics beside the drive method. Increasing the voltage to a stepper motor at standstill or low stepping rates will produce a proportionally higher torque until the magnetic flux paths within the motor saturate. As the motor nears saturation, it becomes less efficient and thus does not justify the additional power input.

The maximum speed a stepper motor can be driven is limited by hysteresis and eddy current losses. At some rate, the heating effects of these losses limits any further effort to get more speed or torque output by driving the motor harder.

The realised driving cicuitry improved the speed characteristics of the stepper motors which are not very suitable for high speed applications. During scanning a speed of 835 pulse per second is reached by means of this modified chopper drive circuit.

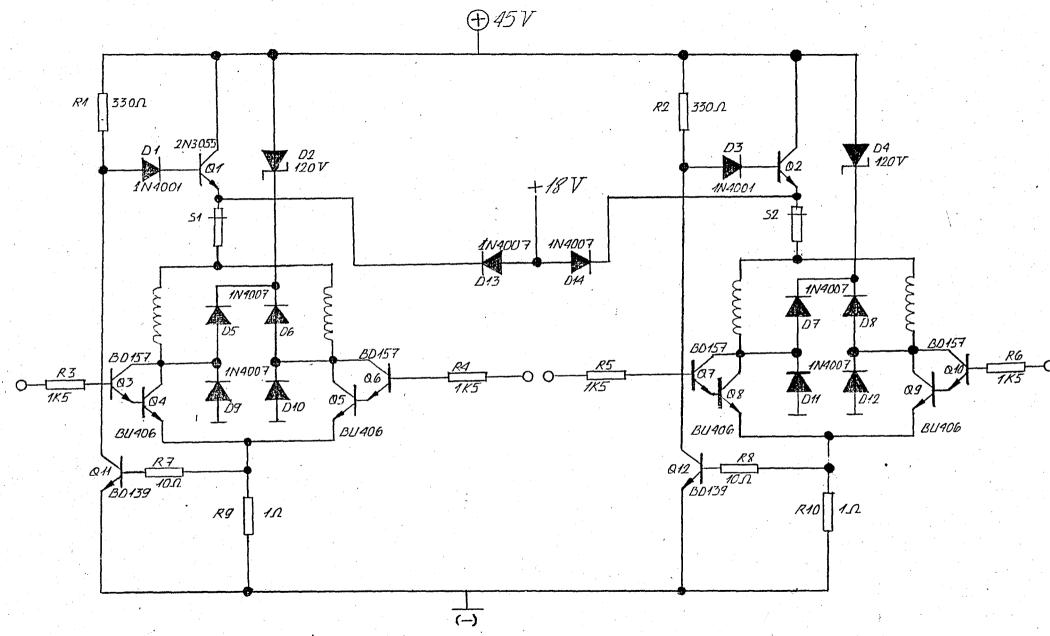


Figure 3.3 Stepper Motor Driving Circuitry

D. Z-80 Microprocessor Based Card

This card consists of four main parts:

- 1. Z-80 CPU
- 2. Z-80 PIO
- 3. Memory Section
- 4. Other IC's

1. Z-80 CPU

All controls are carried out by this unit. It works with a 2 MHz clock. This frequency obtained from a D-type flip-flop which divides the 4 MHz crystal frequency. The Reset input of the CPU is used through a D-type flip-flop also. The non-maskable interrupt, Wait and Bus Request inputs are connected to the V_{CC} by the pull-up resistors. The Halt state is shown by driving a PNP transistor which is used to turn on the LED.

2. Z-80 PIO

The Z-80 parallel input-output circuit is a programmable, two port device which provides a TTL compatible interface between peripheral devices and the Z-80 CPU. The CPU can configure the Z-80 PIO to interface with a wide-range of peripheral devices. In the prototype an 8 bit output is used to give the step sequence of motors, 4 least significant bits are controlling the X-motor, while the most significant

4 bits controlling the Y-motor.

The other port (B) is used as an input port during the scanning process and as an output port while simulation of the drill process. The circuit shown in the figure 3.4 is used for simulation making the LED flash when the detector (simulating the drill) comes on to the dot which should be drilled.

3. Memory

System uses three memory units. Two of them are $2k \times 8$ bit EPROMS (2716 type) and the other is a $2k \times 8$ bit static RAM (6116 P-3 type).

The storage size of the 2k RAM limits the card size to 170 mm x 140 mm despite that the maximum scanning area is 220 mm x 150 mm (X,Y) mechanically. Along with the hole position storage, a part of the RAM acts as a stack and also as a scratch-pad for the program.

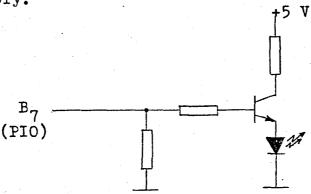
The memory addresses of the system are decoded as follows:

EPROM 1 $\phi \phi \phi \phi$ - $\phi 7 F F$ EPROM 2 $\phi 8 \phi \phi$ - $\phi F F F$ RAM $8 \phi \phi \phi$ - 87 F F

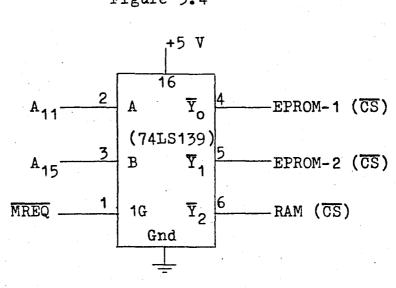
This decoding is performed by one half of a 74LS139 (Decoder/Demux). Inputs of this IC are supplied from the address pins (A_{11} and A_{15}) and $\overline{\text{MREQ}}$ pin of CPU. \overline{Y}_0 , \overline{Y}_1 , \overline{Y}_2 outputs of the decoder select the EPROM 1, EPROM 2 and RAM

respectively, as shown in the figure 3.5

The output enable pins of EPROMS and RAM are connected to the $\overline{\text{RD}}$ pin of CPU. The RAM output enable pin has connection with the $\overline{\text{WR}}$ pin of CPU to perform writing operations into the memory.



Drill Simulator
Figure 3.4



Address Decoding
Figure 3.5

4. Other IC's

The other IC's perform the interrupt action as follow System interrupt mode is set to 2 to have control inputs for

the X-Y table movements. In mode 2 system creates 16 bit starting address of the service routine. The programmer maintains a table of 16 bit starting addresses for every interrupt service routine. This table may be located anywhere in the memory. When an interrupt is accepted a 16 bit pointer must be formed to obtain the desired interrupt service routine's starting address from the table. The upper 8 bits of this pointer are formed from the content of the I-register. The I-register must have been previously loaded with the desired value by the programmer. In the developed board . the lower 8 bits of the pointer are supplied by the interrupting switches. The point to note is that only 7 bits can be used leaving the least significant bit zero. This is needed since the pointer is used to get two adjacent byte to form a complete 16 bit service routine's starting address and the addresses must always start in even locations.

In the Z-80 hardware layout given in the appendix, this interrupt mode works as follows: When one of the switcher connected to interrupt inputs is drawn to ground, the NAND gate output goes high and sends a 1.3 microsecond interrupt pulse through the capacitor and resistor network, meanwhile the Octal Transparent Latch (74LS373) is enabled and it latches the data on its input. Meanwhile the CPU generates an INTA signal which enables the latch output, hence the data is loaded on the data bus. As mentioned before, this data form the lower 8 bits of the 16 bit starting address of the service routine. Then the CPU executes the program from that address on.

E. Power Supply Unit

This unit is made up of four main parts:

1. The High Voltage Supply

This supply uses 32 VAC input. After rectification and capacitive filtering, this unit is connected to the high voltage pin of the drive card. For this part of the supply no regulator is used since inductive spikes that are created due to high speed switching of the drive card, may damage the regulator circuit besides that there is no need for such regulation as far as drive cicuit structure is concerned. The output of this supply is 45 V at no load conditions, and at loading it falls to 42 V that is sufficient for the drive card.

2. The Low Voltage Supply

After rectification and capacitive filtering 25 VDC is fed to the input of integrated voltage regulator (7818). The output (18 VDC) is used as the low level supply and approximately 350 mA current is drawn by the drive circuitry. This second supply is needed to have bi-level drive for the stepper motors, so it provides current at low speeds (246pps) mostly and prevents the dissipation of transistors (Q₁ and Q₂) due to high voltage, by keeping them at the cut off.

If the low voltage supply were not included in the power supply unit, then, after the inductor current reaches its rated value (0.7 A), there would be a voltage on the transistors (V_{CE}) Q_1 and Q_2 which is equal to 42-17=25 V where

42 V = The high voltage supply

17 V = Voltage drop on the motor windings + V_{CE} of switching transistors (Q_4 , Q_5 , Q_8 and Q_9) + Voltage drop on the current sensing resistors (R_9 and R_{10})

Thus this voltage (25 V) with the rated current of motor windings, would cause approximately 17.5 W power dissipation on the transistors Q_1 and Q_2 .

3. + 5 Volt Supply

The output of 18 V voltage regulator is also taken as the input for +5 V regulator (7805).

+5 V supply is used for the Z-80 microprocessor card, for the drill simulator circuit and also for the detection circuitry. The amount of current that is drawn from this supply is approximately 250 mA.

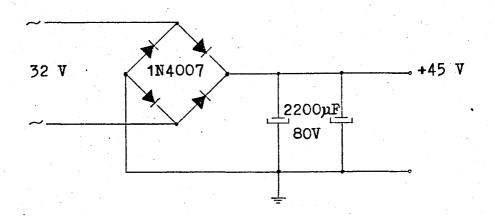
4. Adjustable Voltage Supply

This adjustable voltage regulator (723) also uses
18 V regulator output as input and gives output to the lamp

of the detection circuit. The voltage regulator is so set that its output can be adjusted from +5 V to +15 V. Adjustable source is needed because of the critical trigger levels of optic sense output. Lamp needs approximately 70 mA.

The related figures of the power supply unit are shown on the following page.

High Voltage Supply



Low Voltage & +5 V Supply

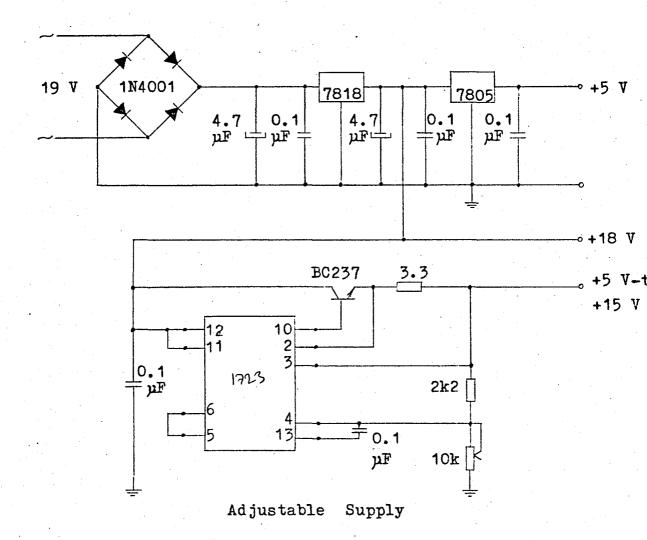


Figure 3.6

F. Optic Detector System

The optic detection is one of the most important feature of this thesis. Presently, there are many different kinds of optical sensors. In the developed system, the resolution of two consecutive points is 1.27 mm. This is not a very small distance for the sensor which is chosen for scanning procedure.

The optic sensor is not sensitive to the side lights due to its lens. In application, a small light source is used and the detector is centered on top of it, keeping a distance for the glass plate and the film.

For detection process, the operator places the dark solid dots on the transparent film. Then this film is scanned line by line. The sensor which is a transistor changes its state depending on the intensity of the light. The transistor is used in the common emitter configuration and the collector voltage is taken as output. Due to the mechanical movement and other disturbances, the best results can be achieved by using a comparator. For this purpose, LM 324 is used in the prototype. So the triggering level can be determined by adjusting the potentiometer i.e comparator inverting input voltage level is adjusted.

The comparator is essential in the circuitry in order to generate a +5 V signal for even a small input from the optical sensor. Direct coupling between the sensor and the microprocessor would not be appropriate because of the weak signal from the sensor, not being able to trigger the input port of the PIO of the Z-80 microprocessor.

Consequently, the output switches between high (+5V) and low (OV) levels. Those voltages are applied to the input port of the PIO of the Z-80 microprocessor card and this optical information is written to the memory, according to the scan program.

The detection circuitry and the detection mechanism are shown in figure 3.7 and figure 3.8 respectively.

Detection Circuitry

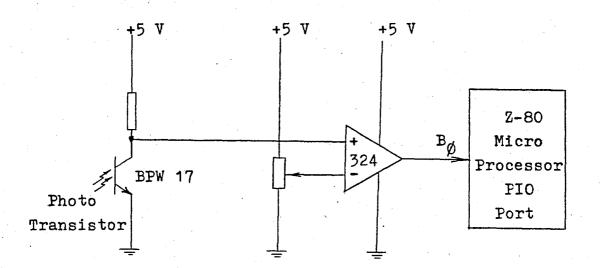


Figure 3.7

Detection Mechanism

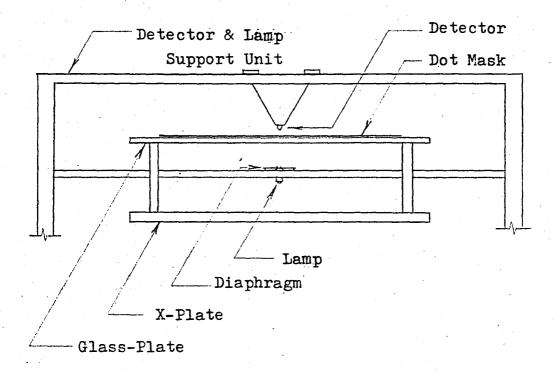


Figure 3.8

IV. SYSTEM SOFTWARE

The software of the system consists of mainly two sections and each program contains subprograms.

A. Detection Program

- 1. Line Detection Program
- 2. Frame-length Detection Program
- 3. Scanning and Storing Program

B. Drilling Program

C. Subprograms

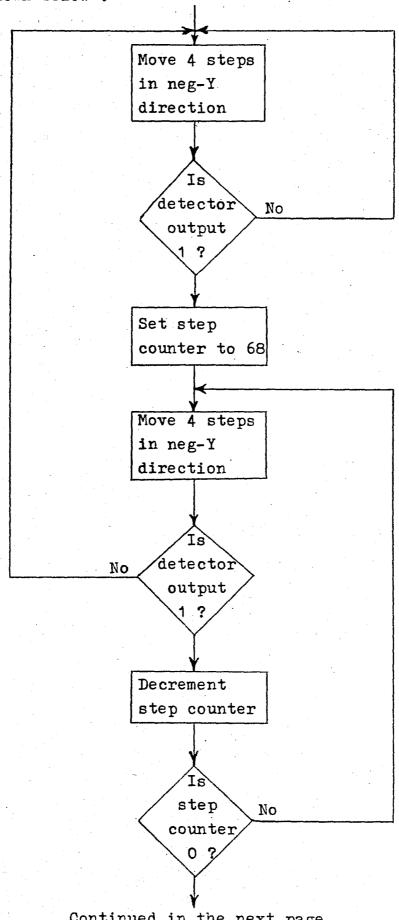
- 1. Reset Routine
- 2. Interrupt Service Routine
- 3. Acceleration and Deceleration Subroutines
- 4. Constant Speed Subroutines
- 5. Delay Subroutines

A. Detection Program

1. Line Detection Program

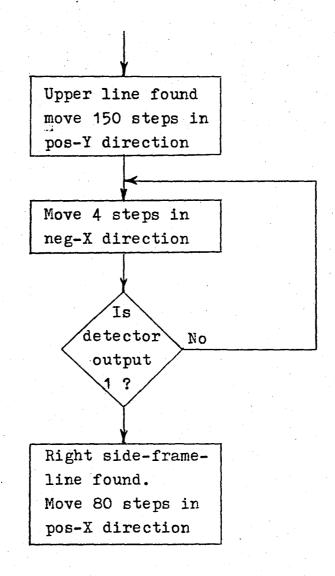
This routine searches the frame lines and locates the detector on the top right corner of the dot mask. Program

flow is shown below:

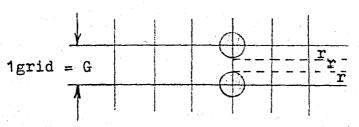


Continued in the next page

1 Grid=1/10 inc r:Radius of dot



The number of steps written in the flowchart are found according to the dimension of dots and grid length i.e dots have a radius of 27 steps where each step is equal to 0.015875 mm. and the length of a grid is 80 steps. Thus, two consecutive dots have a spacing distance of 26 steps as shown in Figure 4.1.

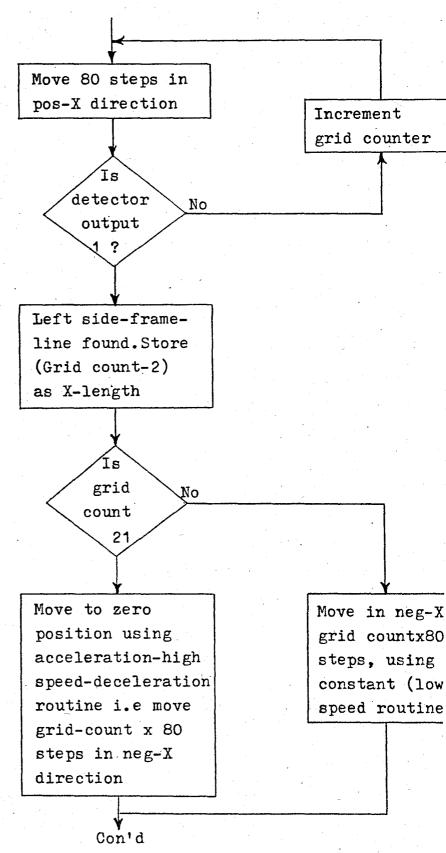


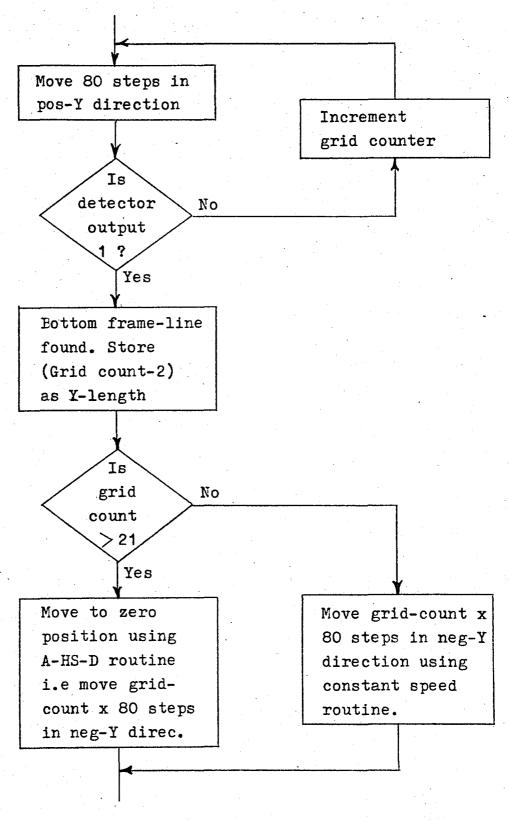
Dot dimensions

Figure 4.1

2. Frame Length Detection Program

This program measures the X and Y lengths of the frame of dot mask.





In this program the grid counter is compared with 21 since 11 grids are needed for acceleration and 10 for deceleration (1 grid = 80 steps).

In the flowchart A-HS-D is used to express the acceleration-high speed-deceleration routine in short.

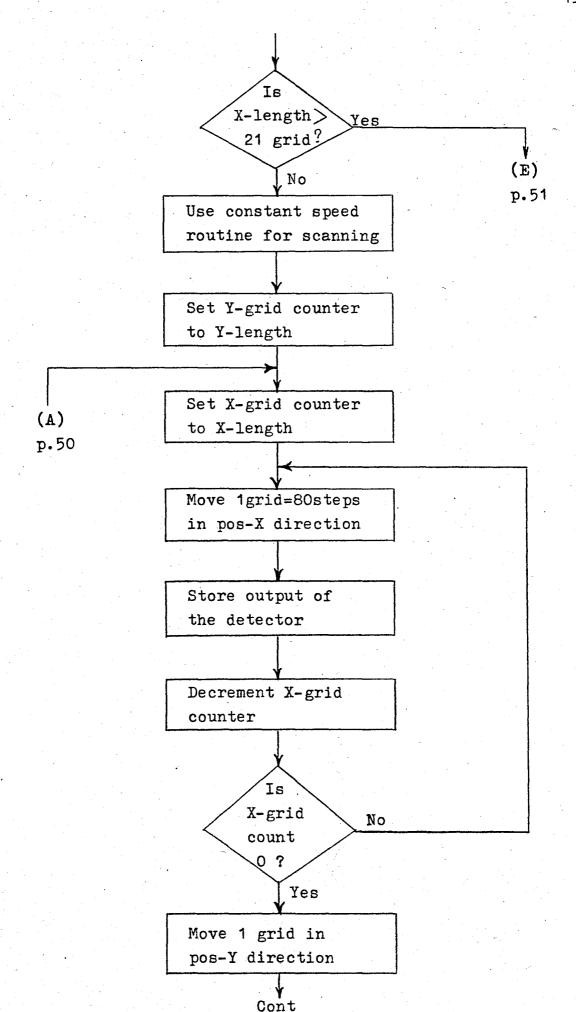
3. Scanning and Storing Program

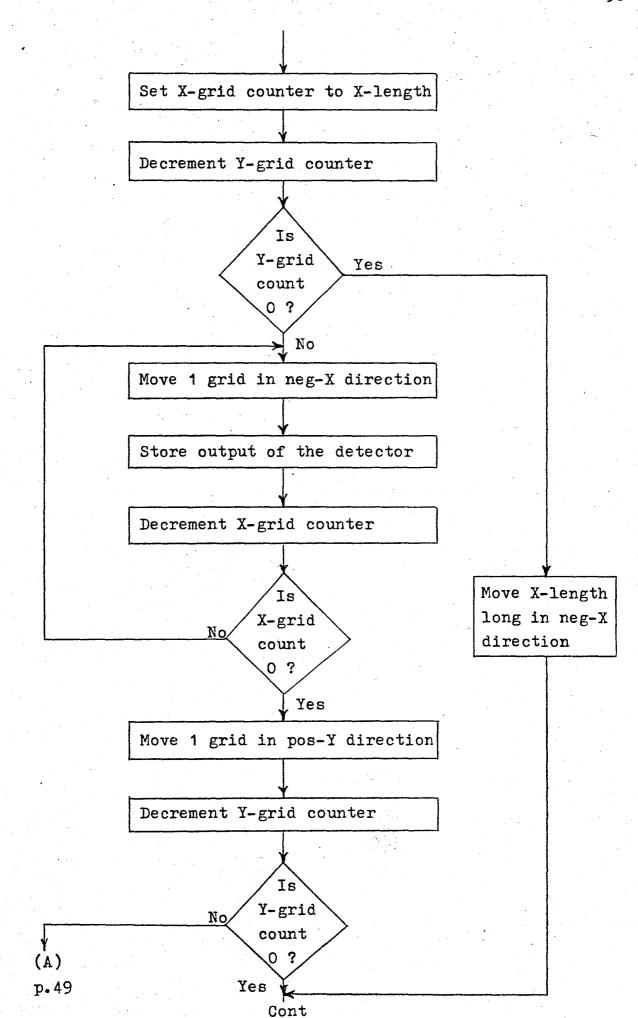
This program scans the dot mask whose dimensions are specified in the previous programs, in a meander pattern i.e odd numbered lines are scanned from right to left while even numbered lines are scanned in the opposite direction.

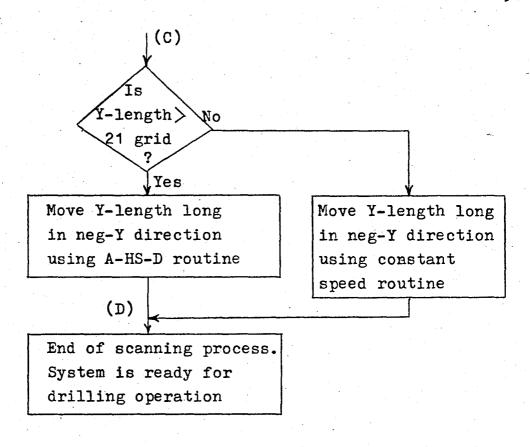
The store routine tests the output of the detector at every grid-node where spacing between two grids is 80 steps which is equal to 1/20 inch. Each test result (0 or 1) is stored in a temporary memory location and when 8 consecutive hole-position information is read (i.e one byte is filled) then this datum(byte) is stored in the memory starting from the address 8000 H.

The scan program can proceed with two different speeds. One of them is constant speed (246 steps/sec) scanning routine and the other is acceleration-high speed-deceleration routine. Those cases will be explained respectively.

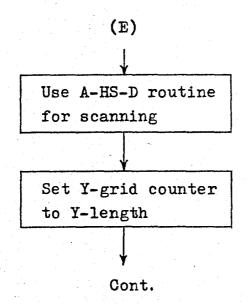
a. Constant Speed Scanning and Detection. This routine is selected if the X-length of the dot mask is equal or smaller than the distance required for acceleration, high speed and deceleration. This distance is equal to 21/20 inch. The flow-chart of this routine is in the following pages.

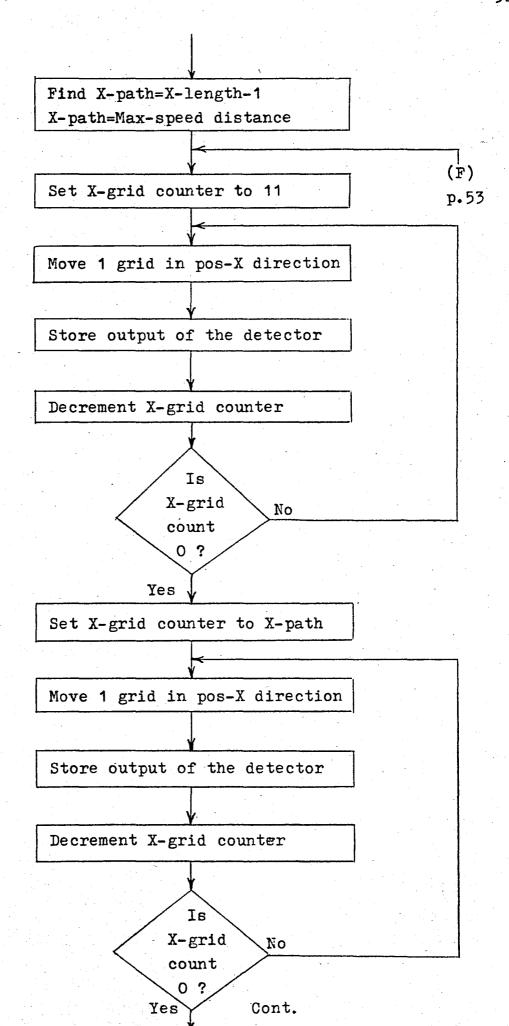


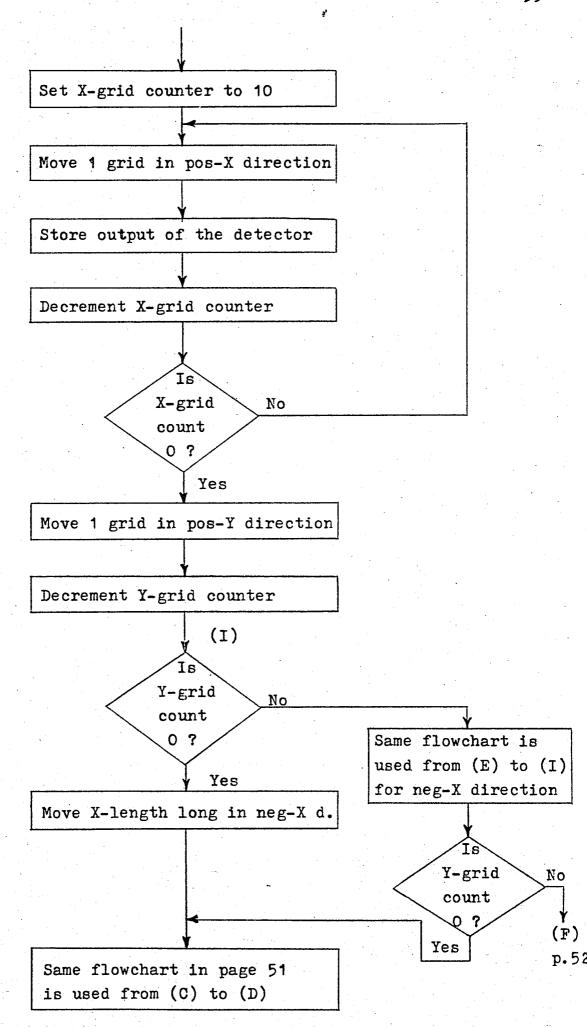




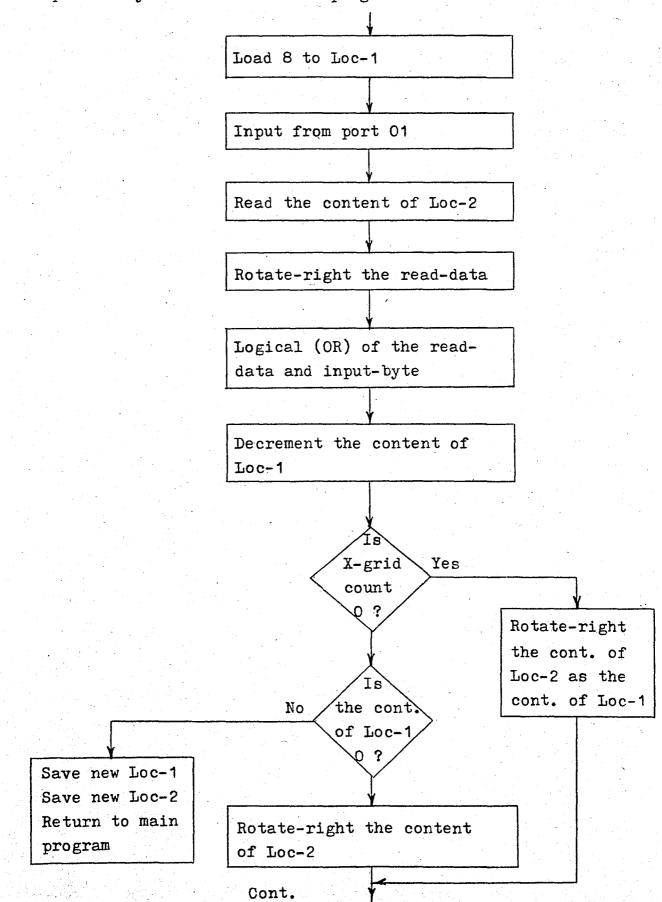
b. High Speed Scanning and Detection. When the X-length of the frame of dot mask, is greater than 21/20 inch, this routine is selected, so a better performance (i.e a shorter scanning time) is obtained due to acceleration—high speed (835 steps/sec)—deceleration profile instead of constant speed (246 steps/sec) scanning. Program flow is as follows:

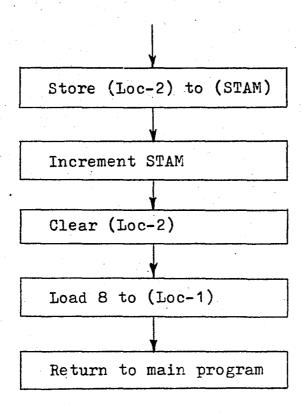






c. Store Program. By this program data which hold the drilling-hole-position information, are stored in the memory sequentially. Flowchart of the program is shown below:





Expressions used in the above flowchart are:

Loc-1: Holds the bit count. Initially Loc-1 contains 8 and decremented at each test of the output of detector (at each grid-node). Its content reaches zero when 8 data are taken i.e a byte of hole-position information is ready to be stored.

<u>Loc-2</u>: Keeps the data till a byte of information is formed. Then that byte is stored in the memory.

STAM: Means starting address of memory. The data (byte) in Loc-2 is stored to the memory location that STAM shows. In the beginning STAM contains 8000 H which is the first RAM location in the memory unit. STAM is incremented after each byte-store.

B. Drilling Program

This program reads the hole-position data from the memory and drives the X-Y stage scanner to perform the drilling process. Path optimization algorithm is used to minimize the drilling procedure time.

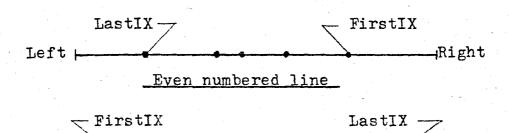
In the program, hole-position data is read from the memory as one byte at a time and every byte is tested bit by bit. A position counter (register) is set to X-length value and it is decremented at each bit test. If the tested bit contains'1' i.e that is a hole information then the value of position counter is stored in the memory starting from the address FirstIX=8730H. Zeroes which are encountered during bit test are not taken into consideration. When position counter reaches zero then it means that, line is finished and drilling of the holes on that line can be performed.

The flowchart in the following page is written for the odd numbered lines. In the even numbered lines holepositions are listed (stored) from left to right. This can be simply shown as follows:

Odd numbered line

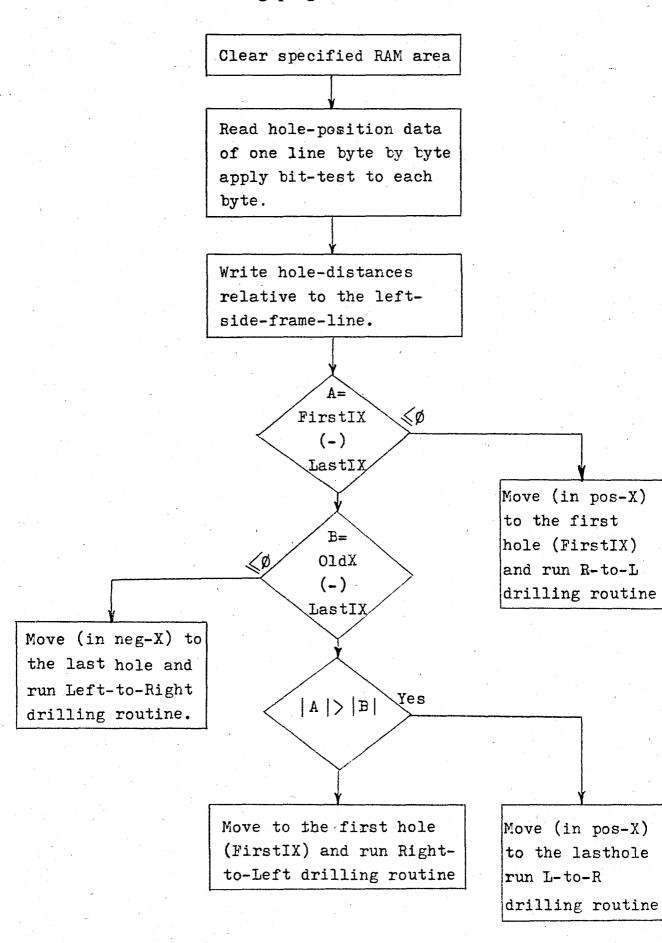
FirstIX (The first hole location)
LastIX (The last hole location)

Left



Right

Flowchart of the drilling program for the odd numbered lines:



In the drilling program, OldX contains the last location of the X-motor. Locations of the holes are specified according to the distance from the left-frame-line i.e holeposition numbers increase from left to right.

After the execution of one line, the next line data are tested. If there is no data in any line then stage moves one grid (80 steps) in the positive-Y direction.

The movement of the stage from one hole position to another is performed due to calculation of relative distance between two subsequent hole-positions. If the distance between two hole-positions is greater than 21 grids then acceleration-maximum speed-deceleration routine is run otherwise the X-Y stage scanner moves with constant speed.

At the end of drilling program, return routine takes place and moves the X-Y table to its original zero position for another drilling operation.

C. Subprograms

1. Reset Routine

This subroutine :

- a. Sets the stack pointer to 87E5 H
- b. Chooses interrupt mode 2
- c. Loads (I) interrupt page address register with Ø7
- d. Programs A-port of PIO as output port and,

B-port of PIO as input port

Reset Routine

ØØØØ	31 E5 87	LD SP,87E5 H
øøø3	ED 5E	IM 2
ØØØ5	3E Ø7	LD A, Ø7
ØØØ7	ED 47	LD I, A
øøø 9	3E ØF	LD A, ØF H
øøøв	D3 Ø2	OUT (Ø2), A
ØØØD	3E 4F	LD A, 4F H
øøøf	D3 Ø3	OUT (Ø3), A
ØØ11	AF	XOR A
ØØ12	D3 ØØ	OUT (ØØ), A
ØØ14	FB	EI
ØØ15	76	HALT

Table 4.1

2. Interrupt Service Routine

Control of the X-Y stage scanner is provided by this routine. Start switch starts the scanning and then the drilling programs. The other four switches (pos-X, neg-X, pos-Y, neg-Y) are used to move the X-Y table in both X and Y directions. Stop switch is used to break the above mentioned programs when they are running.

This routine utilizes the interrupt feature of Z-80 microprocessor. The Z-80 CPU is so operated that an indirect call to any menory location can be achieved in response to an interrupt. For this purpose the I register is loaded with $\emptyset 7$ which is the high order 8-bits of the indirect address. The

lower 8-bits of the address are provided by the interrupting switch.

Interrupt Service Routine Starting Addresses

Start Switch Ø7BE : 1F Ø7BF : ØØ Ø7DE : 25 Stop Switch Ø7DF : Ø7 Pos-X Switch Ø7FC : ØØ Ø7FD : Ø7 Ø7FA : 4Ø Neg-X Switch Ø7FB : Ø7 Pos-Y Switch Ø7F6 : 65 Ø7F7 : Ø7 Neg-Y Switch Ø7EE : DØ Ø7EF : Ø6

Table 4.2

3. Acceleration and Deceleration Subroutines

In the second section, driving conditions are examined for stepper motors. The necessary pulse sequences are supplied from the microprocessor card and the look-up table for bit patterns (shown in stable 4.3) is created in the memory. Since stepper motors cannot start at high speeds, they are driven at low speed in the beginning and speed is increased step by step, changing the delays between pulse-patterns. For the above mentioned reasons, a specific distance is needed to accelerate and decelerate, which is 11 grids for acceleration and 10 grids for deceleration (1Grid=80steps). In the prototype, by changing delay constants, speed is changed from 238 steps/sec to 791 steps/sec in 11 stages.

Stepper Look-up Table

Memory Address	Bit Pattern	
Ø7AØ Н	ØA H	
Ø7A1 H	Ø9 Н	X-MOTOR
Ø7A2 H	Ø5 H	
Ø7A3 H	Ø6 H	
Ø7ВØ Н	AØ H	
Ø7B1 H	9Ø H	Y-MOTOR
Ø7B2 H	5Ø Н	
Ø7В3 Н	6Ø H	

Table 4.3

These bit patterns (shown in Table 4.3) are sent to drivers through PIO unit. For clockwise rotation, bit patterns are in the form of A, 9, 5, 6 and opposite order for the counterclockwise rotation.

4. Constant Speed Subroutines

These routines are used almost in all programs. They provide constant delay between pulse patterns to be sent to stepper motor drivers. Motors obtain a speed of 246 steps/sec by these routines, and a register of the processor is used as the step counter. At every 80 step routine repeates itself.

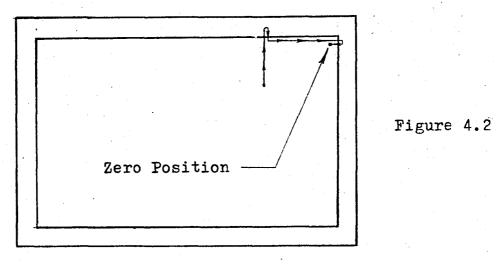
5. Delay Subroutines

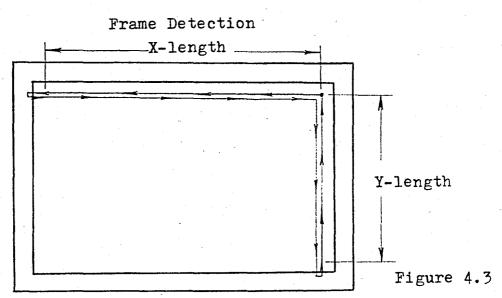
In all programs those routines are used either in constant form or in variable form.

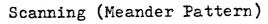
For the stepper motor's pulse sequence, a delay of 8017 T-cycles long, is used between two consecutive pulses. Where, every T-cycle takes 0.5 microsecond due to 2 MHz clock frequency.

For the variable delay, a constant, in the delay routine, is changed. This kind of delay is used in the acceleration-maximum speed-deceleration routine to provide different speeds.

Line Detection







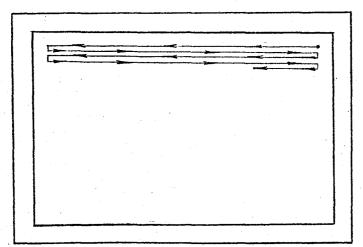


Figure 4.4

V . CONCLUSION

Presently the automation has led to the improvement in production processes, thereby needing minimum manpower. The advantages are, that the whole process once set up, can be executed repeatedly at higher speeds than is possible with an operator, mechanically doing the settings.

During the realization of the prototype, some problems were encountered but all of them were eliminated, for instance, for the mechanical assembly the most important thing was the backlash of the system, which was eliminated by a great deal of precision on the part of the mechanic. Also, in the same case certain methods to prevent backlash (e.g spring system, adjustable nut) could be utilized. Keeping in mind that it was better if the bearings at each end of the lead-screws were of the type that can move in their housing freely, bearing of such a nature could have been used. In addition to these, the alignment of the mechanical assembly had to have some adjustment points to provide smooth movement. In the developed system this was solved by the expertise of the mechanic.

The other important thing was the selection of stepper motors. Since, prior to this selection it was not known
how much torque, a mechanical assembly would need, the steppers
were chosen from powerful series which generally have low
speed, high torque characteristics. This aspect resulted in
success by means of the designed drive circuitry.

The designed system shows an effective use of microprocessors in the industrial field. The objective was to realize a system that needs minimum interaction of the user and to give accurate results. The system performance provides the above mentioned properties. The user can design his/her circuits freely and also due to system resolution, it can fit the mask pattern. The scan time, though, could be reduced considerably if motors of high speed (motors with a speed of upto 4000 steps/sec, rather than the ones used with a speed of 835 steps/sec) more suitable, were selected. The scanning process for a Eurocard takes about 17 minutes, which is considerably short a time due to the right and efficient usage of the software. By using the optimum path concept, this reduction in time is achieved.

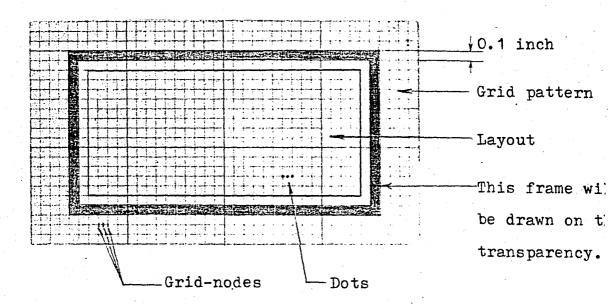
The system can work as a drilling machine with some mechanical modifications such as the detector, the lamp and the glass plate can be replaced by a drill set to perform the drilling operation.

APPENDICES

APPENDIX A

OPERATING INSTRUCTIONS

- 1. How to Prepare The Dot Mask
- i. After the printed circuit layout is drawn, it is placed on a paper which has 0.1 inch divisions (as shown below fig.). On these two, the clean transparency is located.



ii. The frame lines of the dot mask are drawn such that every side of the mask frame is 0.1 inch greater than the frame of the layout. Frame-line thickness of 0.1 inch is considered to be enough and it is advisable to use a drawing-pen with black ink (e.g Rapido 0.5 mm).

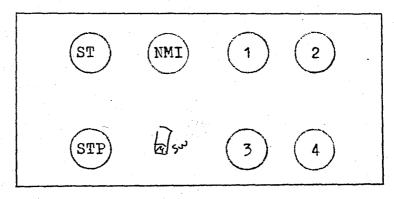
iii. Hole positions are marked on the transparency by locating them at the nodes of the grid pattern. One more hole can be marked between each node of the grid pattern shown in the previous page, because the scanning resolution of the system is 1/20 inch.

If there are any hole positions on the layout which do not coincide with the nodes of the grid pattern, they should be placed on to the closest node.

After the dot-mask is prepared, it is correctly placed onto the glass plate, matching the upper right corner of the dot-mask frame to the right-angled marker on the glass.

2. Running The System

i. System is switched on. Power on-reset runs the reset program and Halt LED is turned on at the end of this program. Then using the manuel control switches, the detector is placed somewhere in the dot-mask frame (i.e X-Y table is positioned in such a way that Detector points somewhere in the dot-mask frame).



Control Panel

The functions of the buttons are as follows:

Button ST : START

Button STP: STOP

Button NMI : Emergency stop

Button 1 : X-Motor control (stage moves in neg-X direction)

Button 2 : X-Motor control (stage moves in pos-X direction)

Button 3 : Y-Motor control (stage moves in pos-Y direction)

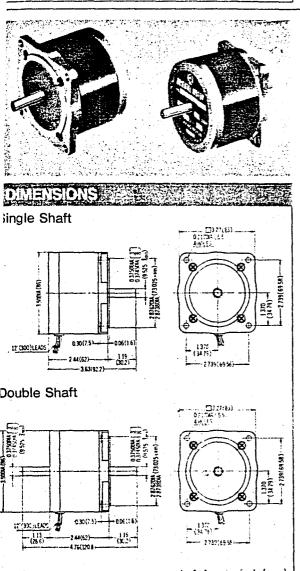
Button 4 : Y-Motor control (stage moves in neg-Y direction)

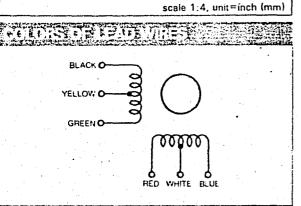
- ii. Pressing the ST (Start) button starts the scanning and detection program and at the end, stage takes its original zero position (at the upper right corner) and HALT LED turns on.
- iii. Now ST button commences the drilling program. At each drilling-hole-position, stage stops, a LED flashes for a few seconds to simulate the drilling operation.
- iv. After completing the drilling process of all holes, stage moves to zero-position and stops. Drilling process can be repeated as desired by pressing the ST button.
- v. For a new dot-mask scanning process, RST (Reset) must be given to the system, then same order (from ii to iv) is followed.

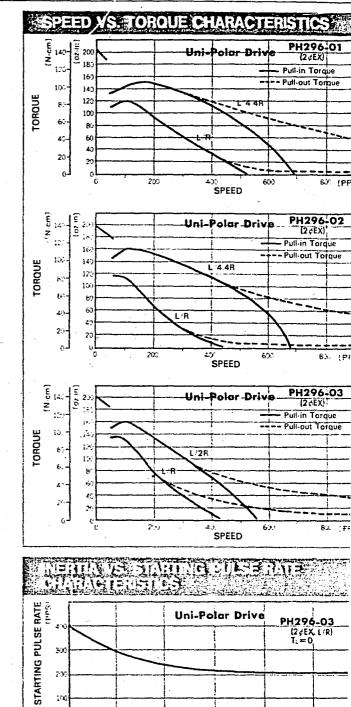
In case of emergency, NMI button should be pressed.

HYBRID T

PH296-







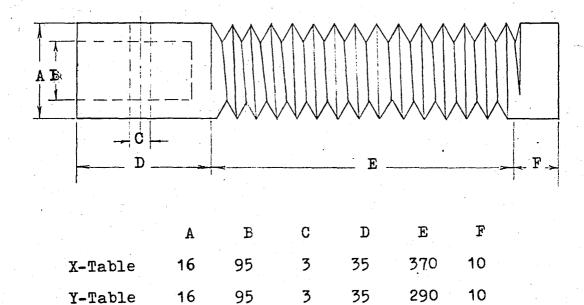
INERTIA

PECIFICATIONS (2-phase full-step)

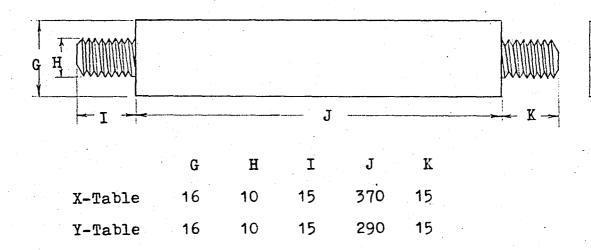
Motor type		Voltage	Current per phase	Holding Torque		Resistance per phase	Induct per pl
Single Shaft	Double Shaft	" V	A/phase	oz-in	N-cm	ohm/phase	mH/p
PH296-01	PH296-01B	1.8	4.5	174	123	0.4	1.4
PH296-02	PH296-02B	5.5	1.25	174	123	4.4	14
PH296-03	PH296-03B	14	0.7	174	123	20	60
Rotor inertia 3 1 nz.	int (ESOn.cm?) • We	inht 3 3lbs (1 F	i ka)				

APPENDIX C

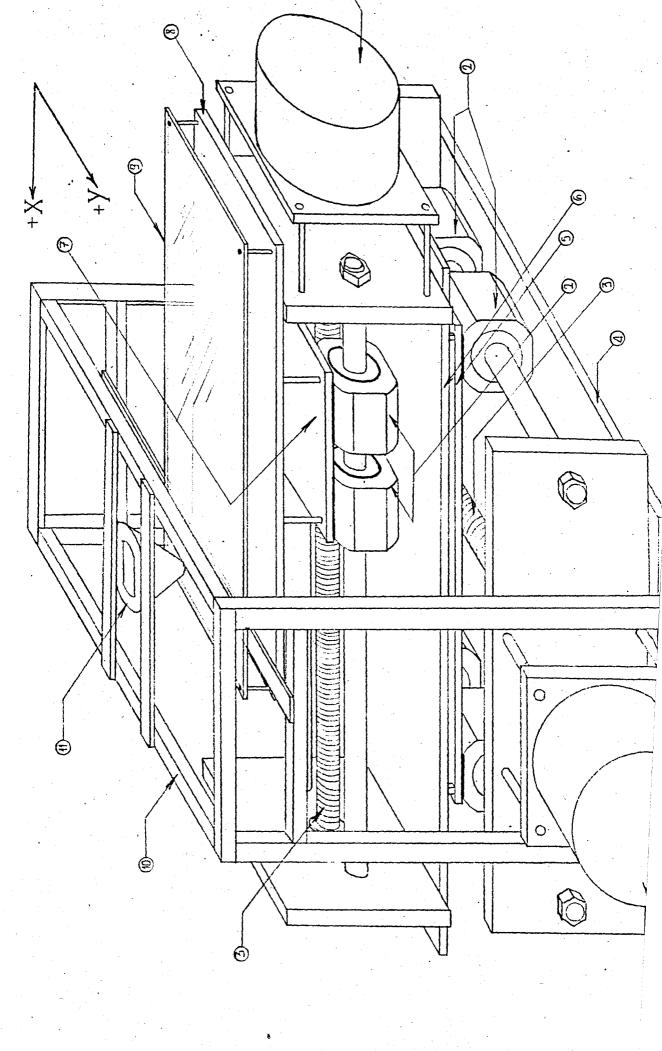
LEAD-SCREW



Cylindrical Shaft



- i. Drawings are not to scale.
- ii. All dimensions are in millimeters.

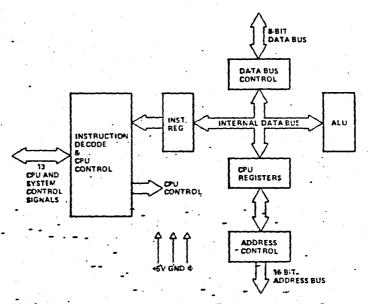


Part List of X-Y Stage Scanner

- 1. Stepper motors
- 2. Linear motion bearings
- 3. Lead-screws
- 4. Base plate
- 5. Intermediate Y-plate
- 6. Y-plate
- 7. Intermediate X-plate
- 8. X-plate
- 9. Glass plate
- 10. Support for lamp and photo-detector
- 11. Photo-detector system

Z-80 CPU ARCHITECTURE

A block diagram of the internal architecture of the Z-80 CPU is shown in figure 2.0-1. The diagram shows all of the major elements in the CPU and it should be referred to throughout the following description.



Z-80 CPU BLOCK DIAGRAM -FIGURE 2.0-1 -

CPU REGISTERS

The Z-80 CPU contains 208 bits of R/W memory that are accessible to the programmer. Figure 2.0.2 illustrates how this memory is configured into eighteen 8-bit registers and four 16-bit registers. All Z-80 registers are implemented using static RAM. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or in pairs as 16-bit registers. There are also two sets of accumulator and flag registers.

Special Purpose Registers

- 1. Program Counter (PC). The program counter holds the 16-bit address of the current instruction being fetched from memory. The PC is automatically incremented after its contents have been transferred to the address lines. When a program jump occurs the new value is automatically placed in the PC, overriding the incrementer.
- 2. Stack Pointer (SP). The stack pointer holds the 16-bit address of the current top of a stack located anywhere in external system RAM memory. The external stack memory is organized as a last-in first-out (LIFO) file. Data can be pushed onto the stack from specific CPU registers or popped off of the stack into specific CPU registers through the execution of PUSH and POP instructions. The data popped from the stack is always the last data pushed onto it. The stack allows simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data manipulation.

MAIN R	EG SET	ALTERNAT		
ACCUMULATOR A	FLAGS	ACCUMULATOR A	FLAGS	Ì
8	С	В.	Ċ	1)
D	E	D.	£'	GENERAL PURPOSE REGISTERS
н	, L	H.	L.	
	INTERRUPT VECTOR I	WEMCRY REFRESH R		· · ·
	INDEX REGIST		PURPOSE REGISTERS	•

Z-80 CPU REGISTER CONFIGURATION FIGURE 2.0-2

PROGRAM COUNTER PC

- 3. Two Index Registers (IX & IY). The two independent index registers hold a 16-bit base address that is used in indexed addressing modes. In this mode, an index register is used as a base to point to a region in memory from which data is to be stored or retrieved. An additional byte is included in indexed instructions to specify a displacement from this base. This displacement is specified as a two's complement signed integer. This mode of addressing greatly simplifies many types of programs, especially where tables of data are used.
- 4. Interrupt Page Address Register (1). The Z-80 CPU can be operated in a mode where an indirect call to any memory location can be achieved in response to an interrupt. The I Register is used for this purpose to store the high order 8-bits of the indirect address while the interrupting device provides the lower 8-bits of the address. This feature allows interrupt routines to be dynamically located anywhere in memory with absolute minimal access time to the routine.
- 5. Memory Refresh Register (R). The Z-80 CPU contains a memory refresh counter to enable dynamic memories to be used with the same ease as static memories. Seven bits of this 8 bit register are automatically incremented after each instruction fetch. The eighth bit will remain as programmed as the result of an LD R, A instruction. The data in the refresh counter is sent out on the lower portion of the address bus along with a refresh control signal while the CPU is decoding and executing the fetched instruction. This mode of refresh is totally transparent to the programmer and does not slow down the CPU operation. The programmer can load the R register for testing purposes, but this register is normally not used by the programmer. During refresh, the contents of the 1 register are placed on the upper 8 bits of the address bus.

Accumulator and Flag Registers

The CPU includes two independent 8-bit accumulators and associated 8-bit flag registers. The accumulator holds the results of 8-bit arithmetic or logical operations while the flag register indicates specific conditions for 8 or 16-bit operations, such as indicating whether or not the result of an operation is equal to zero. The programmer selects the accumulator and flag pair that he wishes to work with with a single exchange instruction so that he may easily work with either pair.

General Purpose Registers

There are two matched sets of general purpose registers, each set containing six 8-bit registers that may be used individually as 8-bit registers or as 16-bit register; pairs by the programmer. One set is called BC, DE and HL while the complementary set is called BC, DE and HL. At any one time the programmer can select either set of registers to work with through a single exchange command for the entire set. In systems where fast interrupt response is required, one set of general purpose registers and an accumulator/flag register may be reserved for handling this very fast routine. Only a simple exchange commands need be executed to go between the routines. This greatly reduces interrupt service time by eliminating the requirement for saving and retrieving register contents in the external stack during interrupt or subroutine processing. These general purpose registers are used for a wide range of applications by the programmer. They also simplify programming, especially in ROM based systems where hitle external read write memory is available.

ARITHMETIC & LOGIC UNIT (ALU)

The 8-bit arithmetic and logical instructions of the CPU are executed in the ALU. Internally the ALU communicates with the registers and the external data bus on the internal data bus. The type of functions performed by the ALU include:

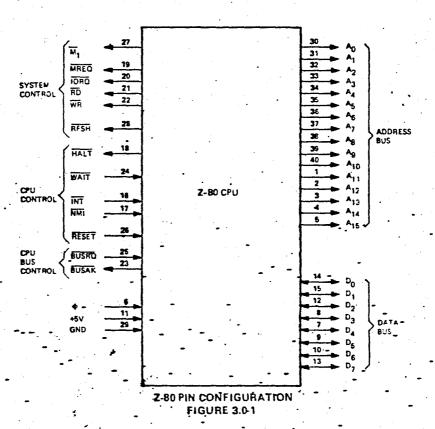
A dd	Left or right shifts or rotates (arithmetic and logical)
Subtract -	Tiggrement -
Logical AND	Decrement
Logical OR	Set bit
Logical Exclusive OR	Reset. bit
· Compare -	Test bit
·	

INSTRUCTION REGISTER AND CPU CONTROL

As each instruction is fetched from memory it is placed in the instruction register and decoded. The control sections performs this function and then generates and supplies all of the control signals necessary to read or write data from of to the registers, control the ALU and provide all required external control signals.

Z-80 CPU PIN DESCRIPTION

The Z-80 CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in figure 3.0-1 and the function of each is described below.



A₀-A₁₅
(Address Bus)

Tri-state output, active high. A₀-A₁₅ constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for 1'O device data exchanges, 1/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A₀ is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

D₀-D₇
(Data Bus)

Tri-state input/output, active high, D_0 - D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

M₁
(Machine Cycle one)

Output, active low \overline{M}_1 indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes \overline{M}_1 is generated as each op code byte is fetched. These two byte op-codes always begin with CBH DDH, EDH or FDH. \overline{M}_1 also occurs with $\overline{10RQ}$ to indicate an interrupt acknowledge cycle.

MREQ (Memory Request)

Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

APPENDIX E

INTRODUCTION

The Z-80 Parallel I/O (PIO) Circuit is a programmable, two port device which provides a TTL compatible interface between peripheral devices and the Z80-CPU. The CPU can configure the Z80-PIO to interface with a wide range of peripheral devices with no other external logic required. Typical peripheral devices that are fully compatible with the Z80-PIO include most keyboards, paper tape readers and punches, printers, PROM programmers, etc. The Z80-PIO utilizes N channel silicon gate depletion load technology and is packaged in a 40 pin DIP. Major features of the Z80-PIO include:

- Two independent 8 bit bidirectional peripheral interface ports with 'handshake' data transfer control
- Interrupt driven 'handstake' for fast response
- Any one of four distinct modes of operation may be selected for a port including:

Byte output

Byte input

Byte bidirectional bus (Available on Port A only)

Bit control mode

All with interrupt controlled handshake

- Daisy chain priority interrupt logic included to provide for automatic interrupt vectoring without external logic
- Eight outputs are capable of driving Darlington transistors
- All inputs and outputs fully TTL compatible
- Single 5 volt supply and ungle phase clock are required.

One of the unique freatures of the Z80-PIO that-separates it from other interface controllers is that all data transfer between the peripheral device and the CPU is accomplished under total interrupt control. The interrupt logic of the PIO permits fall usage of the efficient interrupt capabilities of the Z80-CPU during I/O transfers. All logic necessary to implement a fully nested interrupt structure is included in the PIO so that additional circuits are not required. Another unique feature of the PIO is that it can be programmed to interrupt the CPU on-the occurrence of specified status conditions in the peripheral device. For example, the PIO can be programmed to interrupt if any specified peripheral alarm conditions should occur. This interrupt capability reduces the amount of time that the processor must spend in polling peripheral status.

PIO ARCHITECTURE

A block diagram of the Z80-PIO is shown in Figure 2.0-1. The internal structure of the Z80-PIO consists of a Z80-CPU bus interface, internal control logic, Port A I/O logic, Port B I/O logic, and interrupt control logic. The CPU bus interface logic allows the PIO to interface directly to the Z80-CPU with no other external logic. However, address decoders and or line buffers may be required for large systems. The internal control logic synchronizes the CPU data bus to the peripheral device interfaces (Port A and Port B). The two I/O ports (A and B) are virtually identical and are used to interface directly to peripheral devices.

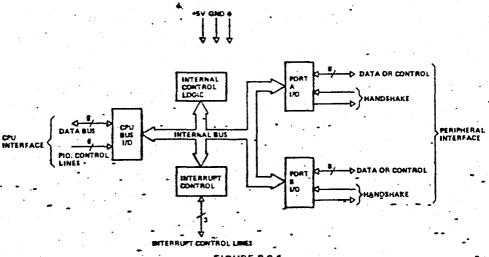


FIGURE 2.0-1
PIO BLOCK DIAGRAM

The Port I/O logic is composed of 6 registers with "handshake" control logic as shown in Figure 2.0-2. The registers include an 8-bit data input register, an 8-bit data output-register, a 2-bit mode control register, an 8-bit mask register, an 8-bit input output select register, and a 2-bit mask control register.

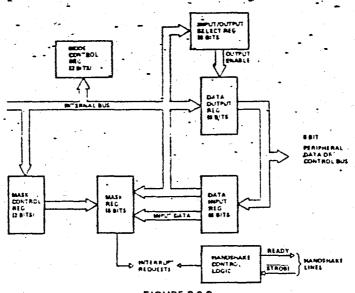


FIGURE 2.0.2 PORT I/O BLOCK DIAGRAM

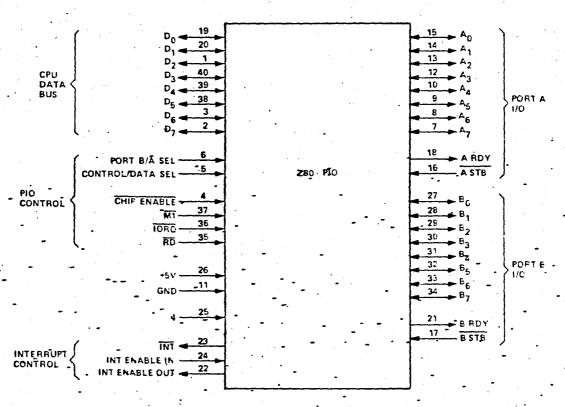
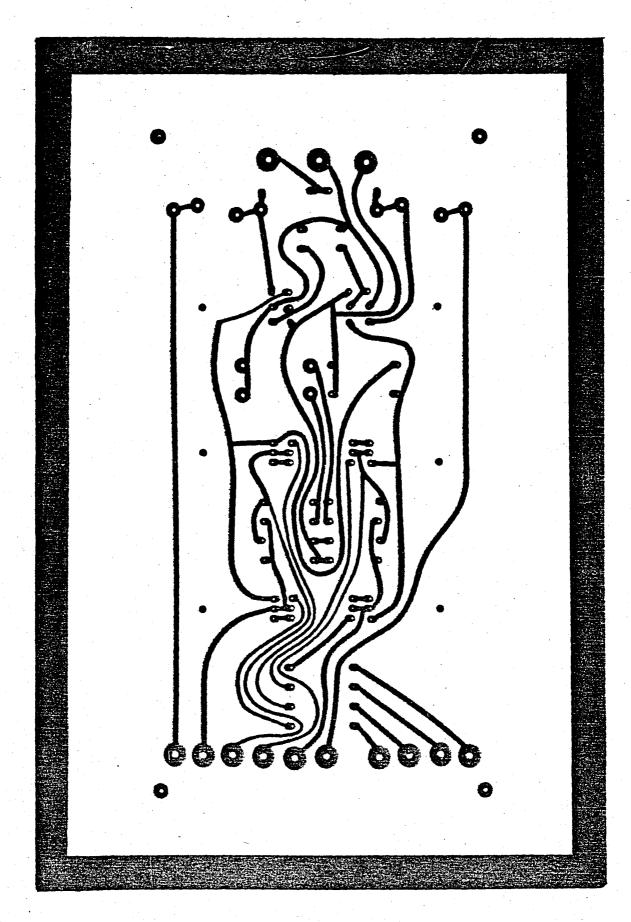
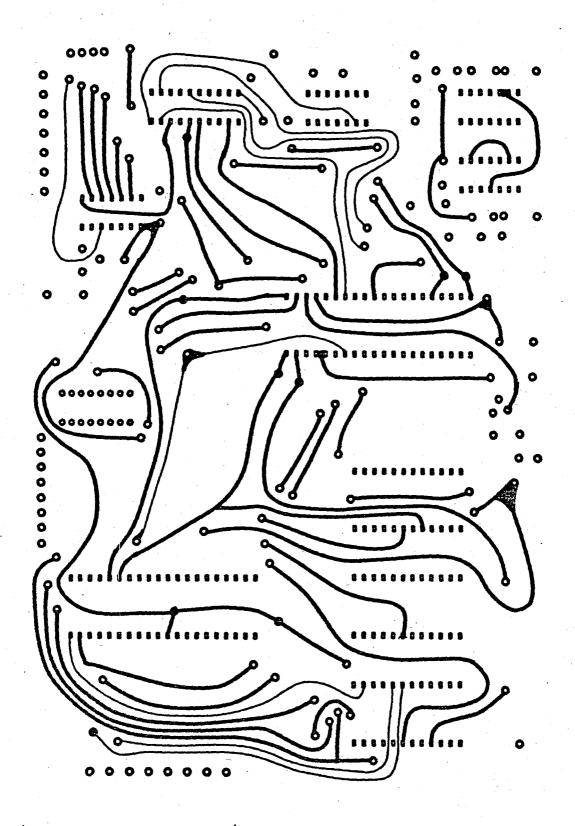


FIGURE 3.0.1
PIO PIN CONFIGURATION

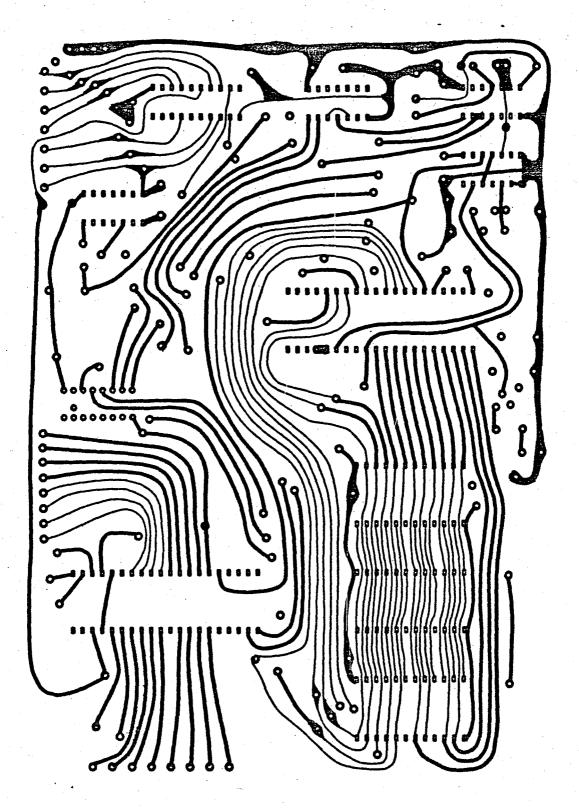


Stepper Motor Drive Card



(Component side)

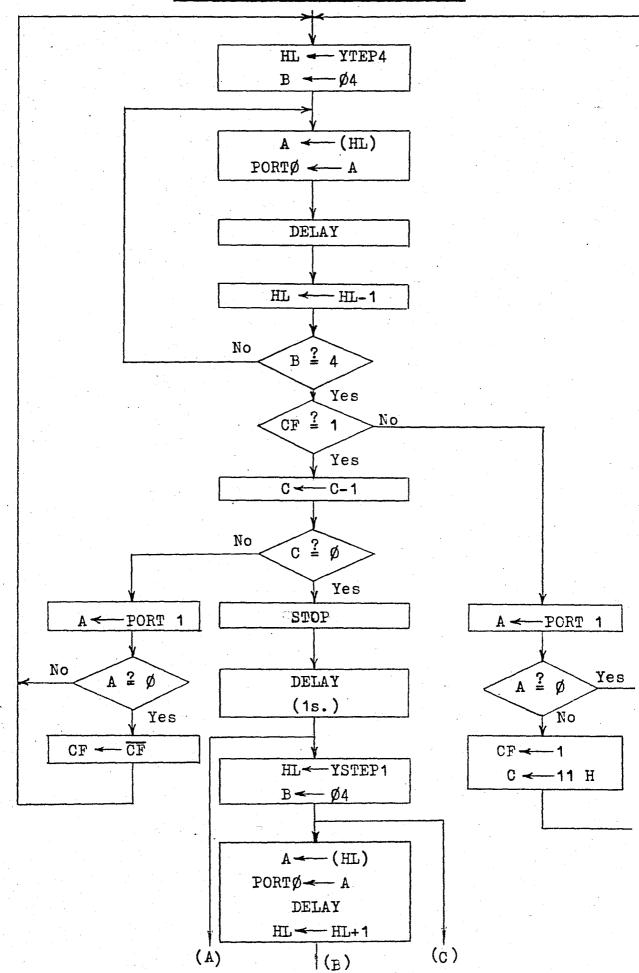
Z-80 Microprocessor Card

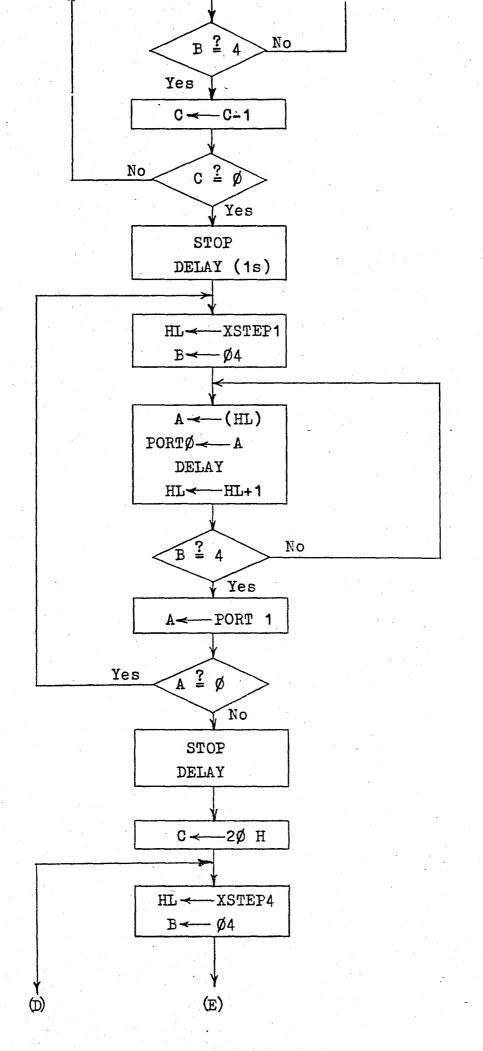


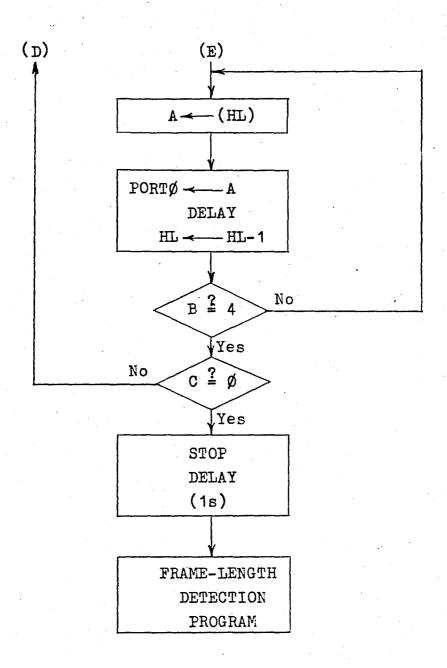
(Solder side)
Z-80 Microprocessor Card

7-80 MICRO PROCESSOR CARD

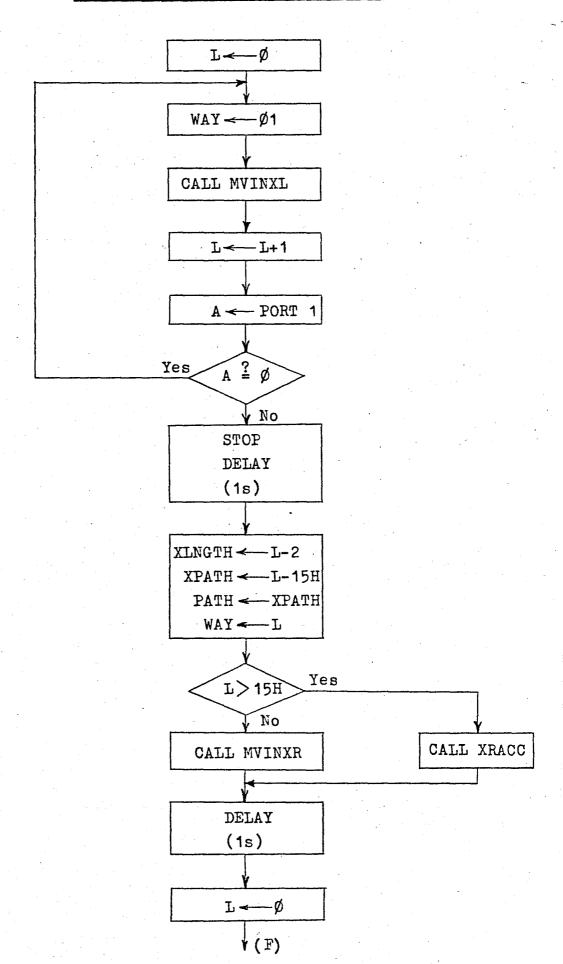
Frame Line Detection Program

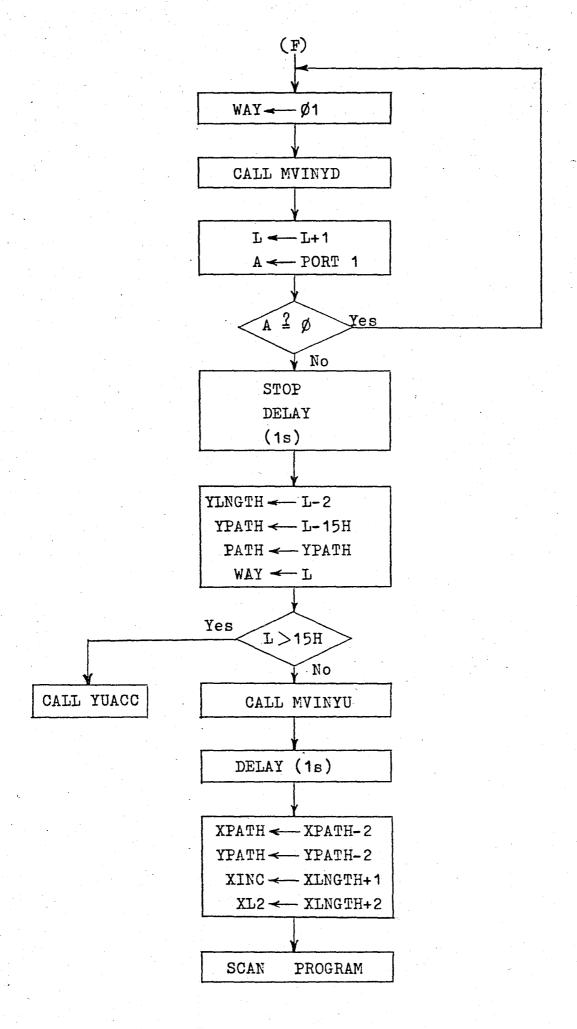


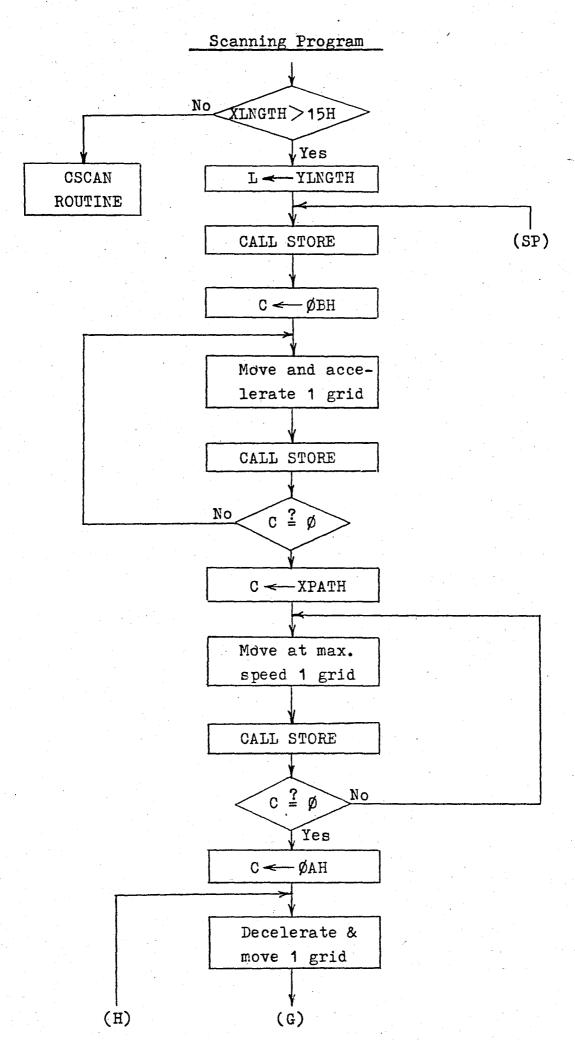


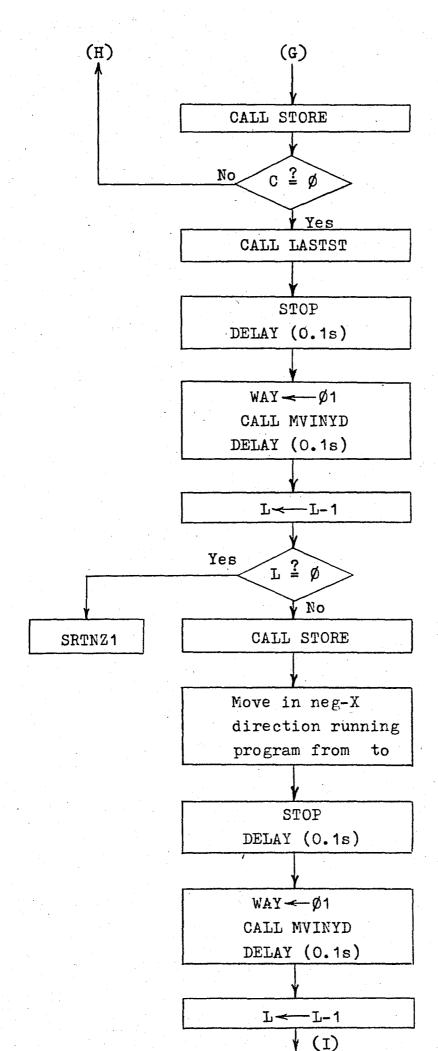


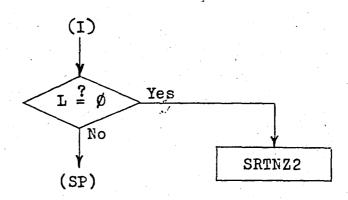
Frame-length Detection Program



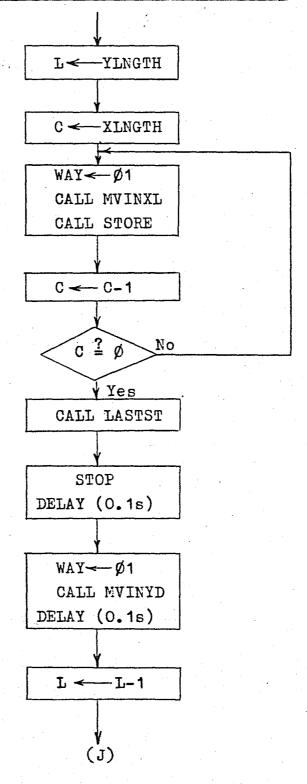


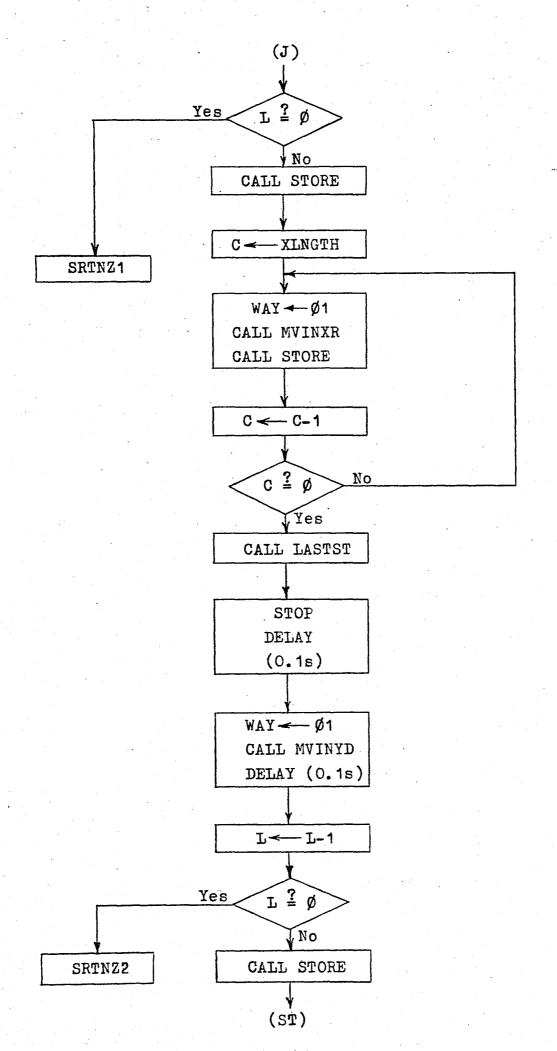




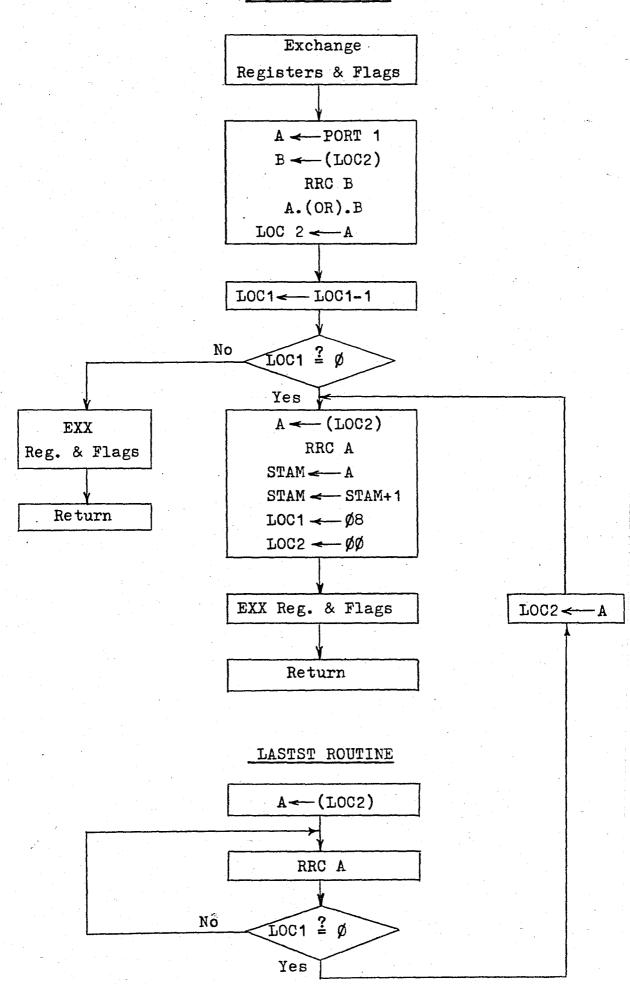


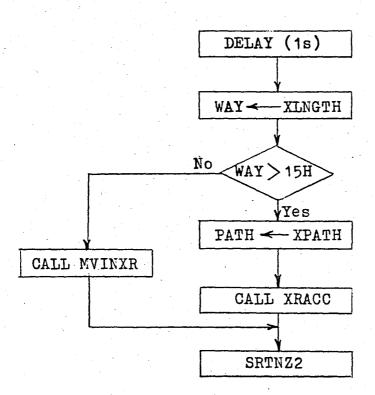
Constant speed scanning (CSCAN) Routine

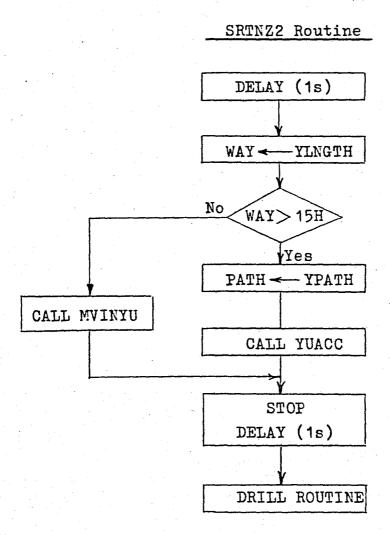




Store Routine

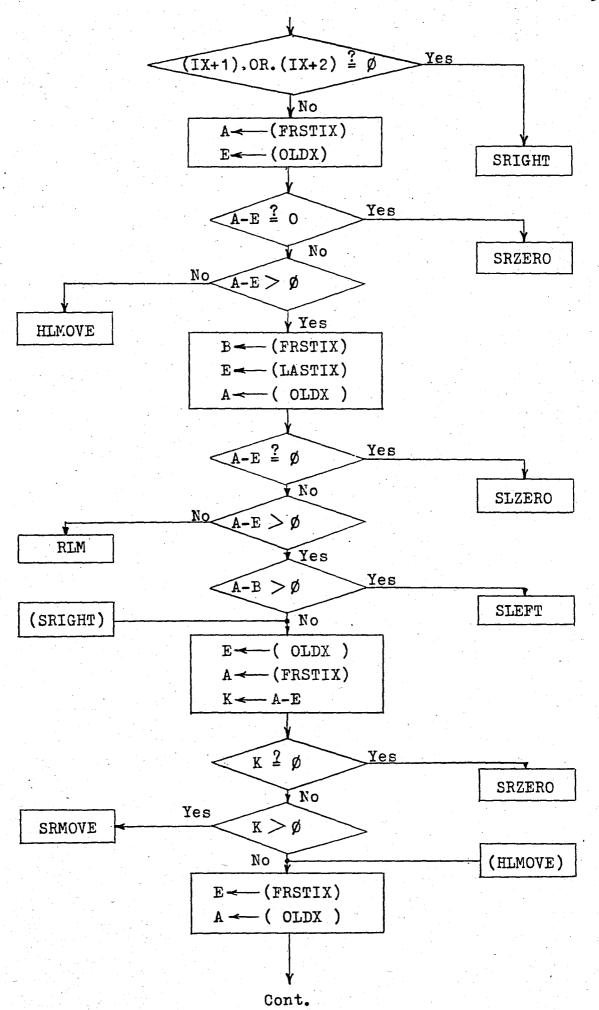


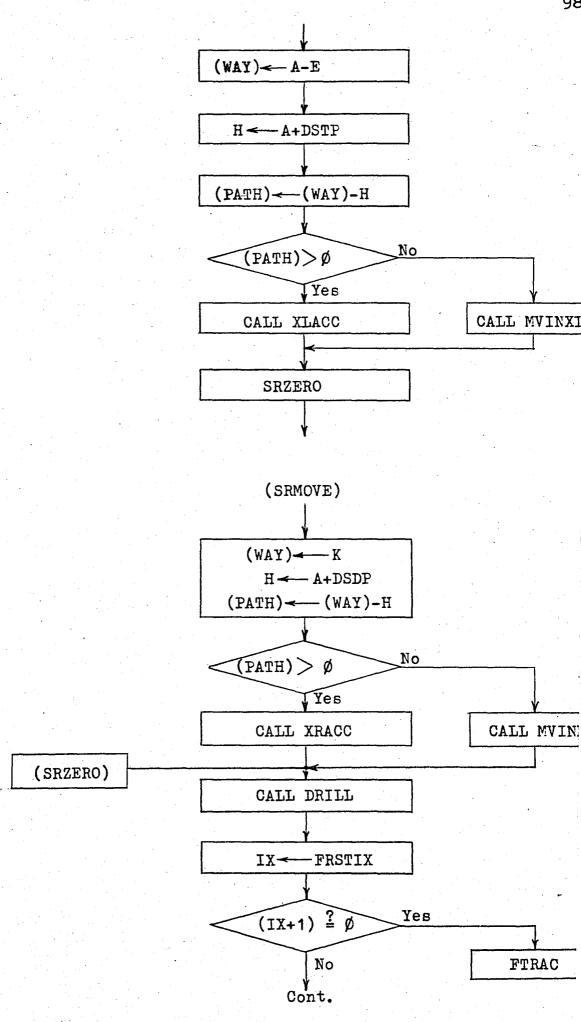


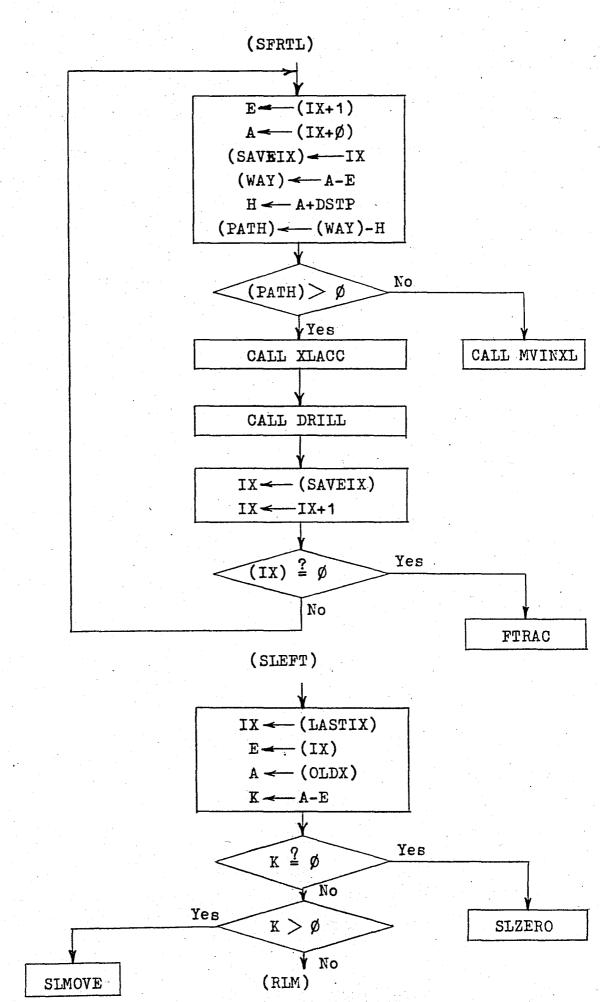


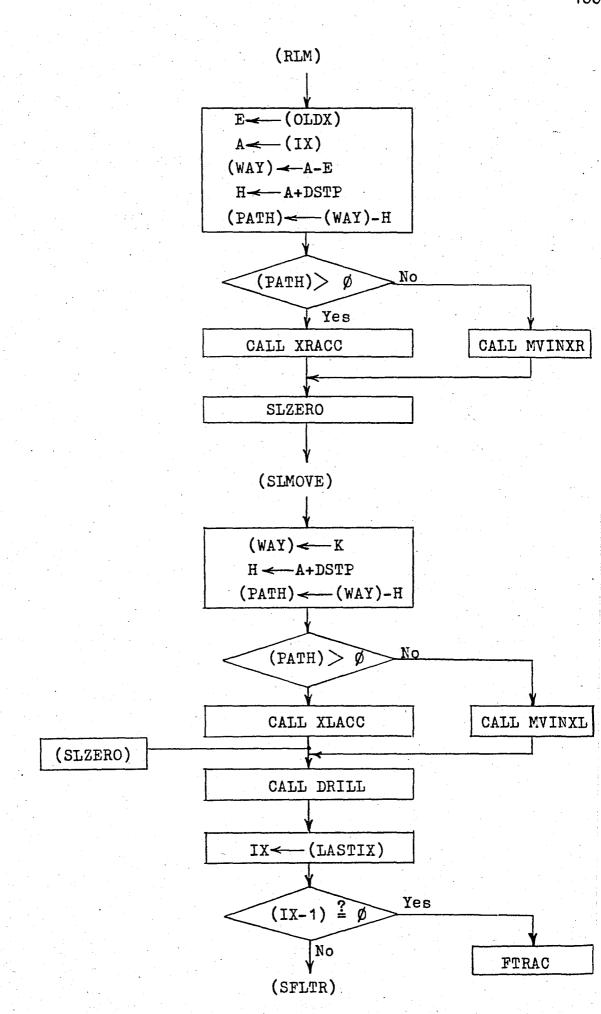
Drill Program (For odd lines) B --- 9Ø H HL ---872D H $(HL) \leftarrow \phi \phi$ HL←HL+1 $B \stackrel{?}{=} \phi$ No Yes $C \leftarrow (XINC)$ (OLDX)←A D - (YLNGTH) HL -- STRAM IX FRSTIX X--ø BIT X, HL No BITX = Ø Yes (IX)- C C--- C - 1 No c ≟ ø -IX+1 IX < YYes $IX \leftarrow IX-1$ -X+1X <-- HL --- HL+1 No (SAVEHL) --- HL IX --- FRSTIX CALL MOVINY Yes -HL+1 HL-Yes (IX).OR.(IX+1)=0> FTR

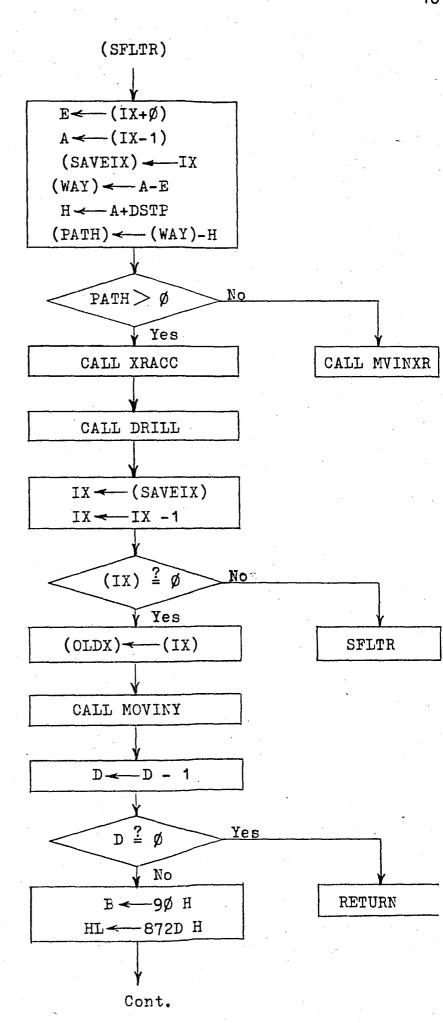
Cont

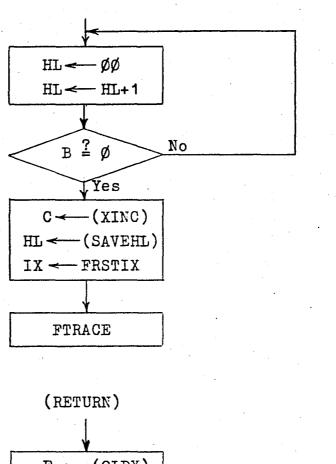


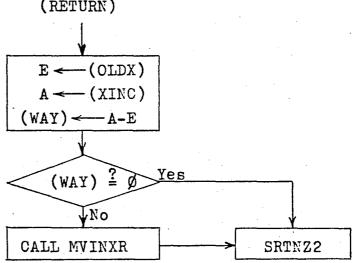






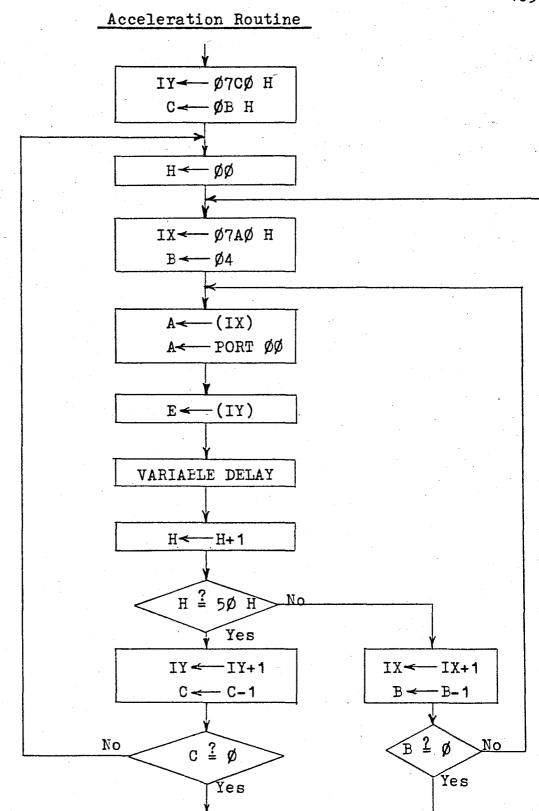


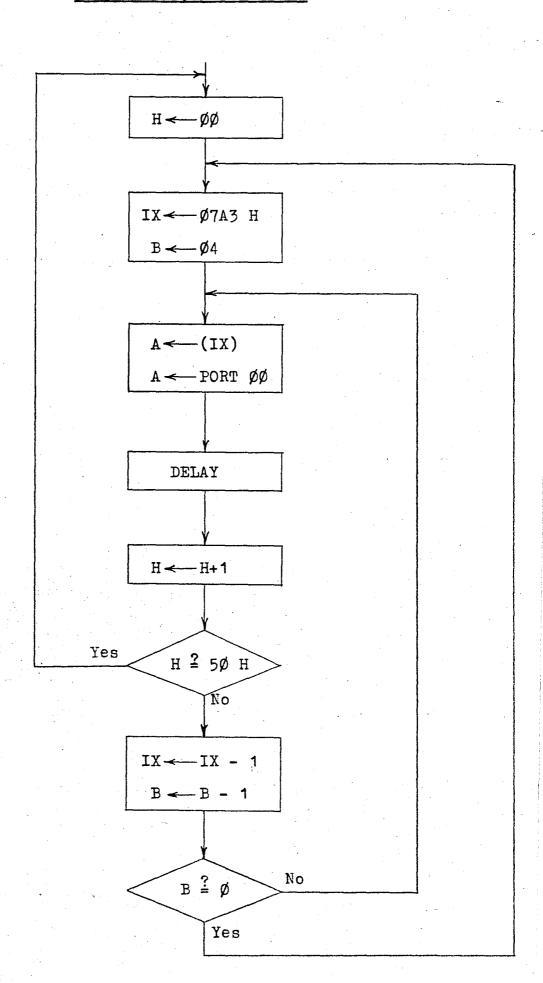




Drill Program
(For even lines)

The same flowchart (which is written for odd lines) can be used, with certain changes, for the even lines also. These changes can be understood by looking at the related sections of the drill program listing.





```
øøøø
        XLNGTH : EQU 87FØH
                            :Memory location for X-length
øøø1
        XPATH
               : EQU 87F1H
                            ; Memory location for X-path
øøø2
        YLNGTH : EQU 87F2H
                            :Memory location for Y-length
øøø3
        YPA TH
               : EQU 87F3H
                            :Memory location for Y-path
ØØØ4
        XSTEP1 : EQU Ø7AØH
                            :Location of first X-motor const
ØØØ5
        XSTEP4 : EQU Ø7A3H
                            ;Location of last X-motor consta
øøø6
        YSTEP1 : EQU Ø7BØH
                            ;Location of first Y-motor const
øøø7
                             :Location of last Y-motor consta
        YSTEP4 : EQU Ø7B3H
øøø8
        XINC
               : EQU 87F4H
                             ;Location of incremented x-lengt
øøø9
                             : " of twice "
        XL2
               : EQU 87E8H
                                                 x-length
øølø
        LOCL
               : EQU 87F5H
                             :Location of byte count
ØØ11
        LOC2
               : EQU 87F6H
                             ;Location of incomplete store by
ØØ12
        STAM
               : EQU 87FAH
                             ;Starting address location of me
ØØ13
        SAVEHL: EQU 87EEH
                             ;Location to save HL registers
ØØ14
                             ;Location to save IX register
        SAVEIX: EQU 87FCH
ØØ15
        LASTIX : EQU 87F8H
                                    to store last IX content
                             ;
ØØ16
        OIDX
               : EQU 87ECH
                                    to store old position of
ØØ17
        FRSTIX : EQU 873ØH
                                    to store first IX content
               : EQU 87F7H
                             :Location to store distance path
øø18
        PATH
ØØ19
        WAY
               : EQU 87EBH
                             ;Location to store length way
ØØ2Ø
               : EQU 8ØØØH
                             :Starting address of RAM
        STRAM
ØØ21
        A+DSTP : EQU 15H
                             ;Sum of acceleration+dec. steps
        ACOUNT : EQU ØBH
ØØ22
                             :Acceleration steps
ØØ23
        DCOUNT : EQU ØAH
                             Deceleration steps
               : EQU Ø4H
ØØ24
        COUNT
                             ; Motor pulse sequence steps
               : EQU Ø8H
ØØ25
        BYTE
                             ;Bit count in a byte
                : EQU Ø1H
ØØ26
        STEP
                             One step length
ØØ27
        GRID
               : EQU 5ØH
                             ;One grid length, 80D steps
ØØ28
        MAXSPD : EQU 12H
                             ; Maximum speed constant
```

			•	
ØØ29			ID IX,87F5H	
øø3ø	÷		LD (IX+ØØ),Ø8H	
ØØ31		•	LD (IX+Ø1),ØØH	
ØØ32			ID HL,8ØØØH	
øø33			LD (STAM), HL	
ØØ34	NGY	. :	LD HL, YSTEP4	;Frame Detection Program
ØØ35			LD B, COUNT	
øø36	OUT	:	LD A, (HL)	;Move in 4-step sequence
øø37			OUT (PORTØ),A	;and input data
øø38			CALL DLY	
øø39			DEC HL	
øø4ø	•		DJNZ OUT	
ØØ41			JP NC, IN1	
ØØ42			DEC C	
ØØ43			JP Z,STOP	
ØØ44			IN A, (PORTL)	
ØØ45			BIT Ø,A	
ØØ46			JP NZ,NGY	
ØØ47			CCF	
øø48			JP NGY	
øø49	INl	:	IN A, (PORT1)	
øø5ø	*		BIT Ø,A	
ØØ51			JP Z,NGY	;If input is zero continue
øø52			LD C,11H	;to move,if not move 68 mor
øø53			SCF	;steps to determine the dep
ØØ54	· ~		JP NGY	
ØØ55	STOP	:	XOR A	
øø56			OUT (PORTØ),A	
ØØ57			LD B, FFH	
4 4	* *			

		· ·	•
ØØ58	D EL1	: CALL DLY	
øø59	. :	DJNZ DEL1	
øø6ø		LD C,29H	;Move out from the upper fr
øø61	PSY	: LD HL, YSTEP1	
ØØ62		LD B, COUNT	
øø63	оитз	: LD A, (HL)	
øø64	· .	OUT (PORTØ),A	
øø65		CALL DLY	
øø66		INC HL	
øø67	· · · · · · · · · · · · · · · · · · ·	DJNZ OUT3	
øø68		DEC C	
øø69	· · · · · · · · · · · · · · · · · · ·	JP NZ, PSY	
øø7ø		XOR A	
øø71		OUT (PORTØ),A	
ØØ72		LD B, FFH	
ØØ73	DEL2	: CALL DLY	
øø74		DJNZ DEL2	
ØØ75	NGX	: LD HL, XSTEP1	;Search for the right side
øø76		LD B, COUNT	;frame line
øø77	OUT2	: LD A, (HL)	
øø78		OUT (PORTØ), A	
ØØ79		CALL DLY	
øø8ø		INC HL	
ØØ81		DJNZ OUT2	
øø82		IN A, (PORT1)	
øø83		BIT Ø, A	
øø84		JP Z,NGX	
øø85		XOR A	
øø86		OUT (PORTØ),A	
		and the second s	

ØØ87	•	ID B, FFH	
ØØ88	DEL3	: CALL DLY	
ØØ89		DJNZ DEL3	
øø90		LD C,2ØH	;Move out from the right side
ØØ91	PSX	: LD HL, XSTEP4	;frame
ØØ92	· .	LD B, COUNT	
ØØ93	OUT4	: LD A, (HL)	
ØØ94		OUT (PORTØ),A	
ØØ95		CALL DLY	
øø96		DEC HL	
ØØ97		DJNZ OUT4	
ØØ98		DEC C	
ØØ99		JP NZ,PSX	
ø1øø		XOR A	;Stop on the zero position
ØlØl		OUT (PORTØ),A	;location
ØlØ2	_	LD B, FF	
Ø1Ø3	DEL4	: CALL DLY	
ØlØ4		DJNZ DEL4	
Ø1Ø5	FRIGTH	: LD L,ØØ	;Frame length program
ØlØ6	FPSX	: LD A, STEP	;Measure x-length
Ø1Ø7		LD (WAY),A	
Ø1Ø8		CALL MVINXL	
Ø1Ø9		INC L	
ØllØ		IN A, (PORT1)	
Ølll		BIT Ø, A	
Ø112		JP Z,FPSX	
Ø113		XOR A	
Ø114		OUT (PORTØ), A	
Ø115		LD B, FFH	
			·

Ø116	DEL5	CALL DLY	
Ø117		DJNZ DEL5	
Ø118		DEC L	
Ø119		DEC L	
Ø12Ø		ID DE, XLNGTH	
Ø121		LD A, L	
Ø122		LD (DE),A	
Ø123		INC L	
Ø124		INC L	
Ø125		LD A, L	
Ø126		SUB A+DSTP	
Ø127		LD (XPATH), A	
Ø128		ID (PATH), A	
Ø129		LD A, L	
Ø13Ø		LD (WAY),A	
Ø131	•	CALL Z, MVINXR	
Ø132	•	JP Z,DLX	
Ø133		CALL C, MV INXR	
Ø134		JP C,DLX	
Ø135	,	CALL XRACC	
Ø136	DTX	: LD B, FFH	
Ø137	DEL6	: CALL DLY	
Ø138		DJNZ DEL6	
Ø139		ID L,ØØ	
Ø14Ø	FPSY	: LD A, STEP	;Measure y-length
Ø141		LD (WAY), A	
Ø142		CALL MVINYD	
Ø143		INC L	
Ø144	•	IN A, (PORTL)	•

7.		
Ø145		BIT Ø, A
Ø146		JP Z,FPSY
Ø147		XOR A
Ø148		OUT (PORTØ), A
Ø14 9		ID B, FFH
Ø15Ø	DEL7 :	CALL DLY
Ø151		DJNZ DEL7
Ø152		DEC L
Ø153		DEC L
Ø154		LD DE, YLNGTH
Ø155		ID A, L
Ø156		LD (DE),A
Ø157		INC L
Ø158		INC L
Ø159		LD A, L
Ø16Ø		SUB A+DSTP
Ø161		LD (YPATH), A
Ø162	talining of the second of the	LD (PATH), A
Ø163		LD A, L
Ø164		ID (WAY),A
Ø165		CALL Z, MVINYU
Ø166		JP Z,DLYY
Ø167		CALL C, MVINYU
Ø168		JP C,DLYY
Ø169		CALL YUACC
Ø17Ø	DLYY :	LD B, FFH
Ø171	DEL8 :	CALL DLY
Ø172		DJNZ DEL8
Ø173		LD A, (XPATH)

Ø174		DEC A
Ø175		DEC A
Ø176		LD (XPATH), A
Ø177		LD A, (YPATH)
Ø178		DEC A
Ø179		DEC A
Ø18Ø		LD (YPATH), A
Ø181		LD A, (XINGTH)
Ø182		INC A
Ø183	4	LD (XINC), A
Ø184		INC A
Ø185	: · · ·	LD (XL2),A
Ø186	SCANPR :	LD A, (XLNGTH) ;Scanning Program
Ø187		SUB A+DSTP ; Test for constant speed scan
Ø188		JP Z, CSCAN ; or by acceleration
Ø189		JP C, CSCAN
ø19ø		LD A, (YLNGTH)
Ø191		LD L, A
Ø192		CALL STORE
Ø193	SXPA	LD IY, ACONS ;Start scanning the first line
Ø194		LD C, ACOUNT ; by acceleration
Ø195	SXPAH	ID H,ØØ
Ø196	SXPAR	ID IX, XSTEP4
Ø197		LD B, COUNT
Ø198	SXPAM	ID A, $(IX+\emptyset\emptyset)$
Ø199	•	OUT (PORTØ), A
ø2øø		LD E, $(IY+\emptyset\emptyset)$
ø2Ø1		CALL VDLY

ø2ø2

INC H

Ø2Ø3		ID A, GRID
Ø2Ø4		СР Н
Ø2Ø5		JR Z+9
ø2ø6		DEC IX
Ø2Ø7		DJNZ SXPAM
ø 2 ø 8	• •	JP SXPAR
ø2ø9		INC IY
Ø21Ø		CALL STORE
Ø211		DEC C
Ø212		JP NZ, SXPAH
Ø213		PUSH HL
Ø214		ID HL, XPATH
Ø215		ID C, (HL)
Ø216		POP HL
Ø217	SXAPH :	LD H, ØØ
Ø218	SXAPS :	: LD IX, XSTEP4 ;Scanning with maximum speed
Ø219		LD B, COUNT
Ø22Ø	SXAPM :	$ID A, (IX+\emptyset\emptyset)$
Ø221		OUT (PORTØ), A
Ø222		ID E, MAXSPD
Ø223		CALL VDLY
Ø224		INC H
Ø225		LD A, GRID
Ø226		CP H
Ø227		JR Z,+ 9
Ø228		DEC IX
Ø229		DJNZ SXAPM
Ø23Ø		JP SXAPS

CALL STORE

,			the second second second second	•					
Ø232			DEC C						
Ø233			JP NZ, SXAPH				•		
Ø234	SXPD	:	LD IY, DCONS	;Sta	rt	to	dece	lerat	e
Ø235			ID C,DCOUNT						
Ø236	SXPDH	:	ID H,ØØ						
Ø237	SXPDR	:	LD IX, XSTEP4	*.					
Ø238	.*		ID B, COUNT					· .	
Ø239	SXPDM	:	ID A,($IX+\emptyset\emptyset$)						
Ø24Ø			OUT (PORTØ),A					٠	
Ø241			ID E, $(IY+\emptyset\emptyset)$						
Ø242			CALL VDLY						
Ø243			INC H						
Ø244			ID A,GRID						
Ø245			CP H						
Ø246			JR Z,+9				. *		
Ø247			DEC IX						
Ø248			DJNZ SXPDM	•					
Ø249			JP SXPDR					*	
Ø25Ø			INC IY						
Ø251			CALL STORE						
Ø252			DEC C			•			
Ø253			JP NZ, SXPDH						
Ø254			EXX						
Ø255			EX AF, AF						
Ø256	**************************************		ID HL, LOCI		٠.				
Ø257			LD C, (HL)						
Ø258			LD A, BYTE						
Ø259			AND C					No.	

JP NZ,SX1

ø26ø

```
Ø261
                  CALL LASTST
Ø261
                  JP SP1
Ø262
                : EX AF, AF'
        SX1
Ø263.
                  EXX
Ø264
        SPl
                : XOR A
                           ;Stop at the end of the line
                  OUT (PORTØ), A
Ø265
Ø266
                  LD B, 1FH
Ø267
         SDELl
                : CALL DLY
Ø268
                  DJNZ SDEL1
Ø269
                  LD A, STEP
Ø27Ø
                  ID (WAY), A
Ø271
                 CALL MVINYD ; Move one grid down
Ø272
                  LD B, 1FH
Ø273
         SDEL2 : CALL DLY
Ø274
                  DJNZ SDEL2
Ø275
                  DEC L
                                  ;Test whether the card is
Ø276
                  JP Z.SRTNZ1
                                 ;finished, if yes, return to
Ø277
                  CALL STORE
                                  ;zero position
Ø278
         SXNA : LD IY, ACONS ; if not, scan the next line
Ø279
                   LD C, ACOUNT
Ø28Ø
                : LD H,ØØ
         SXNAH
Ø281
         SXNAR
                : LD IX.XSTEP1
Ø282
                   ID B, COUNT
Ø283
                : LD A, (IX+\emptyset\emptyset)
         SXNAM
                 OUT (PORTØ), A
Ø284
                   LD E, (IY+\emptyset\emptyset)
Ø285
Ø286
                   CALL VDLY
Ø287
                   INC H
```

LD A, GRID

		•
Ø289		CP H
Ø29Ø		JR Z+9
Ø291	•	INC IX
Ø292		DJNZ SXNAM
Ø293		JP SXNAR
Ø294	•	INC IY
Ø295		CALL STORE
Ø296		DEC C
Ø297		JP NZ, SXNAH
Ø298		PUSH HL
Ø299		LD HL, XPATH
Ø3ØØ		LD C, (HL)
ø3ø1		POP HL
ø3ø2	SXDPH	: LD H,ØØ
ø3ø3	SXDPS	: LD IX,XSTEP1
Ø3Ø4		LD B, COUNT
ø3ø5	SXDPM	: LD A, (IX+ØØ)
ø3ø6		OUT (PORTØ), A
Ø3Ø7		ID E, MAXSPD
ø3ø8		CALL VDLY
Ø 3 Ø 9		INC H
Ø31Ø		LD A,GRID
Ø311		CP H
Ø312		JR Z+9
Ø313		INC IX
Ø314		DJNZ SXDPM
Ø315		JP SXDPS
Ø316		CALL STORE
Ø317		DEC C
		· · · · · · · · · · · · · · · · · · ·

Ø318		JP NZ, SXDPH
Ø319	SXND	: LD IY, DCONS
Ø32Ø		LD C, DCOUNT
Ø321	SXNDH	: LD H,ØØ
Ø322	SXNDR	: LD IX,XSTEP1
Ø323		LD B, COUNT
Ø324	SXNDM	: LD A, $(IX+\emptyset\emptyset)$
Ø325		OUT (PORTØ),A
ø326		LD E, $(IY+\emptyset\emptyset)$
Ø327		CALL VDLY
ø 328		INC H
ø329	• .	ID A, GRID
Ø33Ø	•	CP H
Ø331		JR Z,+9
Ø332		INC IX
Ø333		DJNZ SXNDM
Ø334		JP SXNDR
Ø335		INC IY
Ø336		CALL STORE
Ø337		DEC C
ø338		JP NZ, SXNDM
Ø339		EXX
Ø34Ø		EX AF, AF
Ø341		ID HL, LOC1
Ø342		ID C, (HL)
Ø343		LD A, BYTE
Ø344		AND C
ø345		JP NZ,SX2
Ø346		CALL LASTST

Ø347		JP SP2	
Ø348	SX2	EX AF, AF	
Ø349		EXX	
Ø35Ø	SP2	: XOR A	
ø351		OUT (PORTØ),A	
Ø352	; ,	LD B,1FH	
Ø353	SDEL3	: CALL DLY	
Ø354		DJNZ SDEL3	
Ø355		LD A, STEP	
Ø356		LD (WAY),A	
Ø357		CALL MVINYD	
Ø358		CALL STORE	
ø359		LD B,1FH	
Ø36Ø	SDELR	: CALL DLY	
ø361		DJNZ SDELR	
Ø361		DEC L	
ø362		JP Z, SRTNZ2	
ø363		JP SXPA	
Ø364	CSCAN	: LD A, (YLNGTH)	;Constant Speed Scanning Prog
Ø365	. *	LD L,A	
ø366		CALL STORE	
ø367	CSTART	: LD A, (XLNGTH)	
ø 368		LD C,A	
ø369	LCONT	: LD A, STEP	
Ø37Ø		ID (WAY),A	
Ø371		CALL MVINXL	
Ø372	•	CALL STORE	
Ø373		DEC C	

JP NZ, LCONT

Ø375		EXX
Ø376		EX AF, AF
Ø377		ID HL, LOCI
ø378		ID C, (HL)
ø379		LD A, BYTE
ø38ø		AND C
Ø381		JP NZ,CX1
Ø382		CALL LASTST
Ø383		JP CP1
Ø384	CX1 :	EX AF, AF
ø385		EXX
ø386	CP1 :	XOR A
ø387		OUT (PORTØ),A
Ø388		LD B, 1FH
ø 389	CDELL :	CALL DLY
ø39ø		DJNZ CDEL1
Ø391		ID A, STEP
Ø392		ID (WAY),A
Ø393		CALL MVINYD
Ø394		LD B,1FH
Ø395	SDEL3:	CALL, DLY
Ø396	· · · · · · · · · · · · · · · · · · ·	DJNZ SDEL3
Ø397		DEC L
ø398		JP Z,SRTNZl
Ø399		CALL STORE
Ø4ØØ		LD A, (XLNGTH)
Ø4Ø1		LD C,A
Ø4Ø2	RCONT:	LD A, STEP
Ø4Ø3		LD (WAY),A

Ø4Ø4			CALL MVINXR	
Ø4Ø5			CALL STORE	
Ø4Ø6			DEC C	
Ø4Ø7			JP NZ, RCONT	
Ø4Ø8	•		EXX	
Ø4Ø9			EX AF, AF	
Ø41Ø			ID HL, LOCI	
Ø411			LD C, (HL)	
Ø412			LD A, BYTE	
Ø413			AND C	
Ø414		•	JP NZ,CX2	
Ø415			CALL LASTST	
Ø416	•		JP CP2	
Ø417	CX2	:	EX AF, AF	
Ø418			EXX	
Ø419	CP2	:	XOR A	
Ø42Ø	·		OUT (PORTØ),A	
Ø421			ID B, 1FH	
Ø422	SDELR	:	CALL DLY	
Ø423			DJNZ SDELR	
Ø 424			LD A, STEP	
Ø425			LD (WAY),A	
Ø426	1 · 1		CALL MVINYD	
Ø427			DEC L	
Ø428			JP Z,SRTNZ2	
Ø429	•		CALL STORE	
Ø43Ø			JP CSTART	
Ø431	STORE	:	EXX	;Store Program
Ø432			EX AF, AF	
			*	

Ø433		IN A, (PORTL)	
Ø434		ID HL, LOC2	
Ø435		ID B, (HL)	
Ø436		RRC B	
Ø437		OR B	
Ø438		ID HL, LOC1	
Ø439		LD C, (HL)	
Ø44Ø		LD (LOC2),A	
Ø441		DEC C	
Ø441		LD (HL),C	
Ø442		JP Z,STM	
Ø443		EX AF, AF	
Ø444		EXX	
Ø445		RET	
Ø446	LASTST	ID A, (LOC1)	;Last store
Ø447		LD B, A	
Ø448	•	ID A, (LOC2)	
Ø4 49	ROT	RRC A	
Ø45Ø		DJNZ ROT	
Ø451		ID (IOC2),A	
Ø452	STM	ID A, (LOC2)	;Store to memory
Ø453		RRC A	
Ø454		LD HL, (STAM)	
Ø455		LD (HL),A	
Ø456		INC HL	
Ø457		LD (STAM), HL	
Ø458		LD A, BYTE	
Ø459		ID (LOC1),A	
Ø46Ø		LD A,ØØ	
A	•		

Ø461	LD (LOC2),A
Ø462	EX AF, AF'
Ø463	EXX
Ø464	RET
Ø465	SRTNZ1 : LD B, FFH ;Return to zero position from
Ø466	SDELX : CALL DLY ; an odd numbered line
Ø467	DJNZ SDELX
Ø468	LD A, (XLNGTH)
Ø469	ID (WAY),A
Ø47Ø	SUB A+DSTP
Ø471	CALL Z, MVINXR
Ø472	JP Z, SRTNZ2
Ø473	CALL C, MVINXR
Ø474	JP C, SRTN Z2
Ø475	LD A, (XPATH)
Ø476	LD (PATH), A
Ø477	CALL XRACC
Ø478	SRTN Z2: LD B, FFH; Return to zero-position from
Ø479	SDEL4 : CALL DLY ;an even-line
Ø48Ø	DJNZ SDEL4
Ø481	LD A, (YLNGTH)
Ø482	LD (WAY),A
Ø483	SUB A+DSTP
Ø484	CALL Z, MVINYU
Ø485	JP Z, END
Ø486	CALL C, MVINYU
Ø487	JP C, END
Ø488	ID A, (YPATH)
Ø489	LD (PATH),A

Ø49Ø		CALL YUACC	
Ø491	END :	XOR A	
Ø492		OUT (PORTØ),A	
Ø493		LD B, FFH	
Ø494	SDEL5 :	CALL DLY	
Ø495		DJNZ SDEL5	
ø 496		LD B,9ØH	;DRILLING Program
Ø497		LD HL,872DH	
ø 498	zerø :	INC HL	
ø 499		ID (HL),ØØ	
ø5øø		DJNZ ZERØ	
ø5ø1		LD A, (XINC)	
ø5ø2		LD C,A	
ø5ø3		LD (OLDX),A	
Ø5Ø4		SRL A	
Ø5Ø5		ID (HALFX), A	
ø5ø6		LD A, (YLNGTH)	
ø5ø7		LD D,A	
ø5ø8		LD HL, STRAM	
ø5 ø9		LD IX, FRSTIX	
Ø51Ø		JP STR	
Ø511	FTRACE :	BIT Ø, (HL)	;Routine to trace an even-li
Ø512		JP NZ, FLDØ	
Ø513	FTRØ :	DEC C	
Ø514		JP Z,NXTLIN	
Ø515		BIT 1, (HL)	
Ø516		JP NZ, FLD1	
Ø517	FTRl :	DEC C	
Ø518		JP Z,NXTLIN	
4.			

Ø519		BIT 2, (HL)
ø52ø		JP NZ, FLD2
Ø521	FTR2	: DEC C
Ø522		JP Z,NXTLIN
Ø523		BIT 3,(HL)
Ø524		JP NZ, FLD3
ø525	FTR3	: DEC C
ø526		JP Z,NXTLIN
Ø527		BIT 4,(HL)
ø52 8		JP NZ, FLD4
Ø52 9	FTR4	: DEC C
Ø53Ø	•	JP Z,NXTLIN
Ø531		BIT 5,(HL)
Ø532		JP NZ, FLD5
Ø533	FTR5	: DEC C
Ø534		JP Z,NXTLIN
Ø535		BIT 6, (HL)
ø536	:	JP NZ, FLD6
ø537	FTR6	: DEC C
ø 538		JP Z,NXTLIN
Ø539		BIT 7, (HL)
Ø54Ø		JP NZ, FLD7
Ø541	FTR7	: DEC C
Ø542		JP Z,NXTLIN
Ø543		INC HL
Ø544		JP FTRACE
Ø545	FLDØ	: LD A, (XL2)
Ø546		SUB C
Ø547		ID (IX+Ø),A

```
Ø548
                    INC IX
Ø549
                    JP FTRØ
Ø56Ø
         FLD1
                  : LD A, (XL2)
Ø561
                    SUB C
Ø562
                    ID (IX+\emptyset), A
Ø563
                    INC IX
Ø564
                    JP FTR1
Ø565
                  : LD A, (XL2)
         FLD2
Ø566
                    SUB C
Ø567
                    LD (IX+\emptyset), A
Ø568
                    INC IX
Ø569
                    JP FTR2
Ø57Ø
                  : LD A, (XL2)
         FLD3
Ø571
                    SUB C
                    LD (IX+\emptyset), A
Ø572
Ø573
                    INC IX
Ø574
                    JP FTR3
Ø575
                  : LD A, (XL2)
         FLD4
Ø576
                    SUB C
Ø577
                    LD (IX+\emptyset), A
Ø578
                    INC IX
Ø579
                    JP FTR4
Ø58Ø
                  : LD A, (XL2)
         FLD5
Ø581
                    SUB C
                    ID (IX+\emptyset),A
Ø582
Ø583
                    INC IX
Ø584
                    JP FTR5
                  : LD A, (XL2)
Ø585
         FLD6
Ø586
                    SUB C
```

```
ID (IX+\emptyset),A.
Ø587
Ø588
                   INC IX
                   JP FTR6
Ø589
Ø59Ø
         FLD7 : LD A, (XL2)
Ø591
                   SUB C
                   LD (IX+\emptyset), A
Ø592
Ø593
                   INC IX
Ø594
                   JP FTR7
Ø595
         NXTLIN : DEC IX
Ø596
                   ID (LASTIX), IX
Ø597
                   INC HL
Ø598
                   LD (SAVEHL), HL
                   LD IX, FRSTIX ; Test whether there is a hole
Ø599
Ø6ØØ
                   ID A_{\bullet}(IX+\emptyset) ; on this line
Ø6Ø1
                   ID E, (IX+1)
Ø6Ø2
                   OR E
                   CALL Z, MOVINY
Ø6Ø3
                   JP Z,STRACE
Ø6Ø4
                   ID A, (IX+1)
Ø6Ø5
                                 ;Test whether there is only
                   LD E, (IX+2)
Ø6Ø6
                                    ;one hole
Ø6Ø7
                   OR E
Ø6Ø8
                   JP Z, FLEFT
Ø6Ø9
                   ID A, (OLDX)
Ø61Ø
                   LD E.A
Ø611
                   ID IX, (LASTIX)
                   ID A, (IX+\emptyset)
Ø612
Ø613
                   SUB E
Ø614
                   JP Z, RZERO
Ø615
                    JP C, LRM
```

	•				
Ø616		ID B,A			
Ø617	6	LD A, (FRSTIX)			
ø61 8		LD E,A		- 1	
ø619		LD A, (OLDX)			
Ø62Ø	•	SUB E			
ø621		JP Z, LZERO		•	
Ø622		JP C,RM			
ø623	•	SUB B			
Ø624		JP NC, FRIGHT			
Ø625		JP FLEFT			
Ø626	FRIGHT:	ID A, (OLDX)	;Routine	to move	right
ø627		LD E,A	•		
ø62 8		LD IX, (LASTIX)			
ø 629		LD A, $(IX+\emptyset)$			
ø63ø		SUB E			
ø631		JP Z, RZERO			
ø632		JP NC, RMOVE			
ø633	LRM :	ID A, $(IX+\emptyset)$			
Ø634		LD E,A	·		
ø635	•	LD A, (OLDX)			·
Ø636		SUB E			
ø637		ID (WAY),A	. •	,	
ø638		LD H, A+DSTP			
ø639		SUB H			
Ø64Ø		CALL Z, MVINXL			
Ø641 \		JP Z,RZERO			
Ø642		CALL C, MVINXL	•		
Ø643		JC C, RZERO			-
Ø644		LD (PATH), A			•

Ø645		CALL XLACC				
Ø646		JP RZERO				
Ø647	FLEFT :	ID A, (FRSTIX)	;Routine	to	move	leſt
Ø648		LD E,A				
Ø649		ID A, (OLDX)				
ø65ø		SUB E				
Ø651		JP LZERO				
Ø652		JP NC, LMOVE				
Ø653	RM :	LD A, (OLDX)				
Ø654		LD E,A				
Ø655		LD A, (FRSTIX)				
Ø656		SUB E		•		
ø657		ID (WAY),A				
ø658		ID H,A+DSTP				
Ø659		SUB H				*
ø66ø		CALL Z, MVINXR			:	
Ø661		JP Z,LZERO				
Ø662		CALL C, MVINXR				
ø663		JP C, LZERO				
Ø664	V	LD (PATH), A				
Ø665		CALL XRACC	*			
Ø666		JP LZERO				
ø667	RMOVE :	LD (WAY),A			-	
ø668	RATEST:	LD H, A+DSTP				
ø669		SUB H				
Ø67Ø		CALL Z, MVINXR				
Ø671		JP Z,RZERO				
Ø672		CALL C, MVINXR				

JP C,RZERO

ø673

Ø674		LD (PATH), A	
Ø675	•	CALL XRACC	
ø676	RZERO	: NOP	
ø677		CALL DRILL	
Ø678		ID IX, (LASTIX)	
Ø679		ID A, (IX-1)	
ø68ø		OR A	
Ø681		JP Z,STRAC	
Ø682	FRRTL	: LD E, (IX-1)	;Routine to move from right
Ø683		LD A, (IX+Ø)	;to left on an evenline
Ø684		ID (SAVEIX), IX	
ø685		SUB E	
ø686		LD (WAY), A	
Ø687		LD H,A+DSTP	
Ø688		SUB H	
Ø689		CALL Z, MVINXL	
Ø69Ø		JP Z,DL	
Ø691		CALL C, MVINXL	
ø692		JP C,DL	
ø693		LD (PATH), A	
ø694		CALL XLACC	
ø695	DT	: NOP	
ø696	•	CALL DRILL	
ø697		LD IX, (SAVEIX)	
Ø698		DEC IX	
ø699		ID A, (IX-1)	
ø7øø		OR A	
Ø7Ø1		JP Z,STRAC	
Ø7Ø2		JP FRRTL	

			• .
Ø7Ø3	LMOVE :	LD (WAY),A	
Ø7Ø4	LATEST :	ID H, A+DSTP	
Ø7Ø5		LD A, (WAY)	
ø7ø6		SUB H	•
Ø7Ø7		CALL Z, MVINXL	
ø 7ø8		JP Z,LZERO	
ø 7 ø 9		CALL C, MVINXL	
Ø71Ø		JP C, LZERO	
Ø711	•	LD (PATH),A	
Ø712		CALL XLACC	
Ø713	LZERO :	NOP	
Ø714		CALL DRILL	
Ø715		LD IX, FRSTIX	
Ø716		LD A, (IX+1)	
Ø717		OR A	
Ø718		JP Z,STRAC	
Ø719	FRLTR :	LD E, $(IX+\emptyset)$;Routine to move from left
Ø72Ø		LD A,(IX+1)	;to right on an evenline
Ø721		ID (SAVEIX), IX	
Ø722		SUB E	
Ø723		LD (WAY), A	
Ø724		LD H, A+DSTP	
Ø725		SUB H	
ø726		CALL Z, MVINXR	
Ø727		JP Z,DR	
Ø728		CALL C, MVINXR	
Ø729		JP C,DR	
Ø73Ø		ID (PATH),A	
Ø731		CALL XRACC	

```
Ø732
        DR ·
                : NOP
Ø733
                  CALL DRILL
Ø734
                  LD IX, (SAVEIX)
Ø735
                  INC IX
Ø736
                  LD A,(IX+1)
Ø737
                  OR A
Ø738
                  JP Z,STRAC
Ø739
                  JP FRLTR
Ø74Ø
        DRILL : EXX
                                  ;Drill simulating routine
Ø741
                  EX AF, AF
Ø742
                  XOR A
Ø743
                  OUT (PORTØ), A
Ø744
                  LD A,8ØH
Ø745
                  OUT (PORT1),A
Ø746
                  LD B.7FH
Ø747
        DR2
                : CALL DLY
Ø748
                  DJNZ DR2
Ø749
                  XOR A
Ø75Ø
                  OUT (PORTI),A
Ø751
                  EX AF. AF
Ø752
                  EXX
Ø753
                  RET
Ø754
                : LD A, (IX+\emptyset)
         STRAC
Ø755
                  LD (OLDX), A
Ø756
                  CALL MOVINY
Ø757
         STRACE : DEC D
                  JP Z, RETURN
Ø758
Ø759
                  LD B,9ØH
```

LD HL,872DH

Ø76Ø

•				
Ø761	SZERO	: INC HL		
Ø762		ID (HL),ØØ		
Ø763		DJNZ SZERO		
Ø764		LD A, (XINC)		
Ø765		LD C,A		
Ø766		LD HL, (SAVEHL)		
Ø767		ID IX, FRSTIX		
Ø768	STR	: BIT Ø,HL	;Routine to trace	an odd-line
ø769		JP NZ,SØ		
Ø77Ø	RØ	: DEC C		
Ø771		JP Z, SECLIN		
Ø772		BIT 1, (HL)		
Ø773		JP NZ,S1		
Ø774	Rl	: DEC C		
Ø775		JP Z, SECLIN		
Ø776		BIT 2,(HL)		
Ø777		JP NZ,S2		
Ø778	R2	: DEC C		
Ø779		JP Z, SECLIN		
Ø78Ø		BIT 3, (HL)		
Ø781	•	JP NZ,S3		•
Ø782	R3	: DEC C		
Ø783		JP Z, SECLIN		•.
¢784		BIT 4,(HL)		
Ø785		JP NZ,S4		
ø786	R4	: DEC C		
ø787		JP Z, SECLIN		
ø788	.•	BIT 5,(HL)		
• •				-

JP NZ,S5

Ø79Ø	R5	. :	DEC C
Ø791			JP Z, SECLIN
Ø7 92			BIT 6, (HL)
Ø793			JP NZ, S6
Ø794	R6	:	DEC C
Ø795			JP Z, SECLIN
Ø796			BIT 7, (HL)
Ø797		~	JP NZ,S7
Ø798	R7	:	DEC C
Ø799			JP Z, SECLIN
Ø8ØØ			INC HL
Ø8Ø1			JP STR
Ø8Ø2	sø	:	ID $(IX+\emptyset),C$
ø8ø3 ·			INC IX
Ø8Ø4			JP RØ
Ø8Ø5	Sl	:	ID $(IX+\emptyset),C$
Ø8Ø6			INC IX
Ø8Ø7			JP Rl
Ø8Ø8	S2	:	ID $(IX+\emptyset),C$
Ø8Ø9			INC IX
Ø81Ø			JP R2
Ø811	S3	:	ID $(IX+\emptyset),C$
Ø812			INC IX
Ø813			JP R3
Ø814	S4	:	ID $(IX+\emptyset),C$
Ø815	:		INC IX
Ø816			JP R4
Ø817	S5	:	ID $(IX+\emptyset),C$
Ø818			INC IX

2020		
Ø819		JP R5
Ø82Ø	s6 :	ID (IX+Ø),C
Ø821		INC IX
Ø822		JP R6
Ø823	s7 :	ID (IX+Ø),C
Ø824		INC IX
Ø825		JP R7
Ø826	SECLIN:	DEC IX
Ø827	•	LD (LASTIX), IX
Ø828		INC HL
Ø829		LD (SAVEHL), HL
Ø83Ø		LD IX, FRSTIX
Ø8 3 1		LD A,(IX+Ø)
Ø832		ID E,(IX+1)
Ø834		OR E
Ø835		CALL Z, MOVINY
Ø836		JP Z,FTR
Ø837		LD A,(IX+1)
Ø838	·	ID A, (IX+2)
Ø839		OR E
Ø84Ø		JP Z, SRIGHT
Ø841		LD A, (OLDX)
Ø842		LD E, A
Ø843		ID A, (FRSTIX)
Ø844		SUB E
Ø845		JP Z, SRZERO
Ø846	•	JP C, HLMOVE
Ø847		LD B,A
Ø848		ID IX, (LASTIX)

Ø 849	ID E, $(IX+\emptyset)$	
Ø85Ø	LD A, (OLDX)	
Ø851	SUB E	
Ø852	JP Z, SLZERO	
Ø853	JP C, RLM	
Ø854	SUB B	
Ø855	JP C, SLEFT	
Ø856 SRIGHT:	LD A, (OLDX)	;Routine to move right on
Ø857	LD E, A	;an odd-line
Ø858	LD A, (FRSTIX)	
Ø859	SUB E	
Ø86Ø	JP Z, SRZERO	
Ø861	JP NC, SRMOVE	
Ø862 HLMOVE:	LD A, (FRSTIX)	
Ø863	LD E, A	
Ø864	LD A, (OLDX)	
Ø865	SUB E	
Ø866	LD (WAY),A	
Ø867	ID H, A+DSTP	
Ø868	SUB H	
Ø869	CALL Z, MVINXL	
Ø87Ø	JP Z, SRZERO	
Ø871	CALL C, MVINXL	
Ø872	JP C, SRZERO	
Ø873	LD (PATH), A	
Ø874	CALL XLACC	
Ø875	JP SRZERO	
Ø876 SRMOVE:	LD (WAY),A	
Ø877	LD H, A+DSTP	

Ø878	SUB H	
Ø879	CALL Z, MVINXR	
Ø88Ø	JP Z, SRZERO	
Ø881	CALL C, MVINXR	
Ø882	JP C, SRZERO	
Ø88 3	LD (PATH),A	
Ø884	CALL XRACC	
Ø885 SRZERO:	NOP	
Ø886	CALL DRILL	
Ø887	LD IX, FRSTIX	
Ø888	LD A, (IX+1)	
Ø 889	OR A	
Ø89Ø	JP Z, FTRAC	
Ø891 SFRTL:	LD E, (IX+1)	;Routine to move from right
Ø892	ID A, (IX+Ø)	;to left on an odd-line
ø893	LD (SAVEIX), IX	
Ø894	SUB E	
Ø895	LD (WAY),A	
ø896	LD H,A+DSTP	
Ø897	SUB H	
Ø898	CALL Z, MVINXL	
Ø899	JP Z,SDL	
ø9øø	CALL C, MVINXL	
Ø9Ø1	JP C,SDL	
ø9ø2	LD (PATH), A	
ø9ø3	CALL XLACC	
Ø9Ø4 SDL :	NOP	
ø9ø5	CALL DRILL	
Ø9Ø6	LD IX, (SAVEIX)	

Ø9Ø7		INC IX	
Ø9Ø8		ID A,(IX+1)	
Ø91Ø		OR A	
Ø911		JP Z,FTRAC	
Ø912		JP SFRTL	
Ø913	SLEFT :	LD IX, (LASTIX)	;Routine to move left or
Ø914		ID A, $(IX+\emptyset)$;an odd-line
Ø915		LD E,A	
Ø916	•	ID A, (OLDX)	
Ø917		SUB E	
ø 918		JP Z,SLZERO	
Ø919		JP NC, SLMOVE	
ø92ø	RLM :	LD A, (OLDX)	
Ø921		LD E,A	
Ø922		ID A, $(IX+\emptyset)$	
Ø923		SUB E	
Ø924		LD (WAY),A	
Ø925		LD H, A+DSTP	
Ø 926		SUB H	
Ø927		CALL Z, MVINXR	
Ø9 28		JP Z, SLZERO	
ø929		CALL C, MVINXR	
Ø93Ø		JP C, SLZERO	
Ø931		ID (PATH),A	
Ø932		CALL XRACC	
Ø933		JP SLZERO	
Ø934	SLMOVE :	LD (WAY),A	
Ø935		LD H, A+DSTP	
ø936		LD A, (WAY)	

			· · · · · · · · · · · · · · · · · · ·
Ø937		SUB H	
Ø938		CALL Z, MVINXL	
Ø939		JP Z,SLZERO	
Ø94Ø		CALL C, MVINXL	
Ø941		JP C, SLZERO	
Ø942		ID (PATH),A	
Ø943		CALL XLACC	
Ø944	SLZERO:	NOP	
Ø945		CALL DRILL	
Ø946		LD IX, (LASTIX)	
Ø947		LD A, (IX-1)	
Ø948		OR A	
Ø949		JP Z, FTRAC	
Ø95Ø	SFLTR :	ID E, (IX+Ø)	;Routine to move from left
Ø951		LD A, (IX-1)	;to right on an odd-line
Ø952		ID (SAVEIX), IX	• • • • • • • • • • • • • • • • • • •
Ø953		SUB E	
Ø954		LD (WAY),A	
Ø955		LD H, A+DSTP	
Ø956		SUB H	
Ø957		CALL Z, MVINXR	
ø958	,	JP Z, SDR	
Ø959		CALL C, MVINXR	
ø96ø		JP C, SDR	
ø961		ID (PATH),A	
ø962	•	CALL XRACC	
Ø963	SDR :	NOP	
ø964		CALL DRILL	
ø965		LD IX, (SAVEIX)	

			•
Ø966		DEC IX	
Ø967		ID A, (IX-1)	
ø968		OR A	
ø969		JP Z,FTRAC	
Ø97Ø		JP SFLTR	
Ø971	FTRAC :	ID A, (IX+Ø)	
Ø972	· .	LD (OLDX),A	
Ø973		CALL MOVINY	
Ø974	FTR :	DEC D	
Ø975		JP Z,RETURN	
Ø976		LD B,9ØH	
Ø977	. •	ID HL,872DH	
Ø978	ZR :	INC HL	
Ø979		LD (HL),ØØ	
ø98ø		DJNZ ZR	
Ø981		ID A, (XINC)	
ø982		LD C, A	
Ø983		ID HL, (SAVEHL))
ø984		LD IX, FRSTIX	
ø985		JP FTRACE	
ø986	RETURN :	LD A, (OLDX)	;Return to zero-position afte
ø987		ID E,A	;drilling of the whole card i
ø988		LD A, (XINC)	;finished
ø989		SUB E	
ø99ø		JP Z,SRTNZ2	
Ø991	• 1 .	ID (WAY),A	
Ø992		CALL MVINXR	
Ø993		JP SRTNZ2	

Ø994	MOVINY : LD A, STEP	;Routine to move one grid
Ø995	LD (WAY),A	;y-direction downwards.
ø 996	CALL MVINYD	
Ø997	RET	
Ø998	DLY : LD D,7DH	;Constant delay routine.
ø 999	LOOP : LD E,Ø3H	
ıøøø	DEC E	
ıøøı	JR NZ,-1	
1ØØ2	DEC D	
1ØØ3	JP NZ, LOOP	
1ØØ4	RET	
1ØØ5	VDLY : LD D,Ø8H	;Variable delay routine.
1øø6	IND : DEC D	
1ØØ7	JP NZ, IND	
1øø8	DEC E	
1ØØ9	JP NZ, VDLY	
ıøıø	RET	
ıøıı	MVINXL : EXX	;Routine to move left in
lø12	EX AF, AF'	;x-direction with constant
1Ø13	LD A, (WAY)	;speed.
1Ø14	ID C,A	
1Ø15	RH : LD H,ØØ	
1Ø16	RLINE : LD IX, XSTEP4	
1Ø17	LD B, COUNT	
1Ø18	RNEXT : ID A, $(IX+\emptyset\emptyset)$	
1Ø19	OUT (PORTØ), A	
1Ø2Ø	CALL DLY	
1Ø21	INC H	
1Ø22	LD A, GRID	

1Ø23	CP H	
1Ø24	JR Z,+9	
1ø25	DEC IX	
1ø26	DJNZ RNEXT	
1ø27	JP RLINE	
1ø28	DEC C	
1Ø29	JP NZ, RH	
1Ø3Ø	EXX	
1Ø31 ·	EX AF, AF	
1Ø32	RET	
1Ø33	MVINXR : EXX	;Routine to move right in
1Ø34	EX AF, AF	;x-direction with constant
1Ø35	LD A, (WAY)	;speed.
1ø36	LD C, A	
1Ø37	LH : LD H, ØØ	
1Ø38	LLINE : LD IX, XSTEP1	
1Ø39	LD B, COUNT	
1Ø4Ø	LNEXT : LD A, (IX+ $\phi\phi$)	
1Ø41	OUT (PORTØ),A	
1Ø42	CALL DLY	
1Ø43	INC H	
1Ø44	LD A, GRID	
1Ø45	CP H	
1Ø46	JR Z,+9	
1Ø47	INC IX	
1 Ø48	DJNZ LNEXT	
1Ø49	JP LLINE	
1Ø5Ø	DEC C	
1Ø51	JP NZ, LH	

1Ø52		EXX	
1Ø53		EX AF, AF'	
1Ø54		RET	
1Ø55	ACONS	: EQU Ø7CØH	;Acceleration constants
1Ø56	DCONS	EQU Ø7DØH	;Deceleration constants
1Ø57	YUACC	EXX	;Routine to move the detect
1Ø58		EX AF, AF	;up in y-direction by accel
1Ø59		ID IY, ACONS	;tion.
1Ø6Ø		LD C, ACOUNT	
1Ø61	YRTH	: LD H,ØØ	
1Ø62	YARTN	: LD IX, YSTEP4	
1Ø63		LD B, COUNT	
1Ø64	BMOVE	: LD A, $(IX+\emptyset\emptyset)$	
1Ø65	e e e e e	OUT (PORTØ),A	
1Ø66		LD E, (IY+ $\emptyset\emptyset$)	
1Ø67		CALL VDLY	
1Ø68		INC H	
1Ø69		ID A, GRID	
1Ø7Ø		CP H	
1Ø71		JR Z,+9	
1Ø72		DEC IX	
1Ø73		DJNZ BMOVE	
1Ø74		JP YARTN	
1Ø75		INC IY	
1Ø76		DEC C	
1Ø77		JP NZ, YRTH	
1Ø78		LD HL, PATH	
1Ø79		ID C, (HL)	
1Ø8Ø	HXAMY	: LD H,ØØ	

1Ø81	XAMY	:	LD IX, YSTEP4
1Ø82			LD B, COUNT
1Ø83	YMMY	:	ID A, $(IX+\emptyset\emptyset)$
1Ø84			OUT (PORTØ),A
1Ø85			LD E, MAXSPD
1Ø86	•		CALL VDLY
1Ø87			INC H
1Ø88			LD A, GRID
1Ø89			CP H
1Ø9Ø			JR Z,+9
1Ø91			DEC IX
1Ø92			DJNZ YAMV
1Ø93			JP YMAX
1Ø94			DEC C
1Ø95		•	JP NZ, YMAXH
1Ø96	YDEC	:	LD IY, DCONS
1Ø97			LD C, DCOUNT
1Ø98	YDRTH	:	LD H,ØØ
1 ø 99	YDRTN	:	LD IX, YSTEP4
11ØØ			LD B, COUNT
ııøı	YDMV	:	LD A, $(IX+\emptyset\emptyset)$
11Ø2			OUT (PORTØ),A
11Ø3	•		ID E, (IY+ $\phi\phi$)
11Ø4			CALL VDLY
11Ø5			INC H
11Ø6			LD A, GRID
llØ7			СР Н
11Ø8			JR Z,+9
11Ø9			DEC IX
			Programme of the control of the cont

111Ø	DJNZ YDMV
1111	JP YDRTN
1112	INC IY
1113	DEC C
1114	JP NZ, YDRTH
1115	XOR A
1116	OUT (PORTØ),A
1117	EX AF, AF'
1118	EXX
1119	RET

112Ø	MVINYU:	EXX	;Routine to move the detect
1121		EX AF, AF	;up in y-direction with
1122		LD A, (WAY)	; constant speed.
1123		LD C,A	
1124		ID H,ØØ	
1125	ULINE :	ID IX, YSTEP4	
1126		LD B, COUNT	
1127	UNEXT :	ID A, $(IX+\emptyset\emptyset)$	
1128		OUT (PORTØ),A	
1129		CALL DLY	
113ø	•	INC H	
1131		LD A, GRID	
1132		СР Н	
1133		JR Z,+9	
1134	totalis in the second	DEC IX	
1135		DJNZ UNEXT	
1136		DEC C	
1137		JP NZ, ULINE	
1138		EXX	
1139		EX AF, AF	
114ø		XOR A	
1141		OUT (PORTØ), A	
1142		RET	

1143	MVINYD : EXX	;Routine to move the	detec
1144	EX AF, A	F' ;down in y-direction	with
1145	ID A, (W	AY) ; constant speed.	
1146	LD C,A		
1147	ID H, ØØ		. •
1148	DLINE : LD IX, Y	STEPL	
1149	ID B,CO	UNT	
115ø	DNEXT : LD A, (1	X+ØØ)	
1151	OUT (PO	RTØ),A	•
1152	CALL DI	Y	
1153	INC H		
1154	LD A,GR	ID	
1155	CP H		•
1156	JR Z,+9		
1157	INC IX		
1158	DJNZ DI	YEX T	
1159	DEC C		
116ø	JP NZ,I	DLINE	
1161	EXX		
1162	EX AF,	AF'	•
1163	XOR A		
1164	OUT (PO	ORTØ),A	
1165	RET		•

1166	XRACC :	EXX	;Routine to move the detec
1167		EX AF, AF	;right in x-direction by
1168		LD IY, ACONS1	;acceleration.
1169		LD C, ACOUNT	;Acceleration starts.
117ø	XRTH:	LD H,ØØ	
1171	XARTN:	ID IX,XSTEP1	
1172		ID B, COUNT	
1173	AMOVE :	ID A, $(IX+\emptyset)$	
1174	:	OUT (PORTØ),A	
1175		LD E, (IY+Ø)	
1176		CALL VDLY	
1177		INC H	
1178		LD A, GRID	
1179		CP H	
118Ø		JR Z,+9	
1181		INC IX	
1182	•	DJNZ AMOVE	
1183		JP XARTN	
1184		INC IY	
1185		DEC C	
1186		JP NZ, XRTH	
1187	• • • • • •	LD HL, PATH	
1188		LD C, (HL)	
1189	XNMXH:	: LD H,ØØ	; Maximum speed is reached
119Ø	XNMAX:	: LD IX,XSTEP1	; the stage moves with the
1191		LD B, COUNT	;speed PATH long.
1192	XAMV:	: ID A, $(IX+\emptyset)$	
1193		OUT (PORTØ),A	

1194		LD E, MAXSPD	
1195		CALL VDLY	
1196		INC H	
1197		ID A,GRID	
1198		СР Н	
1199		JR Z,+9	
12ØØ		INC IX	
12Ø1	•	DJNZ XAMV	
12Ø2		JP XNMAX	
12Ø3		DEC C	
12Ø4		JP NZ, XNMXH	
12Ø5	XDEC :	LD IY, DCONSI	;Deceleration begins.
12Ø6		LD C, DCOUNT	
12Ø7	XDRTH :	LD H,ØØ	
12Ø8	XDRTN:	ID IX, XSTEPI	
12Ø 9		LD B, COUNT	
121Ø	XDMV:	LD A,(IX+Ø)	
1211		OUT (PORTØ),A	
1212		LD E, (IY+Ø)	
1213		CALL VDLY	
1214		INC H	
1215		LD A,GRID	
1216		CP H	
1217		JR Z,+9	
1218		INC IX	
1219		DJNZ XDHV	
122Ø		JP XDRIN	
1221		INC IY	
the state of the			•

1222		DEC C	
1223		JP NZ, XDRTH	
1224		XOR A	;Deceleration lasts, and the
1225		OUT (PORTØ),A	;x-stage stops. Then the routine
1226		EXX	;returns to where it is called.
1227		EX AF, AF'	
1228		RET	
1229	XLACC:	EXX	;Routine to move the detector
123Ø		EX AF, AF	;left in x-direction by
1231		LD IY,ACONS1	;acceleration using the same
1232		LD C, ACOUNT	;procedures described in XRACC
1233	SXPAH :	LD H,ØØ	;routine.
1234	SXPAR :	LD IX,XSTEP4	
1235		LD B, COUNT	
1236	SXPAM :	$LD A, (IX+\emptyset)$	
1237		OUT (PORTØ),A	
1238		LD E, (1Y+ $\emptyset\emptyset$)	
1239		CALL VDLY	
124Ø		INC H	
1241		ID A, GRID	
1242		CP H	
1243		JR Z,+9	
1244		DEC IX	
1245		DJNZ SXPAM	
1246		JP SXPAR	
1247		INC IY	
1248		DEC C	
1249		JP NZ, SXPAH	

•			
125Ø		٠	LD HL, PATH
1251			LD C,(HL)
1252	SXAPH	:	ID H,ØØ
1253	SXAPS	:	LD IX,XSTEP4
1254			LD B, COUNT
1255	SXAPM	:	ID A, $(IX+\emptyset)$
1256			OUT (PORTØ),A
1257			LD F, MAXSPD
1258			CALL VDLY
1259			INC H
126Ø			LD A, GRID
1261			CP H
1262			JR Z,+9
1263			DEC IX
1264			DJNZ SXAPM
1265			JP SXAPS
1266		-	DEC C
1267			JP NZ, SXAPH
1268	SXPD	:	LD IY, DCONS 1
1269			LD C, DCOUNT
127Ø	SXPDH	:	ID H,ØØ
1271	SXPDR	•	LD IX,XSTEP4
1272			LD B, COUNT
1273	SXPDM	:	$LD A, (IX+\emptyset)$
1274			OUT (PORTØ),A
1275			LD E,(IY+∅)
1276			CALL VDLY
1277			INC H

1278		LD A, GRID
1279		CP H
128Ø		JR 2,+9
1281		DEC IX
1282		DJNZ SXPDM
1283		JP SXPDR
1284		INC IY
1285		DEC C
1286		JP NZ, SXPDH
1287		EXX
1288	· · · · · · · · · · · · · · · · · · ·	EX AF, AF
1289		RET

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