INTEGRATED CMOS RECEIVER SYSTEM FOR HIGH SPEED VISIBLE LIGHT COMMUNICATION

by

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ABSTRACT

INTEGRATED CMOS RECEIVER SYSTEM FOR HIGH SPEED VISIBLE LIGHT COMMUNICATION

The speed of microprocessor has risen excessively during the last decade. The overall speed of the system is defined not only the speed of microprocessor but also the speed of the channels by which data is distributed inside the system. Using optical channel, a very high speed of data transmission and reception is aimed with the increased data rate. However Visible Light Communication System consists of main four components, which are Light Emitting Diode (LED) in the visible wavelength as transmitter, communication channel, photodiode as receiver and trans-impedance amplifier converting the current signal to voltage one, where the overall speed of the system is limited due to the low bandwidth of the LED.

In order to increase the speed of the system, the restricted bandwidth generated from a LED has to be extended which allows us to obtain higher data speed. Equalization is one of the methods used for this purpose. The circuit of this method is called Equalizer. It can be used in order to increase the bandwidth of a LED. In this thesis, firstly Trans-impedance Amplifier and Discrete Receiver System are designed and simulated with Advanced Design System (ADS) and Altium Designer using discrete elements. Then, the simulation and measurement results of these circuits are given. Secondly, Integrated CMOS Receiver System is designed and simulated with Mentor Graphics using 130 nm CMOS technology and its pre and post-layout simulation results are given.

ÖZET

YÜKSEK HIZLI GÖRÜNÜR IŞIK İLETİŞİMİ İÇİN CMOS TABANLI TÜMLEŞİK ALICI GELİŞTİRİLMESİ

Mikroişlemcilerin hızı son on yılda aşırı bir artış gösterdi. Sistemin genel hızı yalnızca mikroişlemcilerin hızını değil, aynı zamanda verilerin sistem içinde dağıtıldığı kanalların hızını da tanımlamaktadır. Optik kanal kullanarak, artan veri hızı ile çok yüksek bir veri aktarım ve alım hızı hedeflenmektedir. Ancak, Görünür Işık İletişim Sistemi, aktarıcı olarak görünür dalga boyunda ışık yayan diyot (LED), iletişim kanalı, alıcı olarak fotodiyot ve akım işaretini voltaj işaretine dönüştüren trans-empedans yükselticisi olan dört ana bileşenden oluşur ki bu sistemin genel hızı LED'un düşük bant genişiliği nedeniyle sınırlıdır.

Sistemin hızını artırmak için, LED'tan üretilen sınırlı bant genişliğinin daha yüksek veri hızı elde edebilmemiz için artırılması gerekmektedir. Denkleştirme bu amaç için kullanılan yöntemlerden biridir. Bu yöntemin devresi denkleştirici olarak adlandırılır. Denkleştirici LED'un bant genişliğini artırmak için kullanılabilir. Bu tezde öncelikle Trans-empedans Kuvvetlendiricisi ve Ayrık Alıcı Sistemi ayrık elemanlar kullanılarak Advanced Design System (ADS) ve Altium Designer ile tasarlanmış ve simülasyonları gerçekleştirilmiştir. Daha sonra bu devrelerin simülasyon ve ölçüm sonuçları verilmiştir. İkinci olarak, CMOS tabanlı tümleşik alıcı sistemi 130 nm CMOS teknolojisi kullanılarak Mentor Graphics ile tasarlanmış ve simülasyonu gerçekleştirilmiştir. Daha sonra yerleşim öncesi ve sonrası simülasyon sonuçları verilmiştir.

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LIST OF SYMBOLS

T	Absolute Temperature
C_a	Amplifier Input Capacitance
ω_N	Angular Frequency
V_A	Applied Voltage
BW	Bandwidth
Δ_f	Bandwidth of Measurement of Noise
I_B	Biasing Current
k_B	Boltzmann Constant
q	Charge of Electron
A_{cs}	Common Source Voltage Gain
E_c	Conduction Energy
D	Damping Factor
I_D	Dark Current of Photodiode
$GAIN$	DC Trans-impedance Gain
W_d	Depleted Region Width
ε_{si}	Dielectric Constant
A	Diffused Area of Junction
DC_{GAIN}	Direct Current Gain
f_{dp}	Dominant Pole
ω_{P1}	Dominant Pole
v	Electromagnetic Wave Frequency
μ	Electron Mobility
C_f	Feedback Capacitance
R_f	Feedback Resistance
R_{fb}	Feedback Resistor
C_{fb}	Feedback Capacitor
n	Finger Number
GBP	Gain Bandwidth Product

tg	Group Delay
HF_{GAIN}	High Frequency Gain
I_{in}	Ideal Current Source
n	Ideality Factor
$I_{PEAKING}$	Ideal Peaking
P	Incoming Power of Light
C_{in}	Input Capacitance
V_{in}	Input Voltage
Z_{in}	Input Resistance of the RGC Circuit
C_j	Junction Capacitance
C_L	Load Capacitance
$A_T(0)$	Low-frequency Trans-impedance Gain
R_{in}	Low Input Impedance
$\|G(\omega)\|$	Magnitude of Transfer Function
P_{GAIN}	Maximum Gain
m	Multiplier Number
Ω	Ohm
A_0	Open Loop Gain of Amplifier
C_{out}	Output Capacitance
C_{pd}	Parasitic Capacitance
ε_0	Permittivity of Free Space
I_P	Photocurrent
C_{pd}	Photodiode Junction Capacitor
R_{pd}	Photodiode Resistor
h	Planck's Constant
ω_p	Pole
$p - sub$	P-substrate
RC	Resistance of Contact
R_o	Resistivity of Silicon
R_λ	Responsivity
I_{SAT}	Reverse Saturation Current

ω_{P2}	Second Pole
R_s	Series Resistance
I_{sn}	Shot Noise
R_{sh}	Shunt Resistance
V_{bi}	Silicon Built-in Voltage
R_o	Substrate Resistivity
W_s	Substrate Thickness
ω_{P3}	Third Pole
gm	Transconductance
$H(s)$	Transfer Function
$\|Z(TIA)\|$	Trans-impedance Factor
$ZTIA$	Trans-impedance Gain
R_D	Trans-impedance Gain
A_T	Trans-impedance Gain
E_v	Valence Energy Band
λ	Wavelength in nm
ω_z	Zero

LIST OF ACRONYMS/ABBREVIATIONS

ADS	Advanced Design System
AC	Alternating Current
A	Amper
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
cm	Centimeter
CDR	Clock and Data Recovery Circuit
CG	Common Gate
CG-TIA	Common Gate TIA
CS	Common Source
CMOS	Complementary Metal Oxide Semiconductor
CTLE	Continuous Time Linear Equalizer
C	Coulomb
dB	Decibel
dB ohm	Decibell ohm
dBm	Decibels Relative to One Milliwatt
DPPM	Differential Pulse Position Modulation
DC	Direct Current
DMT	Discrete Multi Tone
DFE	Dynamic Filter Efficiency
F	Farad
FIR	Finite Impulse Response
GaN	Gallium Nitride
GSSK	Generalized Space Shift Keying
Gbps	Gigabit per Second
Gbit/s	Gigabit/Second
GHz	Gigahertz
IEEE	Institute of Electrical and Electronics Engineers
IC	Integrated Circuit

J	Joule
K	Kelvin
K	Kilo
kbit/s	Kilobit per Second
kHz	Kilohertz
kohm	Kiloohm
LMSC	LAN MAN Standards Committee
LED	Light Emitting Diode
LA	Limiting Amplifier
Mag	Magnitude
Mbps	Megabit per Second
Mb/s	Megabit per Second
MHz	Megahertz
Mohm	Megaohm
m	Meter
μA	Microampere
μF	Microfarad
μm	Micrometer
mV	Milivolt
mW	Miliwatt
nF	Nanofarad
nm	Nanometer
OOK	On-off Keying
OLED	Organic Light-Emitting Diode
P	Pico
pF	Picofarad
PDM	Polarization Division Multiplexing
PCB	Printed Circuit Board
RX	Receiver
RGB	Red Green Blue
RGC	Regulated-Cascode

RC	Resistor-Capacitor
SMA	SubMiniature Version A
SMD	Surface Mount Device
TIA	Trans-impedance Amplifier
TX	Transmitter
UMC	United Microelectronics Corporation
VLC	Visible Light Communication
V	Volt
WDM	Wavelength Division Multiplexing
WiFi	Wireless Fidelity

1. INTRODUCTION

In this chapter, general information is given related to optical communication, differences between Fully integrated and Discrete Receiver System and how to increase the limited bandwidth of a LED.

1.1. Principles of Optical Communication

The speed of microprocessor has risen excessively during the last decade. The overall speed of the system is defined not only the speed of microprocessor but also the speed of the channels by which data is distributed inside the system. In order to perform a very high speed of data transmission and reception, optical channel has been utilized to have the increased data rate. At the transmitter side a Light Emitting Diode (LED) in the visible wavelength is used and at the receiver side a photodiode is utilized. Data is transmitted and received as light signal inside of an optical cable. This light signal is converted into electrical signal at the receiver side. Figure 1.1 shows an optical communication system [1].

Figure 1.1. Optical Communication System [1].

Optical receivers are utilized in order to detect light coming from the transmitter side through communication medium. Figure 1.2 shows the main four components of a typical optical receiver. An electrical current signal is created by converting the optical signal by a photodiode. Current signal is amplified and converted into a voltage signal by a trans-impedance amplifier following the photodiode. Clock and data recovery circuit (CDR) which follows the post amplifier is utilized in order to extract the carrier and data signal using the received signal [1].

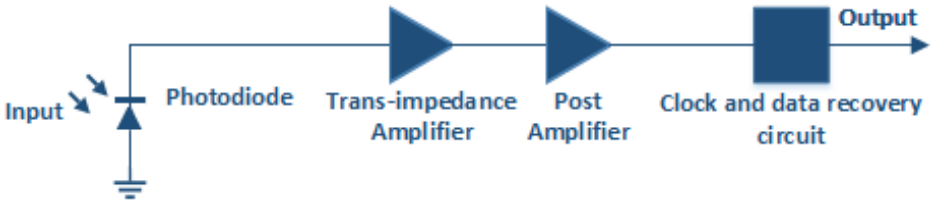


Figure 1.2. Architecture of a typical optical receiver [1].

1.2. Comparison of Fully Integrated and Discrete Optical Receiver

In a fully integrated optical receiver main components mentioned above are integrated on the same substrate. This has some advantages over the discrete optical receiver. When a CMOS photodetector is utilized on the same substrate as a receiver circuit, integration of high level is achived which profits in the economy for optical communication in short distance [9]. Secondly, this compact and low cost receiver solution enables signal integrity on the receiver chip. Thirdly, losses related to hybrid implementation of the photodetector and trans-impedance amplifier are eliminated. [10].

In terms of integrated circuit technology realization, CMOS is a low-cost process. However, the photodetectors created using CMOS process give lesser bandwidth than the ones in which discrete components are utilized. Therefore, it is a difficult task to use a CMOS process to create an integrated optical photodetectors. When a LED is used, bandwidth of an electrical signal obtained from a LED is in the range of a few MHz. However, optical fiber can handle a bandwidth which is in GHz range for a channel. This shows that electrical bandwidth of a LED limits the data rate which can be accessed. The higher the bandwidth is, the higher data speed and bandwidth can be used in the communication link [11].

1.3. How to Extend the Bandwidth of the Visible Light Communication (VLC) System?

In order to utilize advantages of CMOS technology, the restricted bandwidth generated from a LED has to be compensated by a proper design. Equalization is one of the methods used to overcome the limitation of bandwidth of LED. The circuit used in this method is called Equalizer. It can be used in order to extend the bandwidth of a communication channel. From the signals and system theory, it is known that convolution in time domain corresponds to addition in frequency domain. Hence, when the responses obtained from the LED and the equalizer circuits are convolved in time domain, a high bandwidth can be obtained from this process, as can be seen in Figure 1.3 [1], [2].

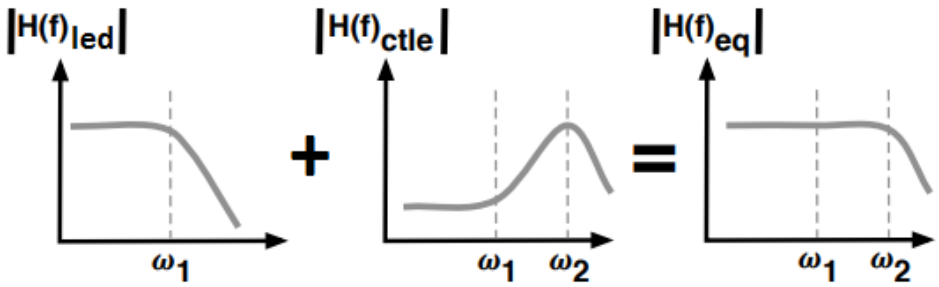


Figure 1.3. Equalization [2].

1.4. Literature Review

The systems in which lighting and wireless communication are performed simultaneously are called optical (wireless) visible light communication (VLC) systems, in which the electrical signal that drives the visible light LED device is modulated and collected by a photodiode on the receiving side [12], [13], [14], [15]. Smart home applications of VLC technology and inter-vechicle communication are presented [16]. Two separate studies on VLC are currently carried out by IEEE 802 LMSC. 802.11 WiFi group prepares the project approval request. When it is accepted, a WiFi-based VLC standard will be prepared [17]. 802.15 group prepared group usage areas and channel modelling in 2014 with a standard [18]. There is a commercially available VLC product

and has been implemented using discrete components [19]. Qian et al. reported that 400 MHz bandwidth and 512 Mbit/s capacity were obtained and it was shown that visible light communication can be done by on-off keying (OOK) method [20]. Fahs et al. reported that a capacity of 150 Mbit/s was obtained from a 6-meter distance using the photodiode compatible with CMOS electronic technology as receiver [21]. Ref. [22] introduced a fully differential transimpedance amplifier with integrated differential photodetector implemented using 0.35 μm standard CMOS process, where it was demonstrated a 3 dB bandwidth of 1.1 GHz and a bitrate of 1.6 Gbit/s respectively. The power dissipation of 100 mW (for the 50 Ω output buffer), and a trans-impedance gain of 98.75 dBΩ were reported in that study. In Ref. [23] trans-impedance amplifier (TIA) and limiting amplifier (LA) were designed using 0.18 μm CMOS technology. The fully integrated optical receiver in this study has a conversion gain of 87 dBΩ, a 3 dB bandwidth of 7.6 GHz and a chip size of 1028 μm x 1796 μm with a power dissipation of 210 mW and measured sensitivity of -12 dBm. Atef et al. presented an optical receiver chip. This chip was designed using 0.6 μm BiCMOS technology and has power consumption of 112 mW and area of 1.33 mm^2 with supply voltage of 3.3 V [24]. Yasotharan et al. reported that an optical receiver was designed using 0.13 μm CMOS technology. This receiver whose area is equal to 0.23 mm^2 has gain of 85 dBΩ, data rate of 5 Gbps with power dissipation of 35.3 mW and sensitivity of -10 dBm [25]. Taghavi et al. presented an optical receiver as a chip in which 65 nm CMOS technology was used. Its trans-impedance gain and 3 dB bandwidth are equal to 77.7 dBΩ and 12 GHz respectively. In addition, photodiode responsivity and simulated sensitivity of this optical receiver are equal to 0.8 A/W and -12 dBm respectively [26]. Tanabe et al. introduced a single-chip. It was realized using 0.15 μm gate bulk CMOS. Power consumption of 104 mW was obtained. In addition, a low-cross-talk sensitive preamplifier circuit was integrated into with this receiver chip [27].

As obvious from the aforementioned discussion, due to the low bandwidth of the LED devices, there is a data-rate limitation of optical wireless VLC methods. The frequency band of the visible LED light sources is optimized for illumination. Therefore, the bandwidth is limited to a few MHz. Li et al. reported that by using simple modulation techniques such as on-off keying/on-off keying-OOK, data could be transmitted

with a few Mbps [28], [29]. In addition to the channels created by each of the RGB LED devices using WDM, Wang et al. showed a capacity of 1 Gbit/s was achieved utilizing Polarization Division Multiplexing-PDM in the receiver part [30]. Popoola et al. reported that a capacity of 40 Mbit/s was achieved using Generalized Space Shift Keying-GSSK [31]. In addition to the works related to increasing the modulation frequency, Liu et al. and Suh et al. showed that receiver system designs had been made by simultaneously changing the brightness of the LED sources [32], [33]. Again, in order to reduce the distortion caused by the non-linear current/voltage connection of micro-LED devices, Qian et al. added post-distortion to the signal collected in the photodetector [34]. Mossad et al. and Jiang et al. reported that another method used to increase the modulation bandwidth was equalization. In this method, the bandwidth of the total response of the light source (LED), the transmission medium and the receiver (photodetector) channel response, which are defined as components of the communication system, is increased [35], [36]. Equalization circuits typically consist of amplifiers and electronic (active) filter circuits. In the literature, using a post equalizer realized by electronic blocks whose power gain can be changed with OOK, it shown that 40 Mbit/s in 2008 [15], 100 Mbit/s in 2009 [37], 340 Mbit/s in 2014 [38], using multitone modulation with pre equalizer 1 Gbit/s in 2012 [39] are achieved. Ref. [5] describes the design of an analog equalizer which compensates for the limited bandwidth of n-well/p-sub photodiode. This is a theoretical study in which it is reported that the bandwidth of the optical receiver is extended to 1 GHz from 6 MHz [5]. Gimeno et al. presented a CMOS equalizer for short-reach optical communications with tuning range between 300 MHz and 3.6 GHz. 0.18 μm CMOS process was used for the prototype [40]. Bandyopadhyay et al. introduced an integrated TIA-Equalizer for a low cost Giga-Bit optical communication system. The overall bandwidth was extended from 400 MHz to about 2 GHz [41]. Radovanovic et al. presented an analog equalizer to compensate the frequency characteristics of a photodiode from DC to 1 GHz [42]. Choi et al. introduced a high speed CMOS adaptive cable equalizer. It was designed using 0.18 μm four-metal mixed-mode CMOS technology and has data rate of 3.5 Gb/s (over a 15-m RG-58 coaxial cable), and 5 Gb/s (manual adjustment mode). Its power dissipation and active area are equal to 80 mW and 0.48 x 0.73 mm^2 respectively [43].

Villanueva realized 30 GHz Adaptive Receiver Equalization Design using 28 nm CMOS technology [44].

Yang et al. designed a front-end amplifier using AMI 0.5 μm CMOS process which consists of transimpedance amplifier and limiter amplifier where it was reported that a data rate of 535 Mb/s was achieved for the front-end amplifier with simulated and measured output swing of 4.2 V and 4.1 V respectively [45]. Bespalko et al. designed 2.5 Gbps and 10 Gbps trans-impedance amplifier. They were manufactured using 0.18 μm CMOS technology. While the 2.5 Gbps trans-impedance amplifier has trans-impedance gain of 64 dBΩ, bandwidth of 1.8 GHz with power dissipation of 115 mW, the 10 Gbps trans-impedance amplifier has trans-impedance gain of 45 dBΩ, bandwidth of 12 GHz with power dissipation of 100 mW [46]. Chen et al. reported that a TIA with a 3-dB bandwidth of approximately 100 MHz was produced using 0.18 micron CMOS technology for VLC. It was mentioned that channel capacity to 150 Mbit/s could be obtained [47].

The LED light used for lighting in the smart home application can also be used in functions such as the use of household appliances, local internet connection, visual material transfer and online shopping. Communication via traffic lights, street lights and LED headlamps in vehicles is the another application of VLC technology [48]. Discrete Multi Tone-DMT realization has achieved a capacity of 513 Mbit/s [49] and 1.5 Gbit/s [50] over a single channel using RGB LED devices. In the literature, fast, energy efficient, cheap light source alternatives which can be utilized for VLC exist. GaN material is one of the candidate that semiconductor families utilized for LED device implementation. By using it, a LED device has been implemented [51]. Zhang et al. reported that a channel capacity of 1.68 Gbit/s was achived using the receiver/transmitter pair with a distance of 3 cm between them. Using the same material, the source array, which was created by the implementation of the LED emitting blue light, was hybridly integrated with a CMOS electronic integrated circuit. Thus, a capacity of 1.5 Gbit/s was achived with 16 separate parallel ports [52]. Ref. [53] introduced a LED implementation where GaN technology was used, it was possible to obtain light at wavelengths such as 370, 405, 450 and 520 nm from different sized sources in

sequence. Light sources realized by organic materials offer cost effective solutions in application areas such as portable electronic devices, smart phones, televisions and information screens [54]. In Ref. [55], with channel matching method, OLED source whose bandwidth is equal to 93 kHz was used as a transmitter with a Silicon photodetector which had a bandwidth of 5 MHz and a gain of 10 dB. 2.7 Mbit/s capacity is achieved. Without channel matching method, Haigh et al. showed that communication with a capacity of 550 kbit/s was possible [56]. Thai et al. obtained capacity of 138 kbit/s using OLED device with differential pulse position modulation-DPPM. [57].

1.5. Aim and Contribution of the Thesis

The work reported in this thesis is a part of a TÜBİTAK (the Scientific and Technological Research Council of Turkey) project under the project number 117E058 carried out at the Department of Electrical and Electronics Engineering at Boğaziçi University. The main aim of this project is to design an Integrated CMOS Receiver System for high speed visible light communication.

In this thesis, architectures of both Discrete and Integrated CMOS Receiver Systems are investigated. The main purpose of this study is to increase the bandwidth of a LED using passive and active equalizer (active CTLE) circuits and design Discrete and Integrated CMOS Receiver System.

1.6. Organization of the Thesis

In Chapter 1, general information and corresponding literature study are given related to optical communication, differences between Fully Integrated CMOS and Discrete Receiver System and how to increase the limited bandwidth of a LED.

In Chapter 2, theories of the basic blocks of the optical receiver are given in detail. Firstly, main characteristics of a photodiode namely electrical, optical, current-voltage, noise and biasing are presented. Secondly, the most important specifications of a TIA are discussed. The most common TIA topologies namely open loop and closed loop

are studied. Thirdly, theories of two equalizer circuits are explained. The first one is passive CTLE which is constructed using only passive electronic components such as resistors, capacitors. The second one is active CTLE which is created using active (transistors) and passive elements (resistors and capacitors).

Design considerations of the PCBs of TIA and Discrete Receiver System with simulation and measurement results are presented in Chapter 3.

Chapter 4 explains design considerations of Integrated CMOS Receiver System which consists of three main blocks (photodiode, trans-impedance amplifier and equalizer. In this Chapter pre-layout and post-layout simulation results are given as well.

In Chapter 5 conclusion is made with future work.

2. THEORY

Theories of photodiode, trans-impedance amplifier and equalizer are presented in this chapter.

2.1. Photodiode

Silicon photodiodes are semiconductor optoelectronic devices. Photons are absorbed by the semiconductor to create a flow of electrical current in the external circuit proportional to incoming optical power. The optical energy, $h\nu$, must be larger than the energy band gap to generate electron-hole pairs

$$h\nu \geq E_g = E_c - E_\nu \tag{2.1}$$

where h represents Planck's constant, ν stands for the electromagnetic wave frequency, E_c conduction energy (the lowest energy level of the conduction band) and E_ν is the valence energy band (the highest energy level of the valence band). Energy diagram is shown Figure 2.1 [1].

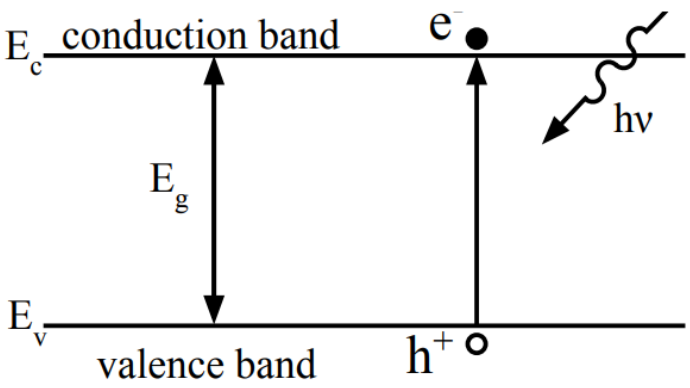


Figure 2.1. Energy diagram [1].

A diode is a semiconductor device. It is n-type doped on one side and p-type doped on the other side. There are a lot of free electrons in n-type region called cathode.

There are a lot of holes in p-type region called anode. In equilibrium state, depletion region is formed in the junction. This region does not have carriers. A pn junction is shown in Figure 2.2.

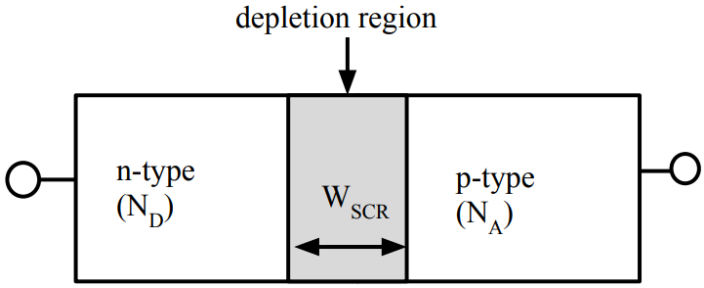


Figure 2.2. PN junction [1].

The width of depletion region is given as

$$W_{SCR} = \sqrt{\frac{2\varepsilon \times (N_A + N_D)V_{bi}}{qN_AN_D}} \tag{2.2}$$

where W_{SCR} stands for the width of depletion region, N_D and N_A represents the doping concentration in n-type and p-type region respectively, V_{bi} is the built-in voltage at the junction and ε is the permittivity of the semiconductor material utilized. If photons with sufficient energy impinge on a semiconductor diode, electronhole pairs are formed in the depletion region, in the n-type region and in the p-type region. The electron and the holes are separated from each other by the electric field within the depletion region. Hence, generation of a photocurrent, which flows between the anode and cathode of the diode, occurs. Hereby, a photodiode is created [1].

2.1.1. Electrical Characteristics

A current source in parallel with an ideal diode creates a silicon photodiode. Current source represents the current generated by incident radiation. Diode stands for p-n junction. One of the most important components is a junction capacitance C_j which is connected in parallel with the other remain components. A shunt resistance R_{ph} is also connected in parallel with the other elements. Series resistance R_s is in

series with all components. A photodiode model is shown in Figure 2.3 below [3].

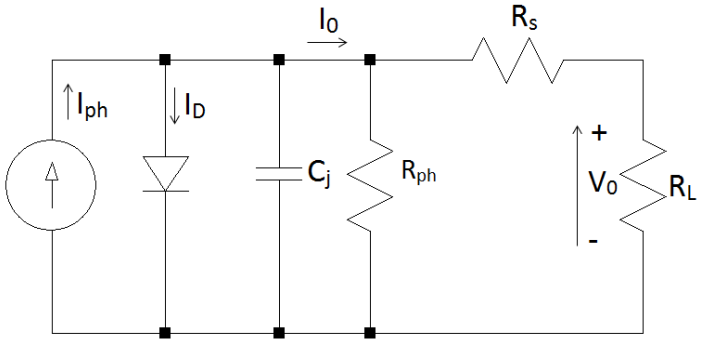


Figure 2.3. Equivalent circuit for a silicon photodiode [3].

The components of the model are described below:

Junction Capacitance (C_j): While the junction capacitance is directly proportional to the diffused area, the capacitance is inversely proportional to the depletion depth. Furthermore, the capacitance is inversely proportional to the reverse bias voltage. When substrate resistivity rises, junction capacitance drops. Junction capacitance and depletion depth are shown as below

$$C_j = A\sqrt{\frac{q\varepsilon_{si}\varepsilon_0 N_A N_D}{2(V_{bi}+V_A)(N_A+N_D)}} \tag{2.3}$$

where A is the photodiode are, $\varepsilon_{si} = 11.9$ is the dielectric constant of silicon, $\varepsilon_0 = 8.854 \times 10^{-14}$ F/cm is the permittivity of free space, V_A is the applied voltage, V_{bi} is the silicon built-in voltage and N_D and N_A represents the doping concentration in n-type and p-type region respectively [3].

Shunt resistance (R_{ph}): The slope of the current-voltage curve of the photodiode at the origin determines the shunt resistance. The value of a shunt resistance in an ideal photodiode is between 10 and 10^4 MΩ. Shunt resistance is depended on noise current. Therefore, it is used in order to find the noise current in photovoltaic mode (when no bias is applied).

Cross-sectional of a Planar diffused silicon photodiode is shown in Figure 2.4 below [3].

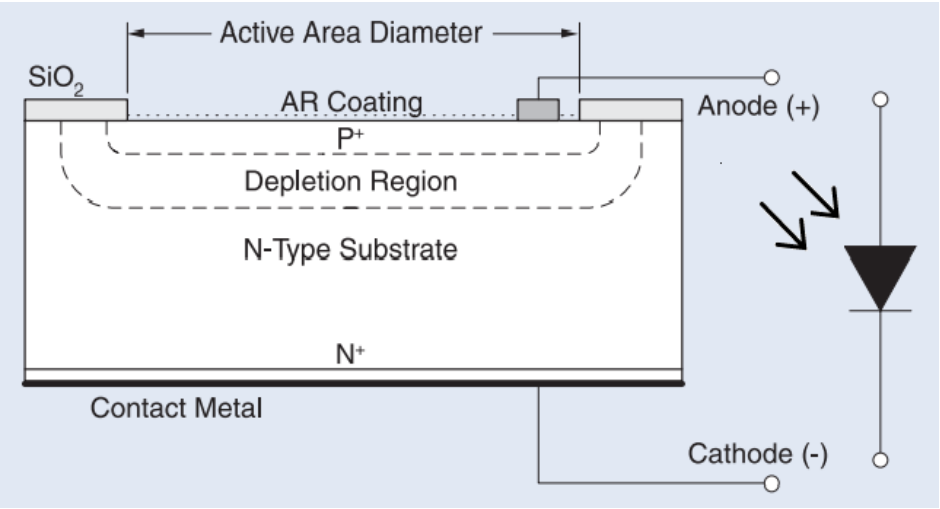


Figure 2.4. Planar diffused silicon photodiode [3].

Formulation of a shunt resistance is expressed as

$$R_{ph} = \frac{(W_s - W_d)\rho}{A} + R_C \tag{2.4}$$

where W_s is the substrate thickness, W_d is the depleted region width, ρ is the substrate resistivity, A is the diffused area of junction and R_C is the resistance of contact. Shunt resistance value is between 10 and 10^3 Ω [3].

2.1.2. Optical Characteristics

Responsivity (R_λ): It determines efficiency of electrical current induction due to incident optical power on a photodiode. The responsivity formulation is found as below

$$R_\lambda = \frac{I_P}{P} \tag{2.5}$$

where I_P represents the photocurrent and P is the incoming power of light at a given wavelength [58].

Quantum Efficiency ($Q.E.$): It is the fraction of the photon flux which contributes to photocurrent in a photodiode. It is given by the following formula

$$Q.E = R_\lambda \frac{hc}{\lambda q} \tag{2.6}$$

$$= 1240 \frac{R_\lambda}{\lambda} \tag{2.7}$$

where $h = 6.63 \times 10^{-34}$ J-s is the Planck constant, $c = 3 \times 10^8$ m/s is the speed of light, $q = 1.6 \times 10^{-19}$ C is the charge of electron, λ is the wavelength in nm and R_λ is the responsivity in A/W [58].

2.1.3. Current-Voltage Characteristics

When there is no incident light, the photodiode current-voltage characteristic is similar to a rectifier diode. When a photodiode is connected in forward bias, an exponential rise in the current occurs. When the photodiode is connected in reverse biased, a small reverse current arises. Current-Voltage relationship is given as

$$I_D = I_{SAT}(e^{\frac{qV_A}{nk_BT}} - 1) \tag{2.8}$$

where I_D stands for the diode current of the photodiode, I_{SAT} represents the reverse saturation current, $q = 1.6 \times 10^{-19}$ C is the electron charge, V_A is the applied voltage, n is the ideality factor, $k_B = 1.38 \times 10^{-23}$ J/K is the Boltzmann Constant and T represents the absolute temperature. When the photodiode is illuminated with an optical radiation, total current can be found as below

$$I_{TOTAL} = I_{SAT}(e^{\frac{qV_A}{nk_BT}}) - I_P \tag{2.9}$$

where I_P (defined in Equation 2.5) is the photocurrent, I_{SAT} is the reverse saturation current [58].

2.1.4. Noise

In a photodiode, there are two noise sources namely Shot noise (I_{sn}) and Johnson noise (I_{jn}). The total noise current is found as below

$$\overline{I_{tn}{}^2} = \overline{I_{sn}^2} + \overline{I_{jn}^2} \tag{2.10}$$

Shot Noise (I_{sn}): It is dependent on both the dark current and the photocurrent. The shot noise magnitude is given as

$$\overline{I_{sn}{}^2} = 2q(I_P + I_D)\Delta f \tag{2.11}$$

where $q = 1.6 \times 10^{-19}$ C is the charge of electron, I_P is the photocurrent, I_D is the dark current of the photodetector and Δf is the bandwidth of the measurement of noise [59].

Johnson Noise (Thermal Noise, I_{jn}): Because of the thermal fluctuations of carriers, there is a Johnson noise associated with the shunt resistance. The magnitude of Johnson noise is given by the following equation

$$\overline{I_{jn}{}^2} = \frac{4k_B T \Delta f}{R_{ph}} \tag{2.12}$$

where $k_B = 1.38 \times 10^{-23}$ J/K is the Boltzmann Constant, T is the absolute temperature, Δf is the bandwidth of the noise measurement and R_{ph} is the photodiode shunt resistance [59].

2.1.5. Biasing

There is a direct proportion between the photocurrent and incident light power. When it is necessary to use voltage as the signal to be processed, a conversion of the photocurrent to voltage is performed using a trans-impedance amplifier. Depending on

the requirements of the application, a reverse bias may or may not be applied to the photodiode. There are three main modes of operations for the photodiode listed as [4]:

Photovoltaic Mode: For the low frequency and low light level applications unbiased photodiode is desired. A circuit for photovoltaic operation can be seen in Figure 2.5. As can be seen from Figure 2.5 the photodiode receives optical power and open circuit voltage (V_{oc}) is measured.

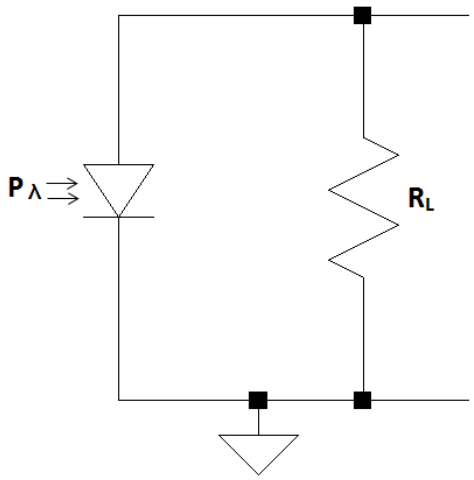


Figure 2.5. Circuit for photovoltaic operation [4].

Zero Bias Mode: There are two important properties of this mode which are linearity and low noise. A circuit for zero bias operation can be seen in Figure 2.6.

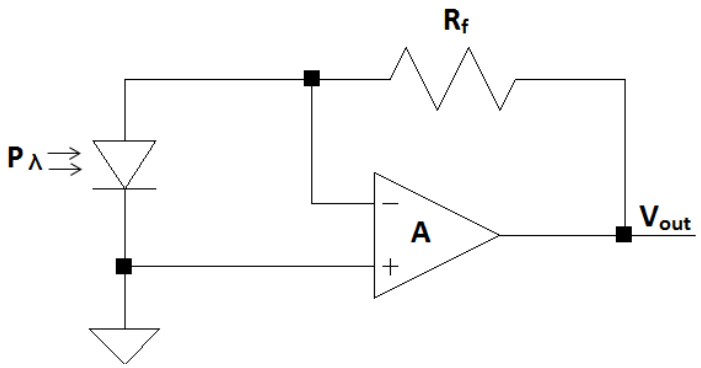


Figure 2.6. Circuit for zero bias operation [4]

Photoconductive Mode: When the photodiode is connected in reverse bias, while cathode becomes positive, anode becomes negative. This improves the response speed and device linearity. The reason of this is that width of depletion region increases and junction capacitance decreases. The dark and noise currents are increased by reverse biasing. A circuit for photoconductive operation can be seen in Figure 2.7.

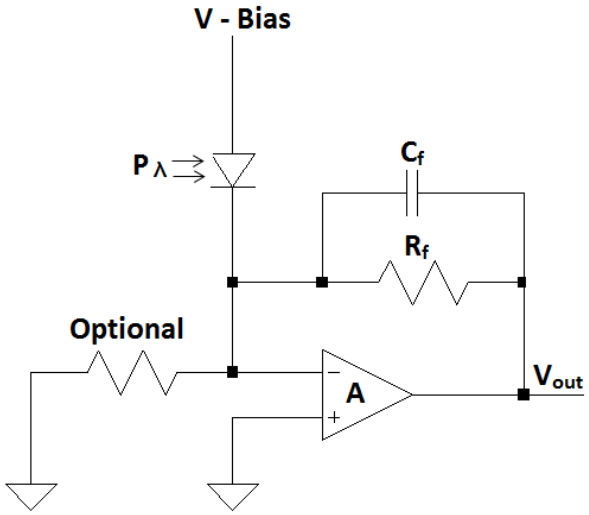


Figure 2.7. Circuit for photoconductive operation [4]

Figure 2.8 shows the effect of load resistance on the current/voltage characteristics.

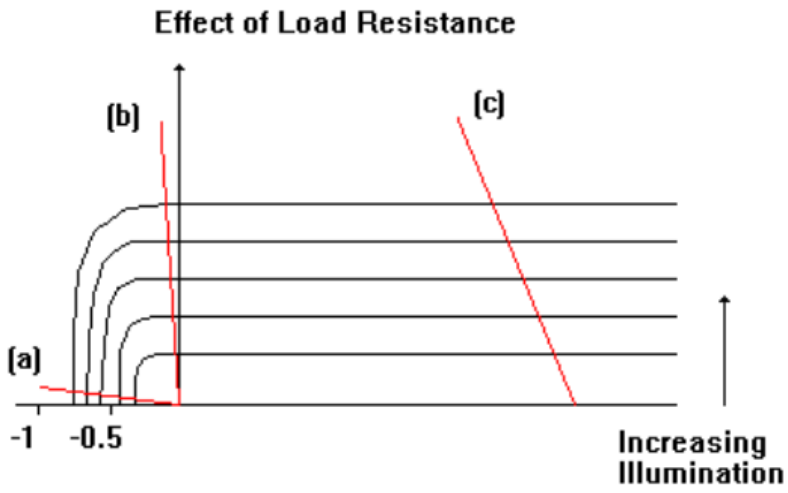


Figure 2.8. Load resistance effect on current/voltage characteristics [4].

In Figure 2.8, (a) is the photovoltaic operation where load resistance ≫ shunt resistance. (b) represents the zero bias operation in which shunt resistance ≫ load resistance. In addition, (c) belongs to photoconductive operation.

2.2. Trans-impedance Amplifier (TIA)

The signal coming to the receiver is attenuated by a number of factors. The current generated by the photo-detector must be amplified in order to be used in other operations. For this purpose, trans-impedance amplifier is used in optical receivers.

There are important points to consider while designing a trans-impedance amplifier. They are trans-impedance gain, bandwidth, input capacitance and input referred noise current [60].

Trans-impedance gain is equal to the output voltage of the amplifier divided by the input current [60]. It is expressed as follows

$$Z_{TIA} = \frac{v_{out}}{i_{in}} \tag{2.13}$$

Figure 2.9 shows the block diagram of the trans-impedance amplifier where input is driven by a current source and output voltage is obtained.

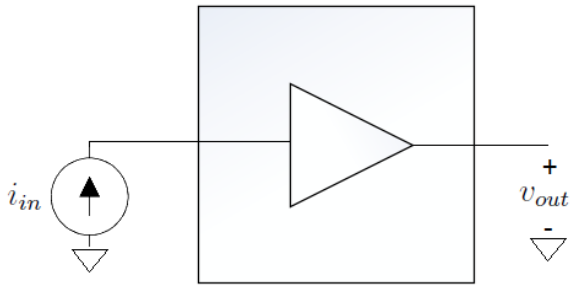


Figure 2.9. Trans-impedance amplifier.

Bandwidth is the upper frequency in which the gain falls 3-dB below its mid-band value. It is mainly determined by photodiode junction capacitance C_j, feedback capacitance C_f, amplifier input capacitance C_a, feedback resistance R_f and gain bandwidth product of the amplifier (GBP). There is a trade off between the gain and the bandwidth due to fact that GBP is equal to gain multiplied by bandwidth. The 3-dB frequency of the trans-impedance amplifier is given as [61]

$$f_{3dB} = \sqrt{\frac{GBP}{2\pi R_f(C_j + C_f + C_a)}} \tag{2.14}$$

The sensitivity of the receiver is determined by input-referred noise current (Figure 2.10). Its definition is that the noise current which can be added to the equivalent noiseless trans-impedance gain in order to produce an equal output noise voltage to that of the original noisy circuit. It can be expressed as follow

$$\overline{|i_{n,in}|^2} = \frac{\overline{|v_{n,out}|^2}}{\overline{|Z_{TIA}|^2}} \tag{2.15}$$

where Z_{TIA} is the trans-impedance gain and $v_{n,out}$ is the output voltage [62].

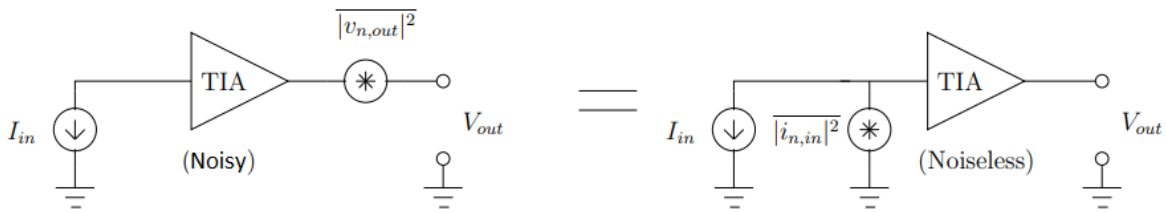


Figure 2.10. Input referred noise current.

Various TIA topologies are presented in this chapter.

2.2.1. Open Loop Topologies

2.2.1.1. Single Resistor Trans-impedance. Figure 2.11 shows the most basic trans-impedance converting a current into a voltage. It is accomplished by using a resistor

R_L on which a current passes through. In Figure 2.11 I_{in} is an ideal current source, C_{pd} represents a parasitic capacitance and C_L stands for load capacitance.

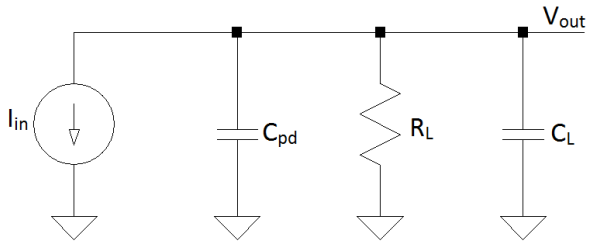


Figure 2.11. Single resistor trans-impedance circuitry in which photodiode model is used [5].

The trans-impedance of the single resistor TIA can be expressed as follows

$$Z_{TIA} = \frac{R_L}{1 + j2\pi f R_L(C_{pd} + C_L)} \tag{2.16}$$

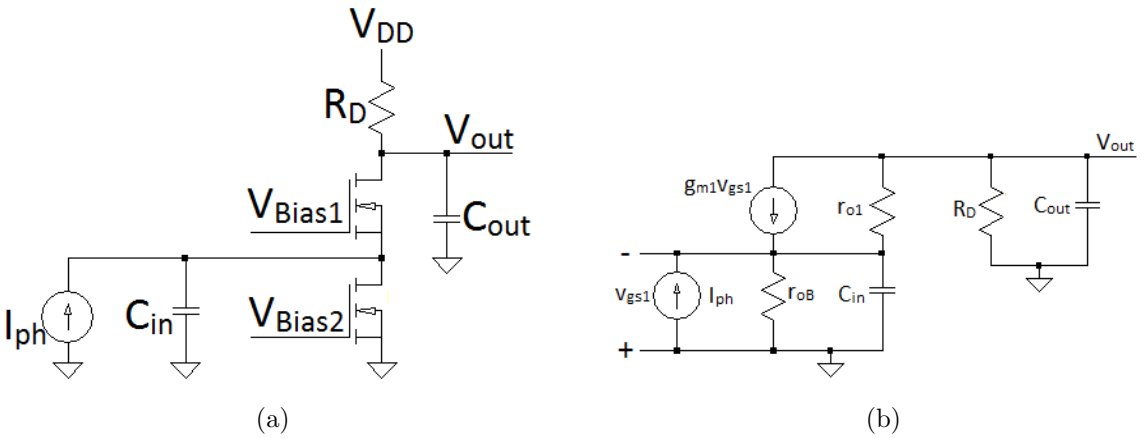
The trans-impedance factor and the 3-dB bandwidth are defined as

$$|Z(T_{IA})| = R_L \tag{2.17}$$

$$f_{TIA} = \frac{1}{2\pi f R_L(C_{pd} + C_L)} \tag{2.18}$$

The disadvantage of the single resistor converter is that in order to increase the bandwidth it is necessary to decrease the R_L. However, doing that decreases the trans-impedance gain [5].

2.2.1.2. Common Gate TIA. Figure 2.12 (a) and (b) show the common-gate circuitry and its small-signal model of the stage respectively.



(a) (b)

Figure 2.12. (a) CG-TIA circuitry, (b) Small-signal model of CG-TIA [5], [6].

A common-gate TIA has low input impedance defined as follows

$$R_{in} = \frac{r_{o1} + R_D}{1 + g_{m1} r_{o1}} // r_{oB} \tag{2.19}$$

$$\approx \frac{r_{o1} + R_D}{g_{m1} r_{o1}} \tag{2.20}$$

$$= \frac{1}{g_{m1}} + \frac{R_D}{A_{v1}} \tag{2.21}$$

where $A_{v1} = g_{m1} r_{o1}$ is the intrinsic gain of the transistor M1. As a result of this, when the trans-impedance gain (R_D) increases, the input impedance rises which decrease the bandwidth of TIA.

The low-frequency trans-impedance gain of the structure given in Figure 2.12 can be expressed as

$$A_T(0) = R_D \tag{2.22}$$

Taking into consideration the effect of input capacitance and output capacitance, the frequency dependent trans-impedance gain is given as follows

$$A_T = \frac{R_D}{(1 + (\frac{1}{g_{m1}})C_{in}s)(1 + R_D C_{out}s)} \tag{2.23}$$

Assuming a properly scaled M1 transistor, $g_{m1} > \frac{1}{R_D}$ therefore $\frac{C_{in}}{g_{m1}} > \frac{C_{out}}{R_D}$, and the dominant pole can be given as

$$f_{dp} = \frac{g_{m1}}{2\pi C_{in}} \tag{2.24}$$

This dominant pole described above determines the bandwidth of CG TIA.

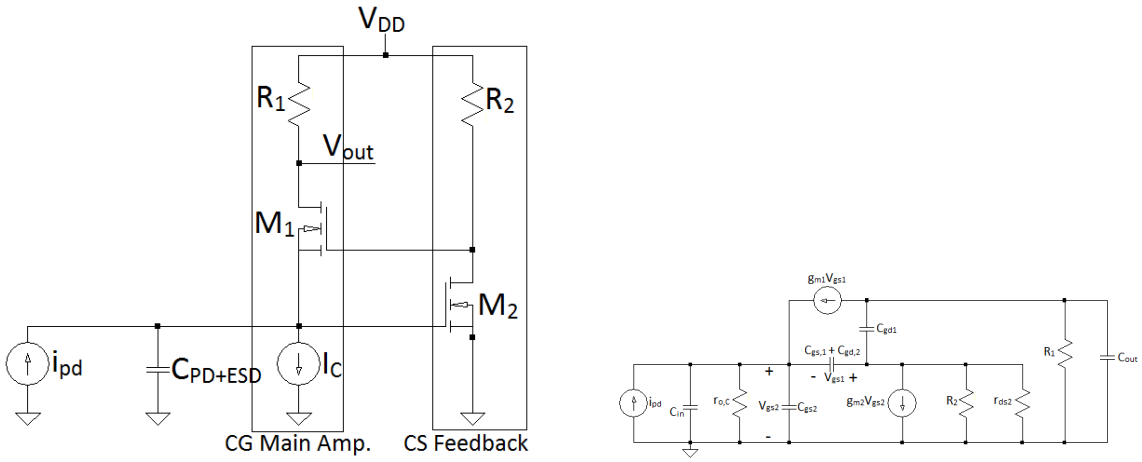
As can be seen from Equation 2.24 when the g_{m1} is increased which can be possible by selecting a proper biasing current I_B and large width to length ratio for M_1, a low impedance can be obtained. Hereby a maximum bandwidth can be achieved [5].

2.2.2. Closed Loop Topologies

2.2.2.1. Regulated-Cascode TIA. Figure 2.13 (a) and (b) show a mos based regulated cascode circuitry and its small-signal model respectively.

Examining the small-signal analysis, the input resistance of the RGC circuit is expressed as follows

$$Z_{in} = \frac{1}{g_{m1}(g_{m2}R_2 + 1)} = \frac{1}{g_{m1}(A_{cs} + 1)} \tag{2.25}$$



(a) (b)

Figure 2.13. (a) Regulated cascode TIA circuitry, (b) Small-signal model of regulated cascode TIA [5].

where A_{cs} is the voltage gain of the common source stage defined by

$$A_{cs} = g_{m2}(R_2//r_{ds2}) \approx g_{m2}R_2 \tag{2.26}$$

As can be seen from Equation 2.25, the input impedance is nearly $(1 + g_{m2}R_2)$ times smaller than that of a common gate TIA. The RGC-TIA has low input impedance which is the main benefit of this structure. The low-frequency trans-impedance gain is given as

$$A_T = R_1 \tag{2.27}$$

Considering the effect of the gate-source, the gate-drain and load capacitances, frequency dependent trans-impedance gain of RGC-TIA can be expressed as follows

$$A_T = \frac{g_{m1}(g_{m2} + \frac{1}{R_2})}{(\frac{1}{R_1 + C_{out}s})[(g_{m2} + \frac{1}{R_2})(g_{m1} + C_1 s) + (\frac{1}{R_2} + C_1 s)(\frac{1}{r_{o,c}} + C_T s)]} \tag{2.28}$$

where $C_{in} = C_{PD} + C_{ESD} + C_{PAD}$, $C_T = C_{in} + C_{gs2}$, $C_1 = C_{gd2} + C_{gs1}$ and $R_2 = R_2//r_{ds2}$

Because $C_T \gg C_1$ and C_L

the dominant pole ω_{P1} is defined as

$$\omega_{P1} = \frac{g_{m1}(g_{m2}R_2 + 1)}{C_T} \tag{2.29}$$

The other poles of the RGC-TIA are given as

$$\omega_{P2} = \frac{1}{R_1 C_{out}} \tag{2.30}$$

$$\omega_{P3} = \frac{g_{m1}}{C_1} \tag{2.31}$$

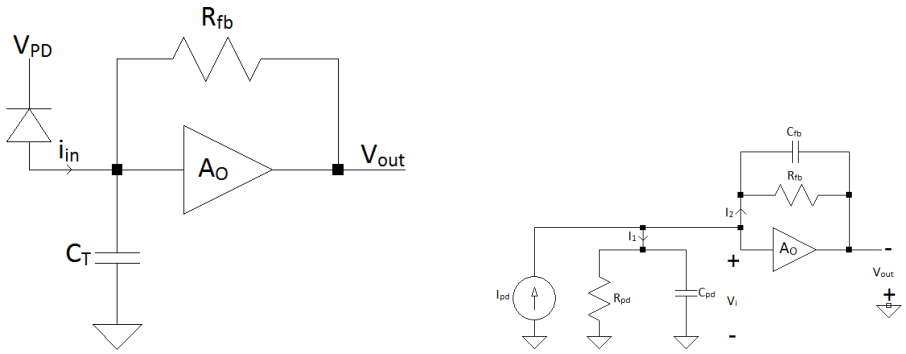
This dominant pole described above determines the bandwidth of RGC.

Comparing Equation 2.29, for the same g_{m1} the bandwidth of RGC is $(1 + A_{CS})$ times greater than that of CG-TIA [5], [6].

2.2.2.2. Shunt-Shunt Feedback TIA. Figure 2.14 (a) shows the basic circuit of shunt feedback TIA and Figure 2.14 (b) shows the TIA circuitry with photodiode model. In the circuitry (Figure 2.14 (a)) C_T includes the input capacitance of the TIA and the capacitance of the photodiode [5].

The trans-impedance gain is given as below

$$Z_{TIA} = \frac{V_o(\omega)}{I_o(\omega)} = \frac{R_{fb}\frac{A_0}{1+A_0}}{1 + j\omega C_T R_{fb}\frac{1}{1+A_0}} \tag{2.32}$$



(a) (b)

Figure 2.14. (a) Basic circuit of shunt feedback TIA, (b) TIA circuitry with photodiode model [5], [6].

where A_0 is the open loop gain of the amplifier, R_{fb} is the feedback resistor and C_T consists of the photodiode capacitance and the TIA input capacitance.

The DC trans-impedance gain can be expressed as follows

$$GAIN = R_{fb} \tag{2.33}$$

The bandwidth of shunt feedback TIA is given as below

$$BW = \frac{1 + A_0}{2\pi C_T R_{fb}} \tag{2.34}$$

The transfer function can be expressed as follows

$$G(\omega) = \frac{V_o}{I_{pd}} = -\frac{Z_{fb}}{1 + \frac{1}{A(\omega)}(1 + \frac{Z_{fb}}{Z_{pd}})} \tag{2.35}$$

where Z_{fb} is defined as

$$Z_{fb} = R_{fb}//C_{fb} \tag{2.36}$$

where R_{fb} is feedback resistor and C_{fb} is feedback capacitor.

Z_{pd} is expressed as

$$Z_{pd} = R_{pd}//C_{pd} \tag{2.37}$$

where R_{pd} is photodiode resistor and C_{pd} is photodiode junction capacitor.

$A(\omega)$ is given by

$$A(\omega) = \frac{A_0}{1 + j\frac{\omega}{\omega_T}A_0} \tag{2.38}$$

3dB bandwidth is defined as

$$BW = \frac{1}{2\pi(R_{fb}C_{fb})} \tag{2.39}$$

2.3. Zero Force Equalizer

There are various types of equalizers. According to where they are placed in the channel, they can be pre-equalizer or post-equalizer blocks. When it is placed at the transmitter side, it is called pre-equalizer. If it is placed at the receiver side, it is called post-equalizer. It may be placed at both sides as well. Equalizer block can be active or passive. While the passive equalizer introduces reduction in the strength of a signal at certain frequencies, the active equalizer can amplify or attenuate certain frequencies in order to obtain the required channel equalization. The last classification scheme is related to the coefficients. If an equalizer has a fixed coefficient which is suitable for a time variant channel, it is called a fixed equalizer. On the other hand, if the coefficients can be adjusted in order to equalize for a time variant channel, it is called an adaptive equalizer. Different kinds of equalization methods utilized at transmitter and/or receiver side can be seen in Figure 2.15 shown below [2].

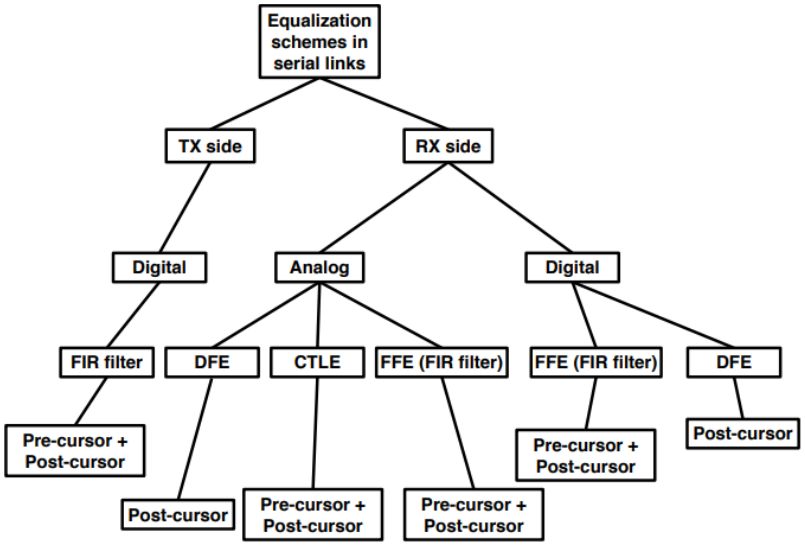


Figure 2.15. Equalizer methods utilized in high speed links [2]

LEDs have a limited bandwidth and their frequency response is modeled as a low-pass filter. Therefore, in order to obtain the best frequency response performance it is necessary to make a combination of the LED with one of the above equalization types [5], [6].

2.3.1. Passive Continuous Time Linear Equalizer (Passive CTLE)

A passive equalizer is a high pass filter. The low frequency components are attenuated in this filter [7]. Figure 2.16 shows passive CTLE circuit.

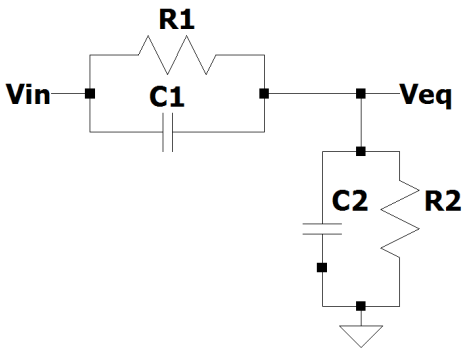


Figure 2.16. Passive CTLE circuit [7].

The branch $R_2//C_2$ creates a pole which is given as

$$\omega_p = \frac{1}{\frac{R_1 R_2}{R_1+R_2}(C_1 + C_2)} \tag{2.40}$$

The branch $R_1//C_1$ creates a zero which can be expressed as follows

$$\omega_z = \frac{1}{R_1 C_1} \tag{2.41}$$

The low frequency signal is attenuated by resistance R_1. DC GAIN (A_{CTLE}) can be defined as follows

$$A_{CTLE}(0) = \frac{R_2}{R_1 + R_2} \tag{2.42}$$

High frequency gain ($A_{CTLE}(\omega \to \infty)$) is dependent on C_1 and C_2. It is given by the following equation

$$(A_{CTLE}(\omega \to \infty)) = \frac{C_1}{C_1 + C_2} \tag{2.43}$$

Peaking can be found dividing high frequency gain by DC gain as in Equation 2.44

$$\text{Peaking} = \frac{(\mathrm{A_{CTLE}}(\omega \to \infty))}{\mathrm{A_{CTLE}}(0)} = \frac{\omega_\mathrm{p}}{\omega_\mathrm{z}} = \frac{\mathrm{R_1 + R_2}}{\mathrm{R_2}} \frac{\mathrm{C_1}}{\mathrm{C_1 + C_2}} \tag{2.44}$$

By adjusting the zero and pole with attenuation, equalization can be performed.

Transfer function of the passive CTLE circuit is expressed as follows

$$H(s) = \frac{R_2}{R_1 + R_2} \frac{1 + R_1 C_1 s}{1 + \frac{R_1 R_2}{R_1 + R_2}(C_1 + C_2)s} \tag{2.45}$$

2.3.2. Active Continuous Time Linear Equalizer (Active CTLE)

Figure 2.17 shows active CTLE circuit with its frequency response where frequencies of zero, the first and second pole are displayed. Source degeneration structure is used. This structure is efficient in obtaining a transfer function of the amplifier which is the inverse of the transfer function of the LED [8].

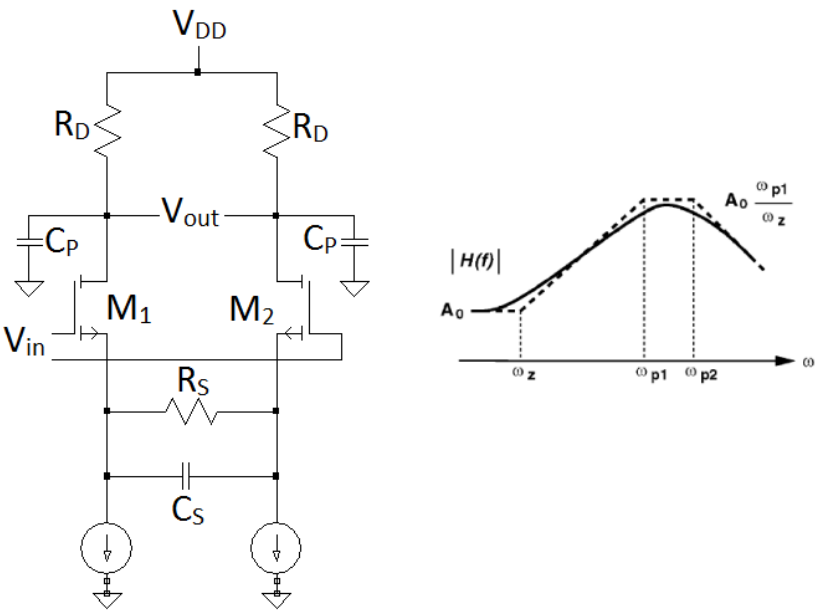


Figure 2.17. Active CTLE circuit [8].

At low frequencies, the impedance of the capacitor C_s is too high. Therefore, it can be assumed that the capacitor is an open circuit. In this situation, the gain of the amplifier is degenerated at low frequencies as in Equation 2.46

$$A(0) = \frac{g_m R_D}{1 + \frac{g_m R_S}{2}} \tag{2.46}$$

At high frequencies, the impedance of the capacitor C_s is too low. Hence, it can be assumed that the capacitor is a short circuit which shorts the resistance R_s. Therefore, high-frequency gain can be achieved. The maximum gain of the circuit is given as

$$A_{max} = g_m R_D \tag{2.47}$$

The location of the first pole is given as

$$\omega_{p1} = \frac{1 + \frac{g_m R_s}{2}}{R_s C_s} \tag{2.48}$$

$$\approx \frac{g_m}{2C_s} \tag{2.49}$$

The location of this pole can be adjusted by altering the degenerating resistor (R_s) value and the capacitor (C_s) value.

The location of the zero is defined as in Equation 2.50. The location of this zero can be adjusted by changing the degenerating resistor (R_s) value and the capacitor (C_s) value. Hence, the bandwidth of the Equalizer circuit can be changed as can be seen from Figure 2.17.

$$\omega_z = \frac{1}{R_s C_s} \tag{2.50}$$

As can be seen from Figure 2.17, another pole exists. The location of this second pole can be changed by varying the resistor R_D and C_p as in Equation 2.51.

$$\omega_{p2} = \frac{1}{R_D C_P} \tag{2.51}$$

Equations 2.52 shows the transfer function in summary.

$$H(s) = \frac{g_m}{C_p} \frac{s + \frac{1}{R_S C_S}}{(s + \frac{1 + \frac{g_m R_S}{2}}{R_S C_S})(s + \frac{1}{R_D C_P})} = A_0 \frac{s + \omega_{z1}}{(s + \omega_{p1})(s + \omega_{p2})} \tag{2.52}$$

Ideal Peaking is given in Equations 2.53.

$$Peaking = \frac{Peak\, A_0}{DC\, A_0} = \frac{\omega_{p1}}{\omega_z} = 1 + \frac{g_m R_S}{2} \tag{2.53}$$

3. Printed Circuit Board Realization of Zero Force Equalizer

Design considerations of two PCBs (TIA and Discrete Receiver System) with simulation and measurement results are given in this chapter.

3.1. Printed Circuit Board Design

In this Chapter, the design and implementation of the TIA and Discrete Receiver System are presented.

3.1.1. TIA

Figure 3.1 shows the TIA schematic.

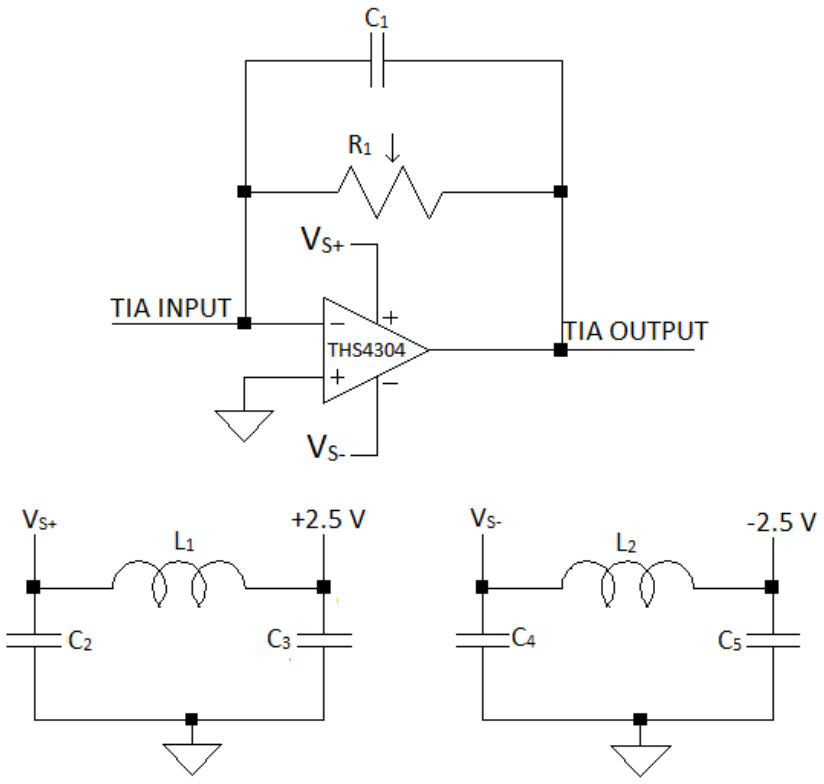
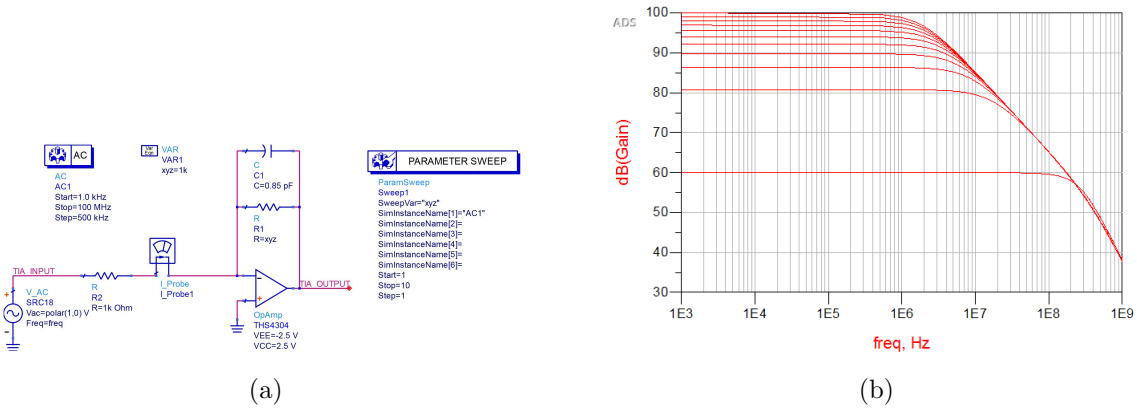


Figure 3.1. Circuit schematic of TIA.

This circuit is designed using a wide bandwidth operational amplifier (THS4304, bandwidth = 3 GHz) in inverting configuration. In this configuration, the inverting input receives feedback from the output. There is a feedback resistor (R_1) connected between the inverting input and amplifier output. In addition, this TIA is configured with split power supply (+2.5 V and -2.5 V). In order to obtain proper operation, power supply bypass capacitors (C_2, C_3, C_4 and C_5) are used with Ferrite beads (L_1 and L_2) which are shown at the bottom of the Figure 3.1 above. In order to reduce parasitic capacitance, the ground plane is removed from under the part.

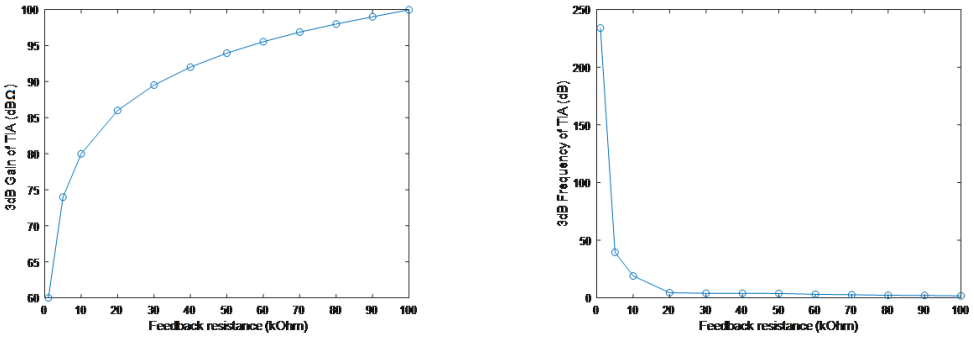
Sweep analysis is performed in order to determine the values of the components of the TIA. While the circuit schematic (Figure 3.2 (a)) used for sweep analysis is shown on the left, the right-hand graph (Figure 3.2 (b)) shows the effect of the feedback resistance on 3-dB gain (in dBΩ) and 3-dB frequency.



(a) (b)

Figure 3.2. (a) Circuit schematic utilized for sweep analysis, (b) Effect of feedback resistance on 3-dB gain and 3-dB frequency.

Figure 3.3 (a) shows the feedback resistance versus 3-dB gain of the TIA. Feedback resistance versus 3-dB frequency of the TIA is shown in Figure 3.3 (b). The first graph is obtained by sweeping the feedback resistance from 1 kΩ to 100 kΩ at 10 kΩ intervals. The second graph is obtained by sweeping the feedback resistance from 1 kΩ to 100 kΩ at 10 kΩ intervals.



(a) (b)

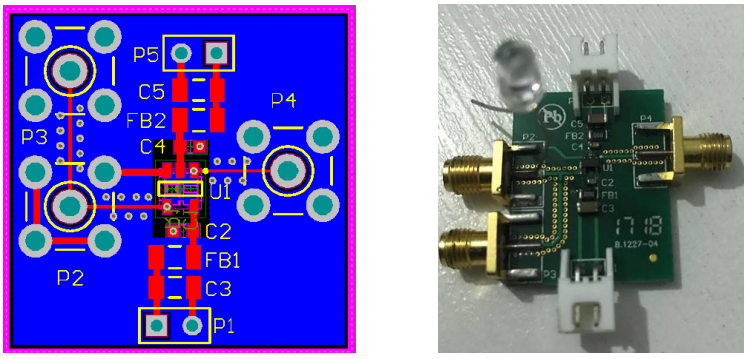
Figure 3.3. (a) Feedback resistance versus 3-dB gain, (b) Feedback resistance versus 3-dB frequency.

In view of the above graphs, the components in the Table 3.1 below are selected.

Table 3.1. Bill of Materials of TIA.

Description	**SMD Size**	**Reference Designator**	**PCB Quantity**
Integrated Circuit THS4304		THS4304	1
Capacitor, 100 nF Ceramic	0603	C2, C4	2
Capacitor, 3.3 μF Ceramic	1206	C3, C5	2
Bead, ferrite 3 A, 80 Ω	1206	L1, L2	2
Connector, 180 C Female, SMA			3
Trimpot, 100 K Cermet Multi Turn Tube		R1	1

Layout and realized PCB of the TIA prepared using the elements in the table above are shown in Figure 3.4 (a) and (b) respectively.



(a) (b)

Figure 3.4. (a) Layout, (b) Realized.

3.1.2. Discrete Receiver System

Figure 3.5 shows the Discrete Receiver System schematic.

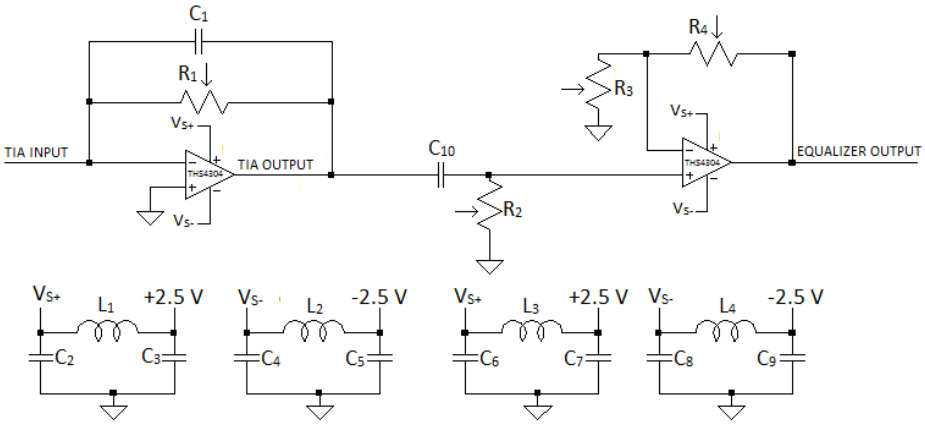


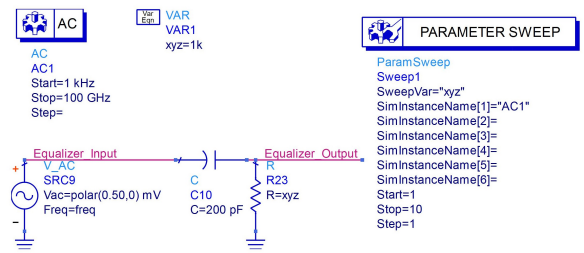
Figure 3.5. Circuit schematic of the Discrete Receiver System.

It consists of 3 parts which are trans-impedance amplifier, equalizer and amplifier. The equalizer is designed using active high pass filter whose operation is the same as RC passive high pass filter. The only difference is that this circuit has an operational amplifier in order to be able to control the gain. Shortly, it includes a passive filter

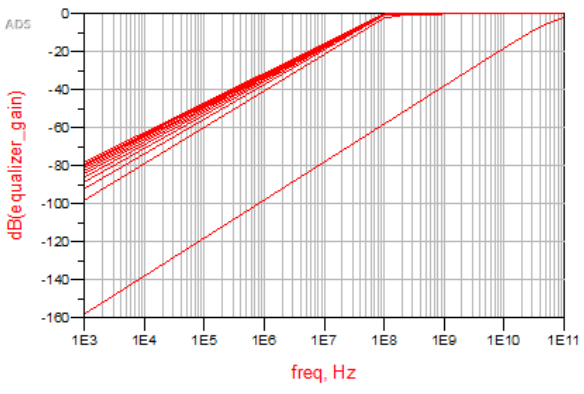
which is followed by a non-inverting amplifier. In order to reduce parasitic capacitance, the ground plane is removed from under the part.

A wide bandwidth operational amplifier (THS4304, bandwidth = 3 GHz) is also selected as an amplifier for this equalizer. As in the TIA, It is configured with split power supply (+2.5 V and -2.5 V). In order to obtain proper operation, power supply bypass capacitors (C_6, C_7, C_8 and C_9) are used with Ferrite beads (L_3 and L_4) which can be seen at the bottom of Figure 3.5.

The first block in this discrete receiver system is TIA. The values related to the TIA were determined in the previous section. Sweep analysis is performed in order to determine the values of the components of the equalizer. While Figure 3.6 (a) shows the circuit schematic used for sweep analysis, Figure 3.6 (b) shows the effect of the equalizer resistance on cutoff frequency.



(a)



(b)

Figure 3.6. (a) Circuit schematic utilized for sweep analysis, (b) Effect of equalizer resistance on cutoff frequency.

Equalizer resistance versus 3-dB Cutoff frequency of Equalizer is given in Figure 3.7.

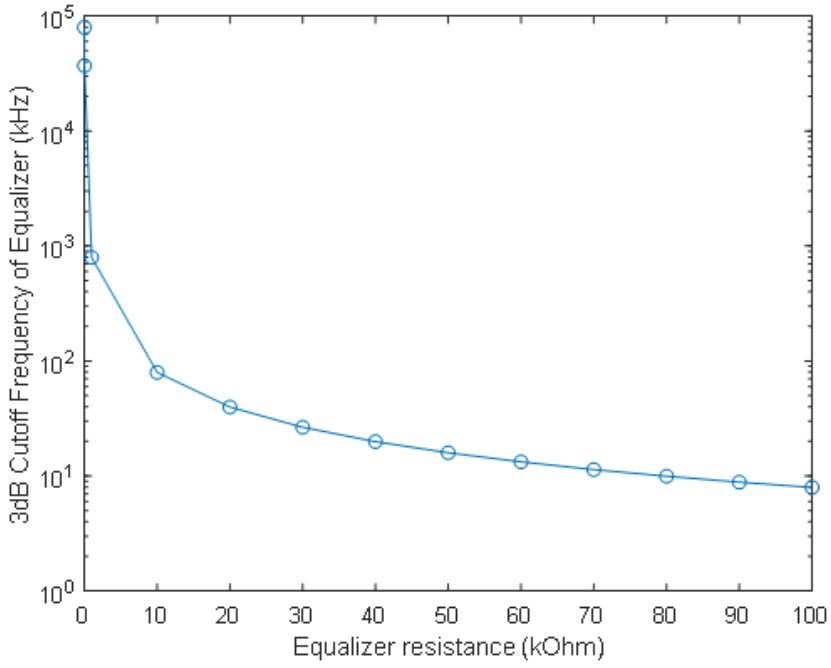
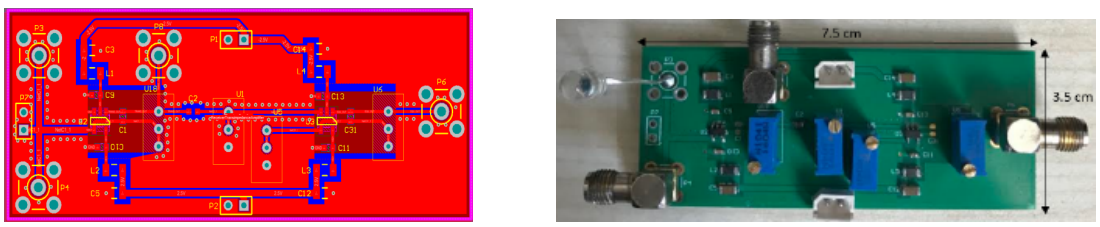


Figure 3.7. Equalizer resistance versus 3-dB Cutoff frequency.

Layout and realized PCB of the Discrete Receiver System prepared using the elements in the Table 3.2 below are shown in Figure 3.8 (a) and (b).



(a) (b)

Figure 3.8. (a) Layout, (b) Realized.

In view of the above graphs (Figure 3.6 and Figure 3.7), the components in the Table 3.2 below are selected for Discrete Receiver System.

Table 3.2. Bill of Materials of Discrete Receiver System.

Description	**SMD Size**	**Reference Designator**	**PCB Quantity**
Integrated Circuit THS4304		THS4304	2
Capacitor, 100 nF Ceramic	0603	C2, C4 C6, C8	4
Capacitor, 3.3 μF Ceramic	1206	C3, C5 C7, C9	4
Bead, ferrite 3 A, 80 Ω	1206	L1, L2 L3, L4	4
Connector, 90 C Female, SMA			4
Capacitor, 200 pF Ceramic	0603	C10	1
Trimpot, 100 K Cermet Multi Turn Tube		R1, R2 R3, R4	4

3.2. PCB Simulation Results

3.2.1. TIA

Simulations are performed using Agilent Advanced Design System. As can be seen from Figure 3.9, in order to test functionally of the trans-impedance amplifier circuit (no photodiode effect), a series resistor (1 kΩ) is connected to the input of the TIA so that we can produce current. The first stage of the Discrete Receiver System is TIA which is the current to voltage converter. For the amplifier, PSpice model

(THS4304) is used for predicting the circuit behavior of the TIA better.

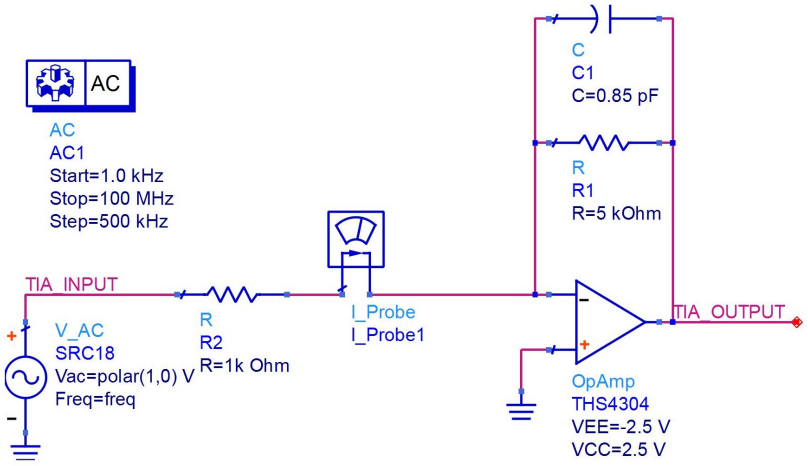


Figure 3.9. Circuit schematic of the TIA for AC simulation.

Feedback resistance and capacitance are 5 kΩ and 0.85 pF respectively. AC simulation from 1 kHz to 100 MHz at 500 kHz intervals is performed and the frequency response of the trans-impedance amplifier circuit is examined. The 3-dB frequency of the trans-impedance amplifier circuit is 36.50 MHz (marker m2) and the midband gain is 73.97 dBΩ (marker m1). The frequency response of the trans-impedance amplifier circuit is shown in Figure 3.10.

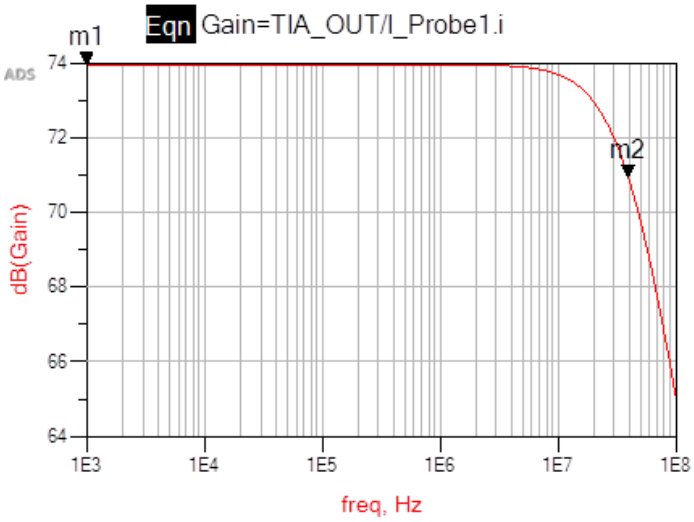


Figure 3.10. Frequency Response of the TIA.

Figure 3.11 shows the circuit schematic of the TIA for transient simulation where input is a sinusoidal wave.

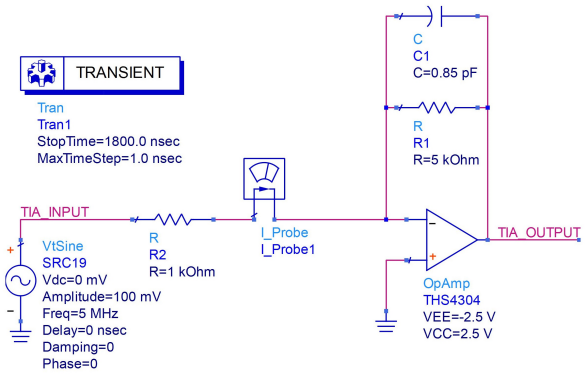
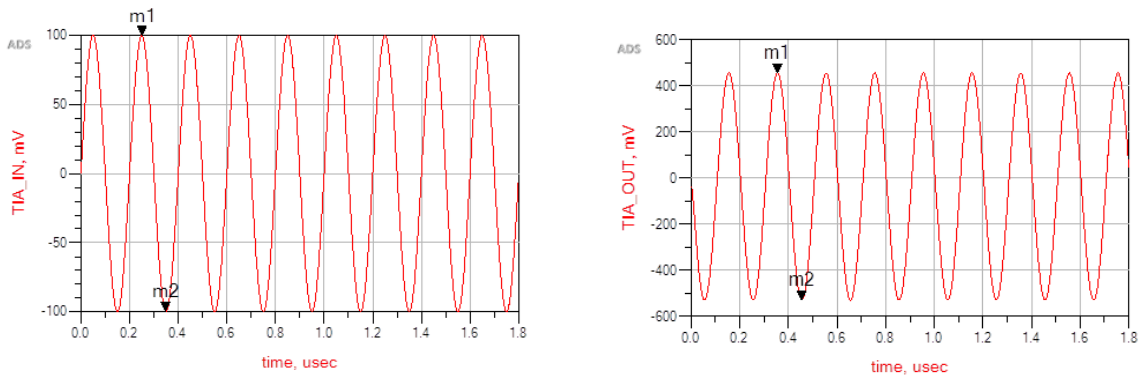


Figure 3.11. Circuit Schematic of the TIA for transient simulation.

Peak-to-peak 200 mV voltage of sinusoidal wave at 5 MHz (Figure 3.12 (a)) is applied to the series resistor (1 kΩ) and the output is examined. Figure 3.12 (a) shows the sinusoidal input. Since the feedback resistance is equal to 5 kΩ, the peak-to-peak value of the output voltage is equal to 0.99 V which is obtained by summing 0.456 V (marker m1) and 0.529 V (marker m2) in Figure 3.12 (b).



(a) (b)

Figure 3.12. (a) Sinusoidal input at 5 MHz, (b) Sinusoidal output of the TIA at 5 MHz.

Figure 3.13 shows the circuit schematic of the TIA for transient simulation where input is a square wave.

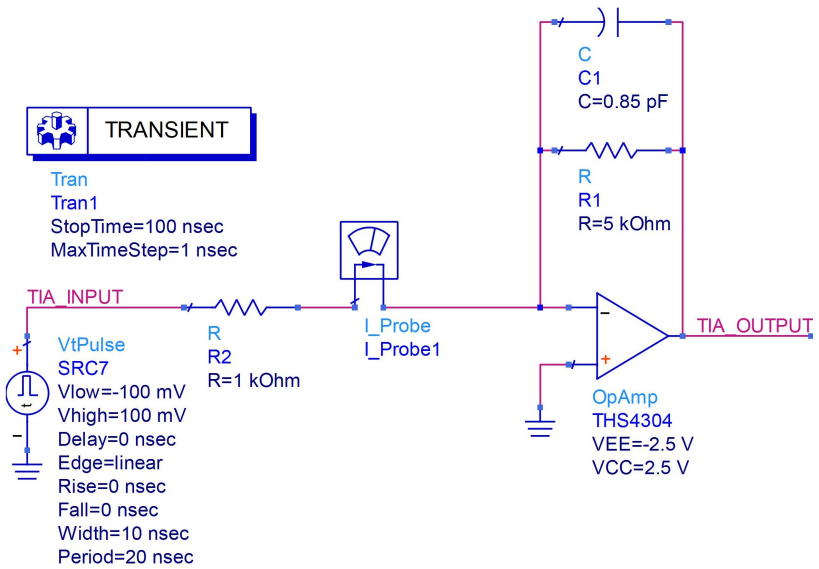
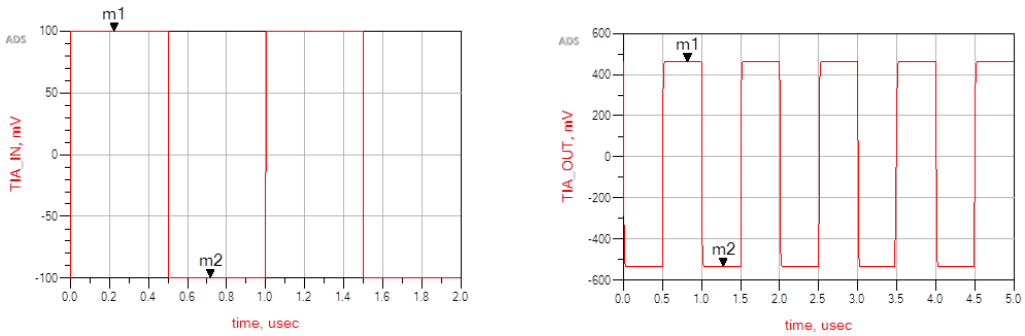


Figure 3.13. Circuit Schematic of the TIA for Transient simulation.

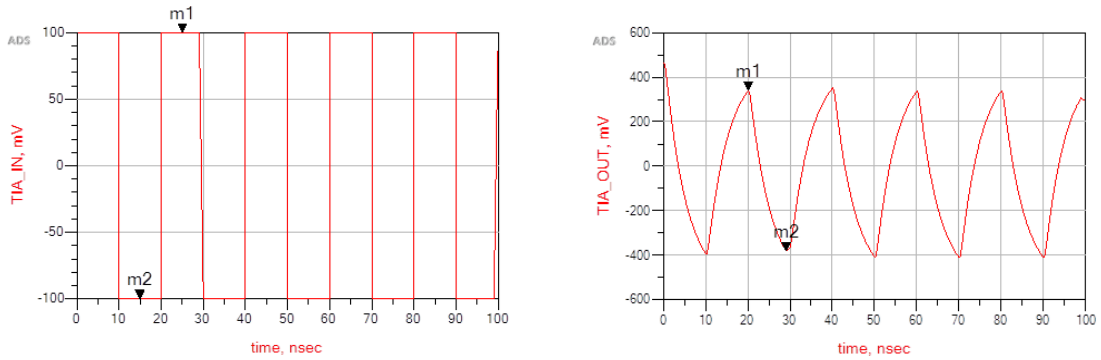
Figure 3.14 (a) and (b) show the applied square wave input and the output at 1 MHz respectively. As can be seen from Figure 3.14 (b), since the frequency is within the bandwidth, the output waveform appears as a square wave and the peak-to-peak value of the output voltage is equal to 1 V which is obtained by summing 0.462 V (marker m1) and -0.535 V (marker m2) in Figure 3.14 (b).



(a) (b)

Figure 3.14. (a) Square wave input at 1 MHz, (b) Output response of the TIA at 1 MHz.

Figure 3.15 (a) and (b) show the applied square wave input and the output at 50 MHz respectively. As can be seen from Figure 3.15 (b), the output waveform is distorted because the frequency is out of the bandwidth.



(a) (b)

Figure 3.15. (a) Square wave input at 50 MHz, (b) Output response of the TIA at 50 MHz.

Figure 3.16 shows the output noise density of the TIA obtained by noise simulation using Agilent Advanced Design System.

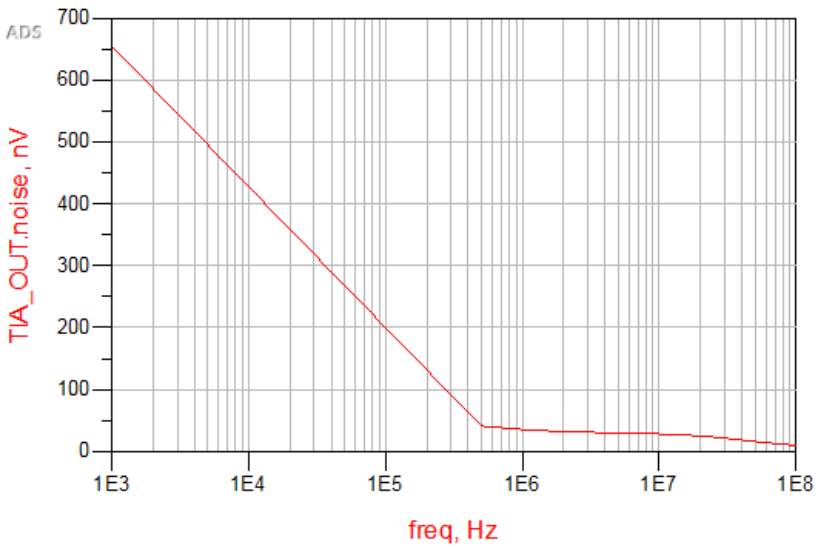


Figure 3.16. The output noise density of the discrete TIA.

Simulation summary of the TIA is shown in Table 3.3 below.

Table 3.3. Simulation summary of TIA.

Midband gain	73.97 dBΩ
3-dB frequency	36.50 MHz
Rise time	0.01 ns
Fall time	0.01 ns
Output range	3 V (p-p)
Input current range	660 μA (p-p)
Noise (input referred)	0.13 nA/$\sqrt{Hz}$
Power consumption	92.5 mW

3.2.2. Discrete Receiver System

Simulations of the Discrete Receiver System are again performed using Agilent Advanced Design System. As can be seen from Figure 3.17, in order to test functionally of the Discrete Receiver System (no photodiode effect), a series resistor (1 kΩ) is connected to the input of the Discrete Receiver System so that we can produce current because the first block of the Discrete Receiver System is TIA which is the current to voltage converter. For the amplifier, PSpice model (THS4304) is used for predicting the circuit behavior of the TIA better.

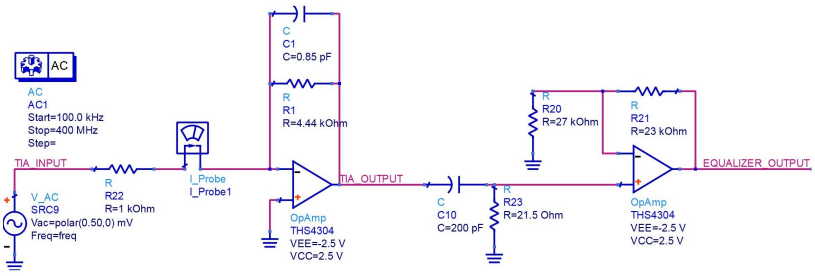
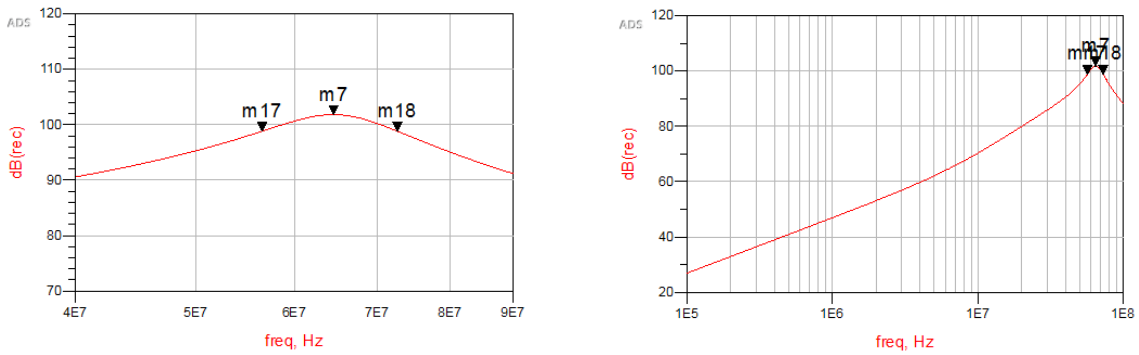


Figure 3.17. Circuit Schematic of the Discrete Receiver System for AC simulation.

Feedback resistance and capacitance of this TIA are 4.44 kΩ (R1) and 0.85 pF (C1) respectively. The second block is the equalizer which consists of 21.5 Ohm resistor (R23) and 200 pF capacitor (C10). This block followed by a non-inverting amplifier for increasing the gain more. It has two resistors of 27 kOhm (R20) and 23 kOhm (R21) which determine the value of the pass band voltage gain. For this amplifier, PSpice model (THS4304) is also utilized for predicting the circuit behavior of the non-inverting amplifier better.

The frequency response of the Discrete Receiver System (zoomed in) from the input of the TIA to the output of the equalizer is shown in Figure 3.18 (a). Figure 3.18 (b) shows the frequency response of the Discrete Receiver System (fully viewed). The first and second pole frequencies are equal to 56.54 MHz (marker m17) and 72.68 MHz (marker m18) respectively.



(a) (b)

Figure 3.18. (a) Frequency response of the Discrete Receiver System (zoomed in), (b) Frequency response of the Discrete Receiver System (fully viewed).

Peak-to-peak 100 mV voltage of sinusoidal wave at 70 MHz (Figure 3.19) is applied to the input of the Discrete Receiver System (to the series resistance (1 kΩ)) and the signal at the equalizer stage output is examined.

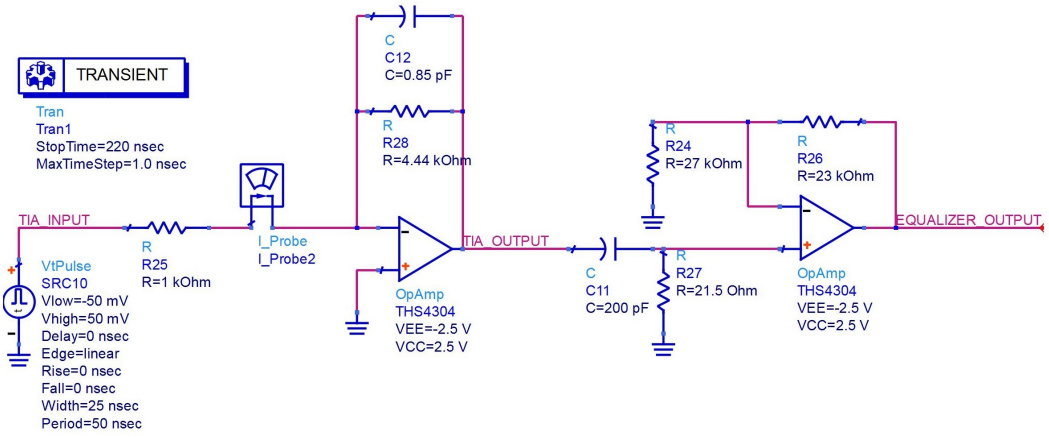
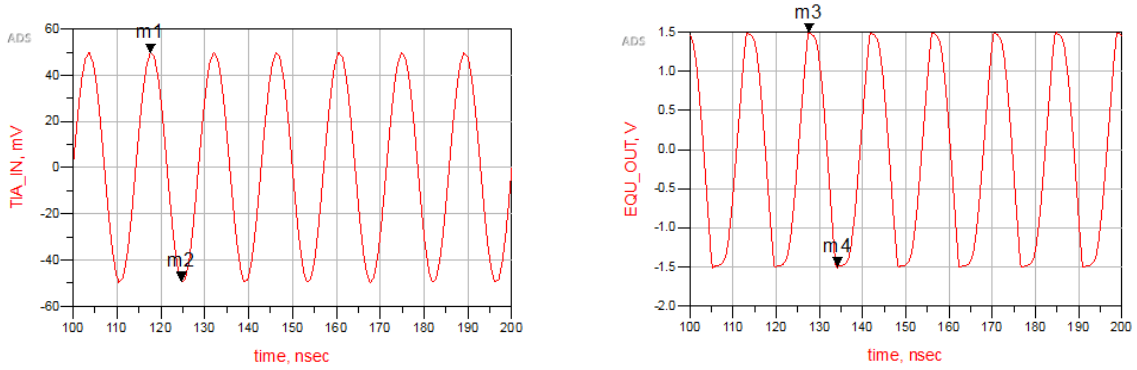


Figure 3.19. Circuit schematic of the Discrete Receiver System for transient simulation.

Figure 3.20 (a) shows the sinusoidal input of the Discrete Receiver System. The peak-to-peak value of the output voltage of the Discrete Receiver System is equal to 2.98 V which is obtained by summing 1.49 V (marker m3) and -1.49 V (marker m4) in Figure 3.20 (b).



(a) (b)

Figure 3.20. (a) Sinusoidal input of the Discrete Receiver System at 70 MHz, (b) Sinusoidal output of the Discrete Receiver System at 70 MHz.

Figure 3.21 shows the circuit schematic of the Discrete Receiver System for transient simulation where input is a square wave.

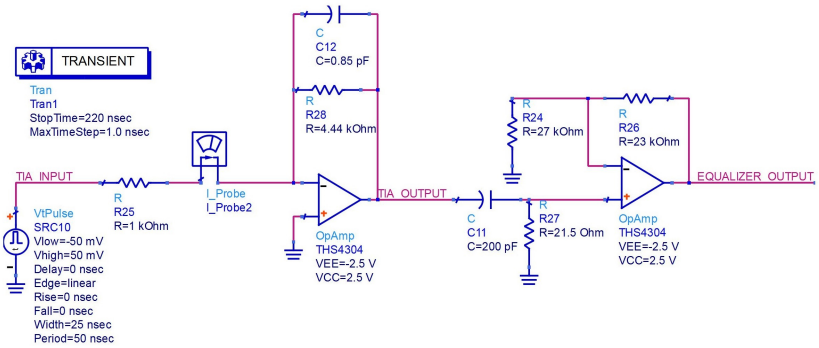
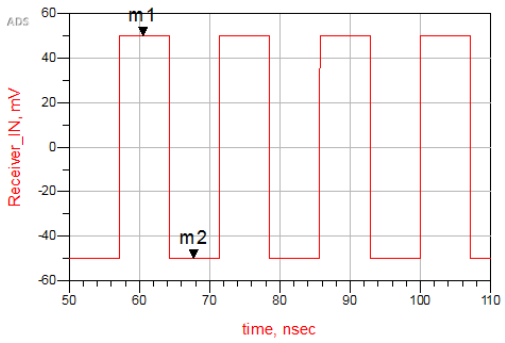
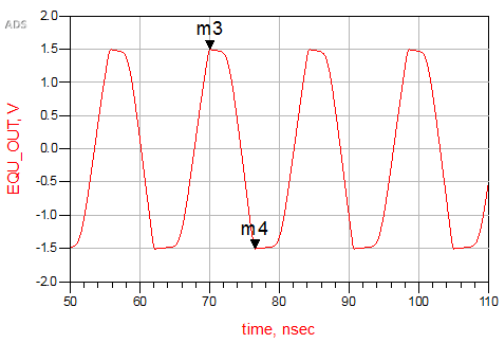


Figure 3.21. Circuit schematic of the Discrete Receiver System for transient simulation.

Figure 3.22 (a) and (b) show the applied square wave input and the output at 70 MHz respectively. As can be seen from Figure 3.22 (b), since the frequency is within the bandwidth, the output waveform almost appears as a square wave and the peak-to-peak value of the output voltage is equal to 2.98 V which is obtained by summing 1.49 V (marker m3) and -1.49 V (marker m4) in Figure 3.22 (b).



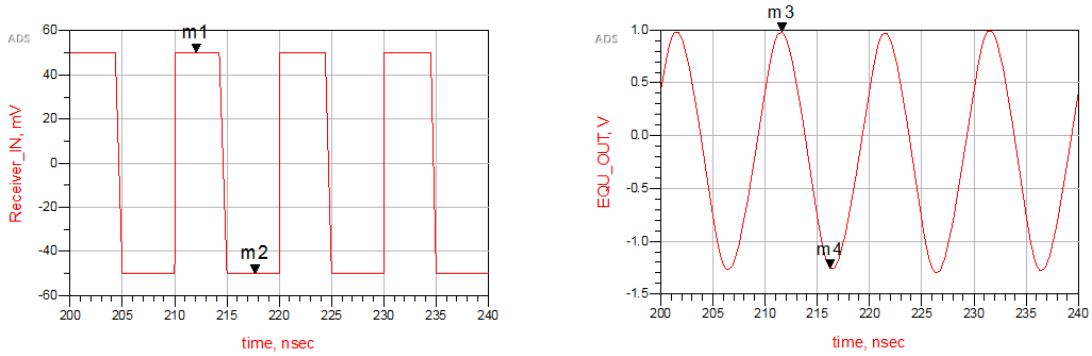
(a)



(b)

Figure 3.22. (a) Square wave input of the Discrete Receiver System at 70 MHz, (b) Output response of the Discrete Receiver System at 70 MHz.

Figure 3.23 (a) and (b) show the applied square wave input and the output at 100 MHz respectively. As can be seen from Figure 3.23 (b), the output waveform is distorted because the frequency is out of the bandwidth of the receiver block.



(a) (b)

Figure 3.23. (a) Square wave input of the Discrete Receiver System at 100 MHz, (b) Output response of the Discrete Receiver System at 100 MHz.

Simulation summary of Discrete Receiver System is presented in Table 3.4 below.

Table 3.4. Simulation summary of Discrete Receiver System.

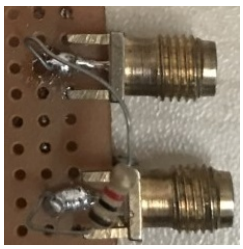
Peaking gain	54 dBΩ
First pole frequency	56.54 MHz
Second pole frequency	72.68 MHz
Rise time	3 ns
Fall time	3 ns
Output range	3 V (p-p)
Input current range	140 μA (p-p)
Power consumption	185 mW

3.3. PCB Measurement Results

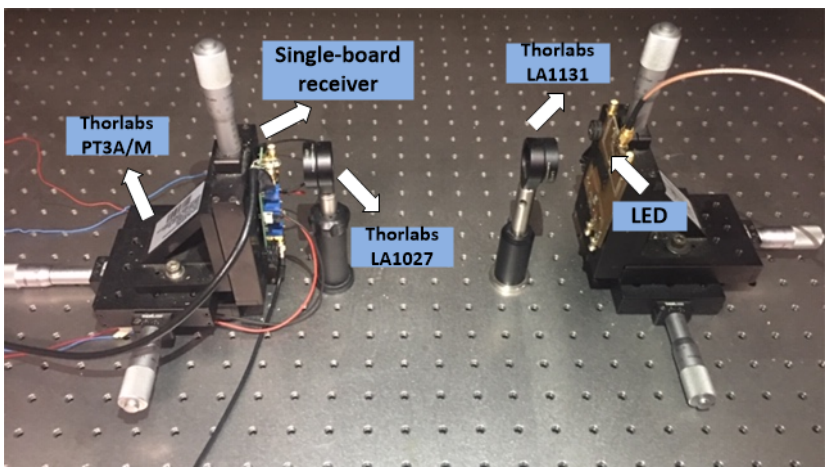
There are three measurements to be discussed in this section. In the first measurement, TIA is tested functionally (no photodiode effect). In the second measurement,

Discrete Receiver System is tested functionally (no photodiode effect). Figure 3.24 (a) shows the series resistor circuit (1 kΩ) which converts the applied voltage to current. From the input of this circuit, we apply a signal, the output of this circuit is connected to the inputs of TIA and Discrete Receiver System for two measurements respectively. This circuit is used for testing two PCBs functionally before performing the test with visible light for Discrete Receiver System. Figure 3.24 (b) demonstrates Measurement Setup for two PCBs (TIA and Discrete Receiver System). In this setup for first two measurements, lenses and visible light generated at the transmitter side by transmitter circuit are not used.

In the third measurement Discrete Receiver System is tested by using the setup in Figure 3.24 (b) where lenses are used with visible light generated at the transmitter side by a LED (bandwidth of the LED is equal to 500 kHz). In addition, a photodiode (bandwidth of the photodiode is equal to 200 MHz) connected to this Discrete Receiver System is used at the receiver side (photodiode effect included).



(a)

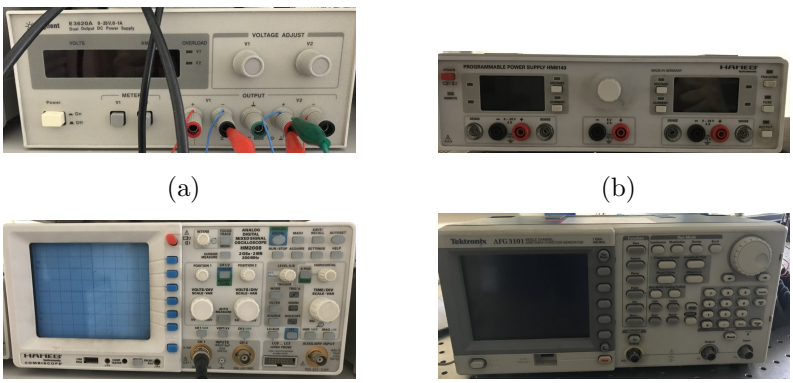


(b)

Figure 3.24. (a) A series resistor circuit for generating current, (b) Measurement Setup.

Figure 3.25 (a), (b), (c) and (d) show the devices used in the setup of the measurement environment for the both TIA and Discrete Receiver System. Because the TIA is configured with split power supply, the power supply shown in Figure 3.25 (a) is

used. +2.5 V and -2.5 V are obtained from this power supply and given to the relevant connector headers on the PCB of TIA. Figure 3.25 (b) demonstrates the Programmable Power Supply used for biasing the photodiode in order to operate it in photoconductive mode (external reverse bias applied). The oscilloscope in Figure 3.25 (c) is utilized in measurement of two PCBs. Figure 3.25 (d) shows the function generator used for generating required electrical signals such as 5 MHz sinusoidal signal.



(a) (b)

(c) (d)

Figure 3.25. (a) DC Power Supply, (b) Programmable Power Supply, (c) HAMEG Oscilloscope, (d) Function Generator.

3.3.1. TIA

Measurements are performed using HAMEG oscilloscope. As can be seen from Figure 3.24 (a), in order to test functionally of the trans-impedance amplifier circuit (no photodiode effect), a series resistor (1 kΩ) is connected between the function generator and the input of the TIA so that we can generate current signal. Feedback resistance is 5 kΩ. AC measurement from 100 kHz to 100 MHz is performed by collecting 23 data. Using the collected data, frequency response of the trans-impedance amplifier circuit is created. The 3-dB frequency of the trans-impedance amplifier circuit is equal to 37.12 MHz and the gain is equal to 73.45 dBΩ. The frequency response of the trans-impedance amplifier circuit is given in Figure 3.26.

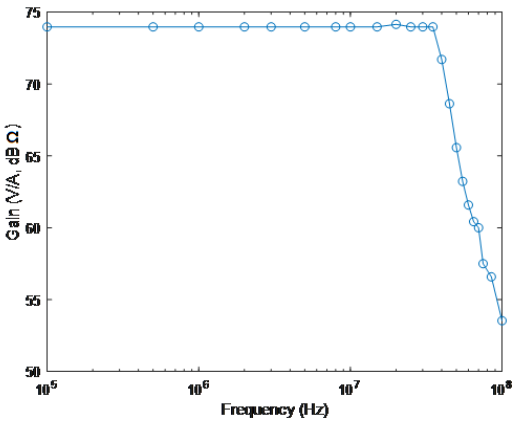
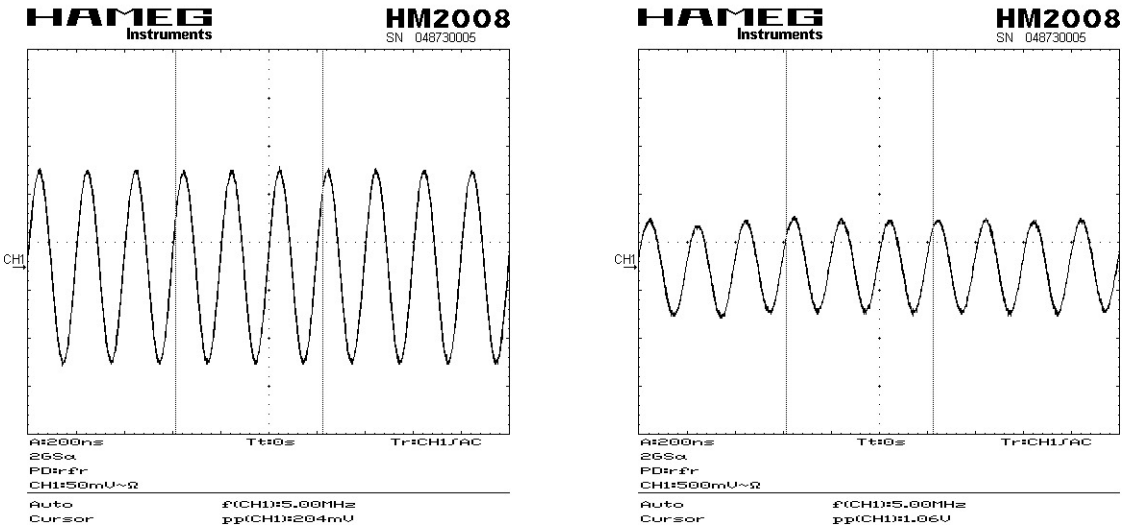


Figure 3.26. Frequency Response of the TIA.

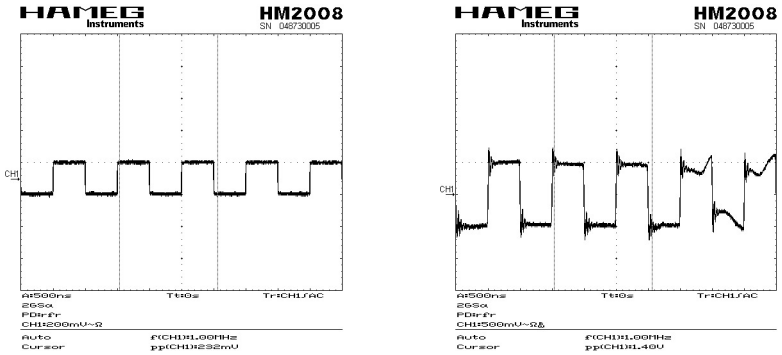
Sinusoidal wave at 5 MHz (Figure 3.27 (a)) is applied to the input and the output is examined. Since the feedback resistance is equal to 5 kΩ, the peak-to-peak value of the output voltage is equal to 1.06 V which is given in Figure 3.27 (b).



(a) (b)

Figure 3.27. (a) Sinusoidal input of the TIA at 5 MHz, (b) Sinusoidal output of the TIA at 5 MHz.

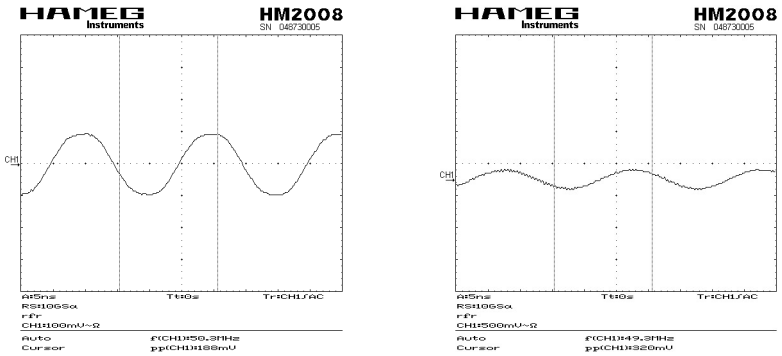
Figure 3.28 (a) and (b) show the applied square wave input and the output at 1 MHz respectively. As can be seen from Figure 3.28 (b), since the frequency is within the bandwidth, the output waveform appears as a square wave and the peak-to-peak value of the output voltage is equal to 1.4 V.



(a) (b)

Figure 3.28. (a) Square wave input of the TIA at 1 MHz, (b) Output response of the TIA at 1 MHz.

Figure 3.29 (a) and (b) show the applied square wave input and the output at 50 MHz respectively. Even if we apply a square wave with a frequency outside the bandwidth, the signal that is generated by the function generator for input is sine-shaped due to its property. Hence, the signal is not distorted in Figure 3.29 (b).



(a) (b)

Figure 3.29. (a) Square wave input of the TIA at 50 MHz, (b) Output response of the TIA at 50 MHz.

Measurement summary of TIA is given in Table 3.5 below.

Table 3.5. Measurement summary of TIA.

Midband gain	73.45 dBΩ
3-dB frequency	37.12 MHz
Rise time	5 ns
Fall time	5 ns
Power consumption	92.5 mW
PCB size	3.5 cm x 3 cm

3.3.2. Discrete Receiver System

As can be seen from Figure 3.24 (a), in order to functionally test the Discrete Receiver System (no photodiode effect), a series resistor (1 kΩ) is connected between the function generator and input of the Discrete Receiver System (input of the first block which is TIA) so that we generate current signal. Measurements are performed using HAMEG oscilloscope. AC measurement from 1 MHz to 100 MHz is performed by collecting 24 data. Using the collected data, frequency response of the discrete receiver system is created. Frequency response of the Discrete Receiver is shown in Figure 3.30. The first and second pole frequencies are equal to 20 MHz and 40 MHz respectively.

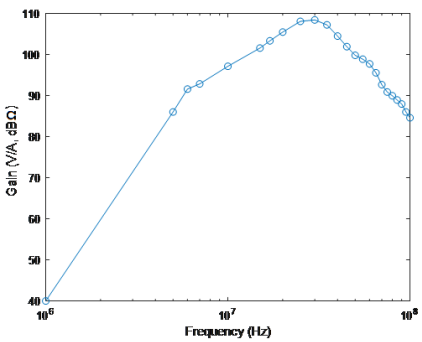
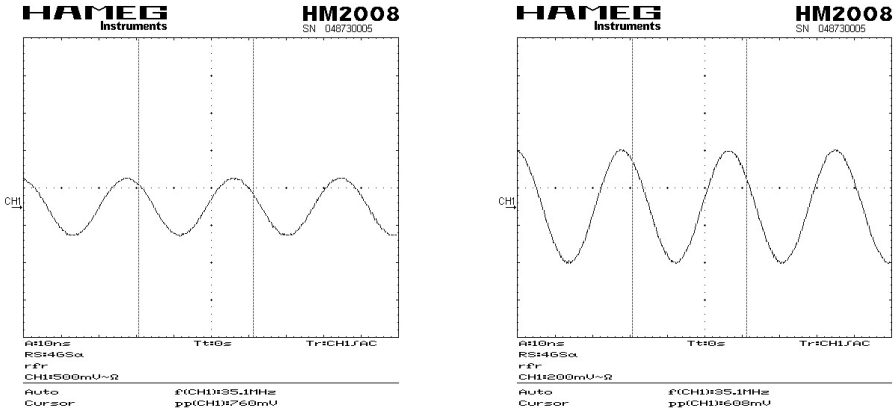


Figure 3.30. Frequency Response of the Discrete Receiver System.

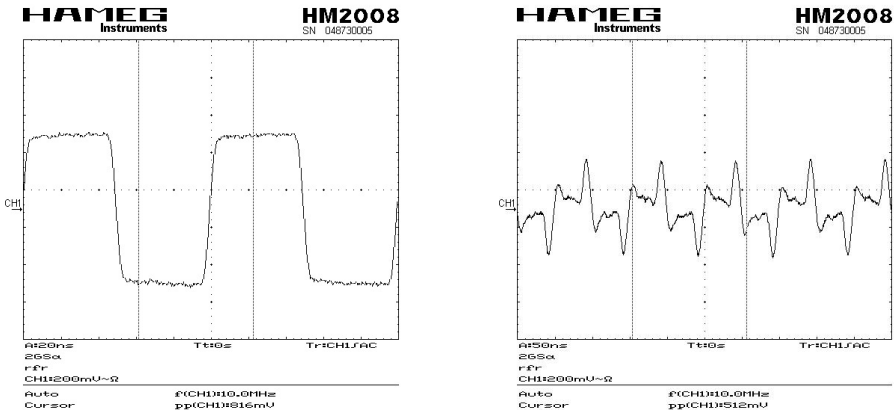
Sinusoidal wave at 35 MHz (Figure 3.31 (a)) is applied to the input of the Discrete Receiver System and the output is examined. The output voltage is equal to 608 mV which is given in Figure 3.31 (b).



(a) (b)

Figure 3.31. (a) Sinusoidal input of the Discrete Receiver System at 35 MHz, (b) Sinusoidal output of the Discrete Receiver System at 35 MHz.

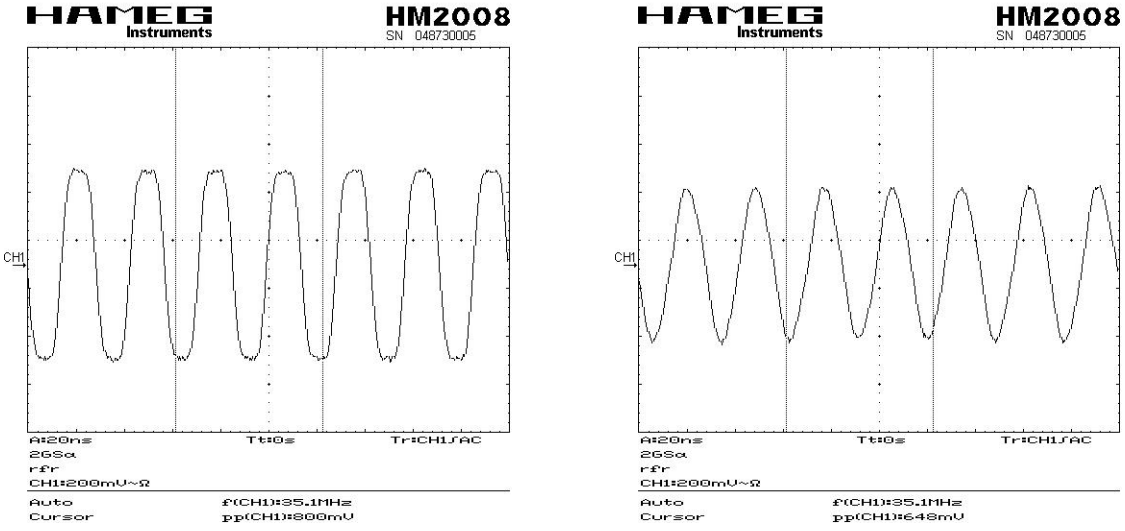
Figure 3.32 (a) and (b) show the applied peak-to-peak 816 mV square wave input and the output at 10 MHz respectively. As can be seen from Figure 3.32 (b), the output waveform is distorted because the frequency is out of the bandwidth.



(a) (b)

Figure 3.32. (a) Square wave input of the Discrete Receiver System at 10 MHz, (b) Output response of the Discrete Receiver System at 10 MHz.

Figure 3.33 (a) and (b) show the applied peak-to-peak 800 mV square wave input and the output at 35 MHz respectively. As can be seen from Figure 3.33 (b), since the frequency is within the bandwidth, the output waveform appears as a square wave and the peak-to-peak value of the output voltage is equal to 648 mV.



(a) (b)

Figure 3.33. (a) Square wave input of the Discrete Receiver System at 35 MHz, (b) Output response of the Discrete Receiver System at 35 MHz.

Measurement summary of Discrete Receiver System is shown in Table 3.6 below.

Table 3.6. Measurement summary of Discrete Receiver System.

Peaking gain	65 dBΩ
First pole frequency	20 MHz
Second pole frequency	40 MHz
Rise time	11 ns
Fall time	11 ns
Power consumption	185 mW
PCB size	7.5 cm x 3.5 cm

3.3.3. Discrete Receiver System with Visible Light Communication

Measurements are performed using HAMEG oscilloscope. LED is forward biased by a 2.8 V DC bias voltage, and driven by a 2 V peak to peak AC signal. AC measurement from 1 MHz to 100 MHz is performed by collecting 24 data. Using the collected data, frequency response of the discrete receiver system with visible light communication is created. The 3-dB frequency of the discrete receiver system with visible light communication is equal to 50.12 MHz. The frequency response of the discrete receiver system with visible light communication (input voltage of the LED divided by output voltage of the Discrete Receiver System) is given in Figure 3.34 (photodiode effect included).

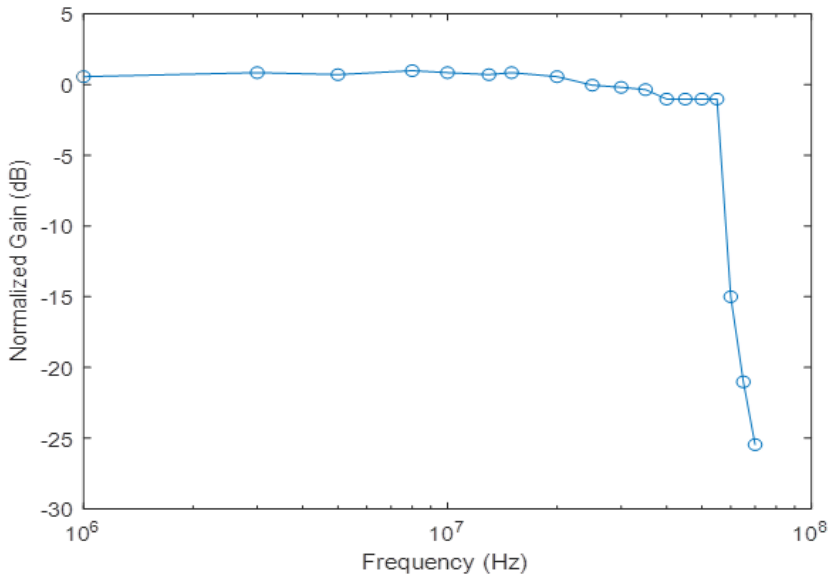
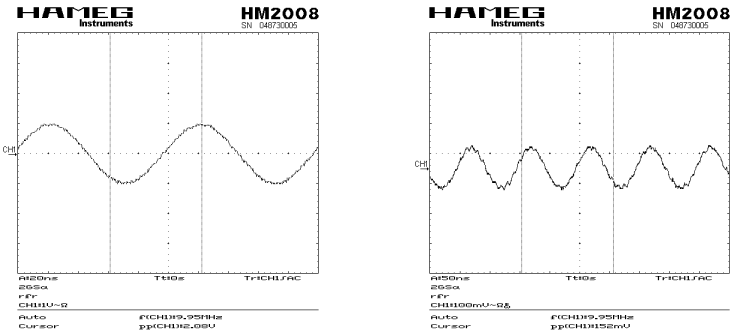


Figure 3.34. Frequency response of the Discrete Receiver System with visible light communication.

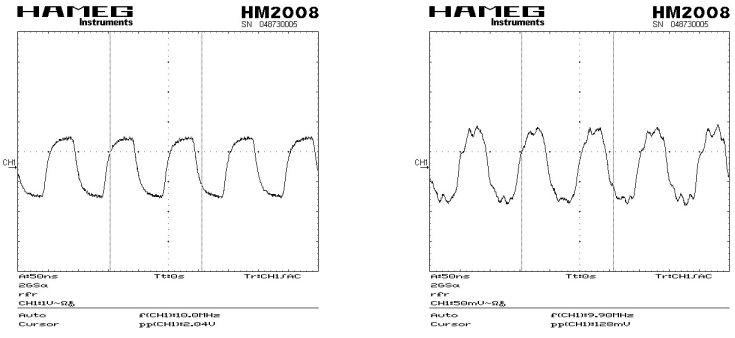
Sinusoidal wave at 10 MHz (Figure 3.35 (a)) is applied to the input of the LED driver circuit and the output of the Discrete Receiver System is examined. The peak-to-peak value of the output voltage is equal to 152 mV which is given in Figure 3.35 (b).



(a) (b)

Figure 3.35. (a) Sinusoidal input of the Discrete Receiver System with visible light communication at 10 MHz, (b) Sinusoidal output of the Discrete Receiver System with visible light communication at 10 MHz.

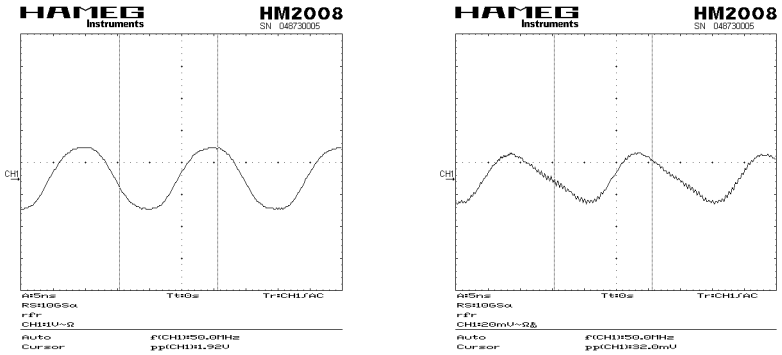
Figure 3.36 (a) and (b) show the applied square wave input to the LED driver circuit and the output of the discrete receiver system at 10 MHz respectively. As can be seen from Figure 3.36 (b), since the frequency is within the bandwidth, the output waveform appears as a square wave.



(a) (b)

Figure 3.36. (a) Square wave input of the Discrete Receiver System with visible light communication at 10 MHz, (b) Output response of the Discrete Receiver System with visible light communication at 10 MHz.

Figure 3.37 (a) and (b) show the applied square wave input to the LED driver circuit and the output of the Discrete Receiver System at 50 MHz respectively. Even if we apply a square wave, the signal that is generated by the function generator for input is sine-shaped due to its property.



(a) (b)

Figure 3.37. (a) Square wave input of the Discrete Receiver System with visible light communication at 50 MHz, (b) Output response of the Discrete Receiver System with visible light communication at 50 MHz.

Measurement summary of Discrete Receiver System with Visible Light Communication is presented in Table 3.7 below.

Table 3.7. Measurement summary of Discrete Receiver System with Visible Light Communication.

3-dB frequency	50.12 MHz
Rise time	23 ns
Fall time	23 ns
Power consumption	185 mW
PCB size	3.5 cm x 3 cm

4. Integrated Circuit

This chapter provides general information about the design of the blocks namely photodiode, trans-impedance amplifier, current mirror and equalizer with Integrated CMOS Receiver System.

4.1. CMOS Technology used for IC Design

In the design of blocks, UMC 130 nm CMOS Technology is used. From this technology, N-12-HSL130E (transistor) device is used for the design of the blocks of trans-impedance amplifier and equalizer. The length of this transistor is constant 130 nm. RNNPO-RF (resistor) and RNHR-RF (resistor) devices are utilized for the design of the blocks of trans-impedance amplifier and equalizer. These are a four terminal resistors where NW terminal is connected to vdd and PSUB terminal is connected to gnd. MOMCAPS-RF device is used for the design of the equalizer block. It is a four terminal capacitor where NW terminal is connected to vdd and PSUB terminal is connected to gnd.

4.1.1. Photodiode

By using the equation shown below, area of photodiode can be calculated for different junction capacitance values.

$$C_j = A\sqrt{\frac{q\varepsilon_{si}\varepsilon_0 N_A N_D}{2(V_{bi}+V_A)(N_A+N_D)}} \tag{4.1}$$

Due to the fact that the process is not revealed by the manufacturer, the junction capacitance of the photodiode has been calculated under the assumption that:

$N_D \gg N_A$ and N_A (the doping concentration in p-type region) is equal to $10^{21}\frac{1}{m^3}$, $\epsilon_{si} = 11.9$ is the dielectric constant of silicon, $\varepsilon_0 = 8.854\times10^{-14}$ F/cm is the permittivity

of free space, $V_A = 0.8V$ is the applied voltage and $V_{bi} = 0.45V$ is the silicon built-in voltage.

Figure 4.1 shows photodiode junction capacitance versus photodiode area. Data points (photodiode area) shown on the graph are obtained by using Equation 4.1 above.

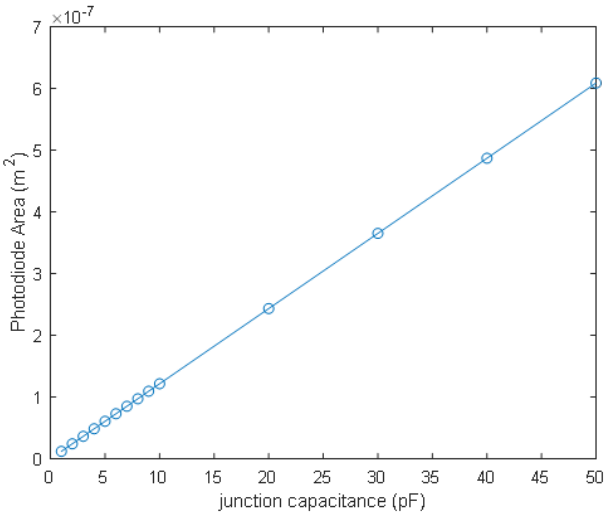


Figure 4.1. Photodiode junction capacitance versus photodiode area.

For the junction capacitance value of 2 pF, the calculated area of photodiode is equal to 154 μm $\times 154 \mu m$. The photodiode models that will be used in the simulations are shown in Figure 4.2.

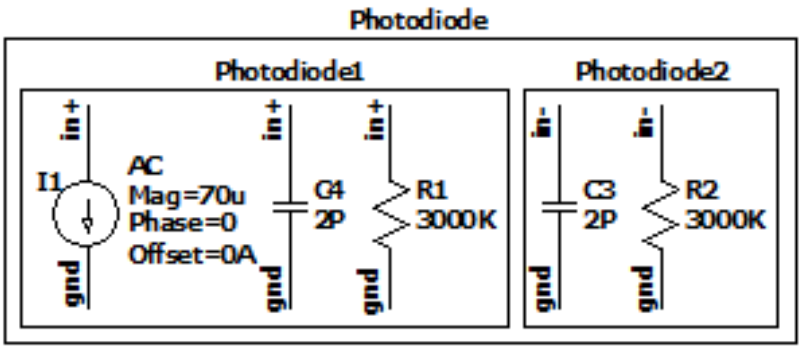


Figure 4.2. Schematic of the equivalents for two types of photodiodes used for simulation.

4.1.2. TIA

The CMOS trans-impedance amplifier designed for IC implementation converts the electrical current obtained from the photodiode into voltage with the least possible noise addition. Therefore, while the input of the circuit is current based, the output is voltage based. The designed and simulated trans-impedance amplifier works as a differential. In the simulation process, one input of the circuit is driven by current, while the other input is not supplied with any current and thus the differential input is formed. The current at the input passes over the feedback resistor in order to form a differential voltage at the output. The schematic design of the trans-impedance amplifier selected for CMOS IC implementation is given in Figure 4.3.

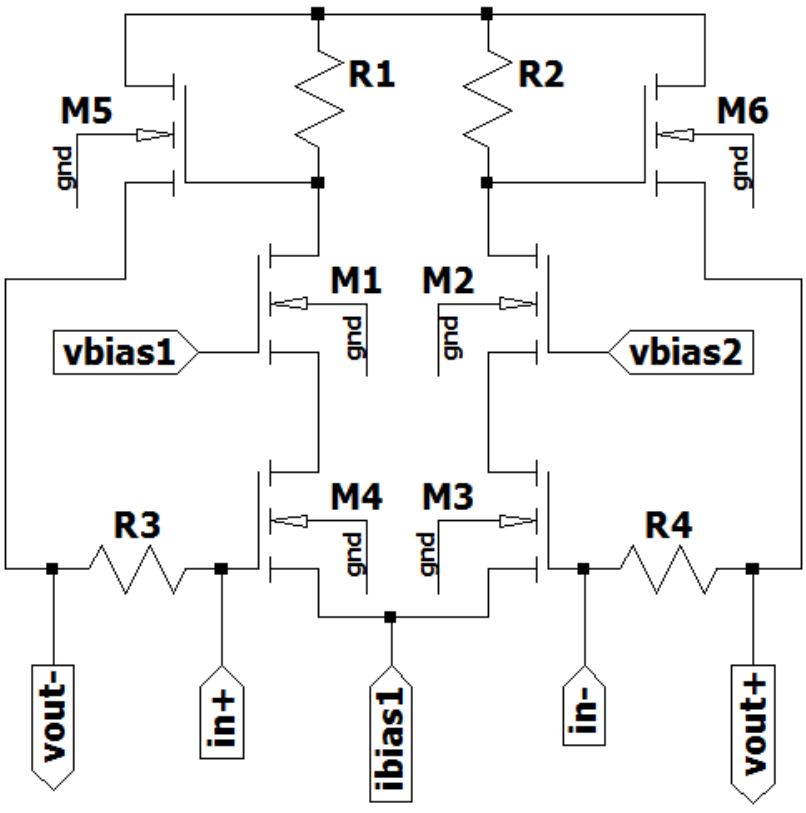


Figure 4.3. Schematic of CMOS TIA circuit.

Block diagram of the CMOS TIA is shown in Figure 4.4 where differential input and output voltages are displayed with two feedback resistors.

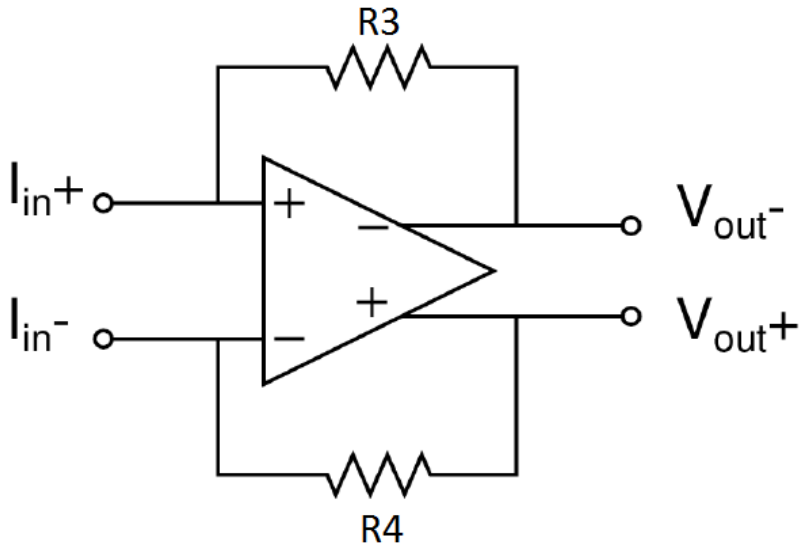


Figure 4.4. Schematic of CMOS TIA circuit (block diagram).

As seen in the schematic of Figure 4.3, the gates of the transistors M3 and M4 are located at the differential input of the circuit. Here, the input of the transistor M4 is driven by the current in order to model the active photodiode, and no current is applied to input of the transistor M3. In addition, cascade connection is used for both (M1 - M4 and M2 - M3) transistor pairs in order to increase the gain. The source terminals of the transistors M5 and M6 are outputs. These two transistors perform the buffering function. Two feedback resistances are used. While the first one is connected between the gate of M4 and the source of M5, the second one is connected between the gate of M3 and the source of M6. Thus, the outputs (the source voltages of the transistors M5 and M6) of this circuit are isolated from the amplifier side. In the trans-impedance amplifier, the transistors M1 and M2 are biased with the voltages Vbias1 and Vbias2.

In addition, a current mirror is implemented with a low voltage topology in order to keep all MOS transistors in the saturation region. This low voltage current mirror is shown in Figure 4.5 where the current of transistor M7 is copied to the transistors M9, M11 and M13.

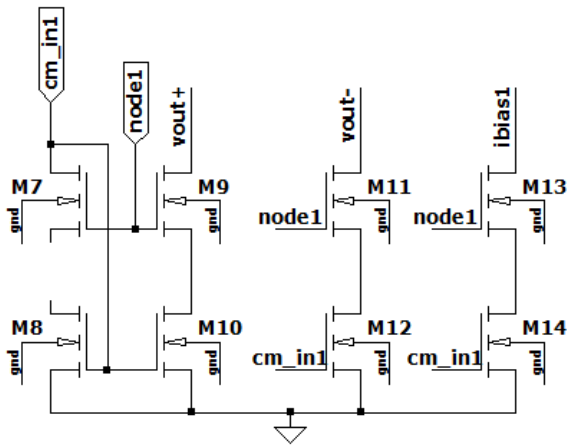


Figure 4.5. Schematic of low voltage current mirror.

In order to observe variation of the 3-dB frequency of TIA, junction capacitance of photodiode is swept. Figure 4.6 shows photodiode junction capacitance versus 3-dB frequency of TIA. This graph was obtained by sweeping the junction capacitance of photodiode from 1 pF to 50 pF (all ten initial values and from 20 pF to 50 pF at 10 pF intervals). The 3 dB Bandwidth values are obtained in AC analysis with Mentor Graphics (pre-layout simulation).

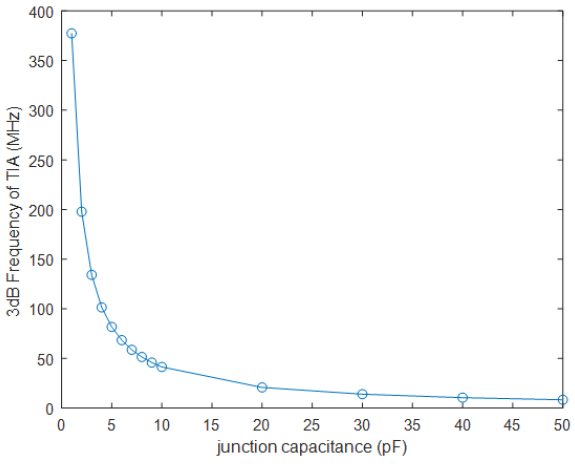


Figure 4.6. Junction capacitance of photodiode versus 3-dB frequency of TIA.

In view of the graph given in Figure 4.6, the components in the Table 4.1 below are selected for the TIA. N-12-HSL130E transistor model is used with RNNPO-RF resistor model. Sizing for all devices in Figure 4.3 is shown in the Table 4.1. In Figure 4.3 the resistance of R1 is equal to 200 Ω which is obtained by connecting X2 and X5 (Table 4.1) in parallel. The resistance of R2 is equal to 200 Ω which is obtained by connecting X1 and X6 (Table 4.1) in parallel. The resistance of R3 is equal to 200 Ω which is obtained by connecting X3 and X7 (Table 4.1) in parallel. The resistance of R4 is equal to 200 Ω which is obtained by connecting X4 and X8 (Table 4.1) in parallel.

Table 4.1. Component values of TIA.

Device	**Type**	**Width**	**Length**	**Multiplier**	**Finger**
M1	NMOS	20u	0.4u	2	1
M2	NMOS	20u	0.4u	2	1
M3	NMOS	20u	0.4u	2	1
M4	NMOS	20u	0.4u	2	1
M5	NMOS	7.5u	0.4u	2	1
M6	NMOS	7.5u	0.4u	2	1
X1	400.049 Ω	6.54u	2u	1	-
X2	400.049 Ω	6.54u	2u	1	-
X3	400.049 Ω	6.54u	2u	1	-
X4	400.049 Ω	6.54u	2u	1	-
X5	400.049 Ω	6.54u	2u	1	-
X6	400.049 Ω	6.54u	2u	1	-
X7	400.049 Ω	6.54u	2u	1	-
X8	400.049 Ω	6.54u	2u	1	-

Similar to the previous procedure, the components in the Table 4.2 below are selected for the low voltage current mirror. N-12-HSL130E transistor model is used. Transistors (M7, M8, M9, M10, M11, M12, M13, M14) have 20 um width, 0.4 um length, 1 finger and 1 multiplier.

Table 4.2. Component values of low voltage current mirrors.

Device	Type	Width	Length	Multiplier	Finger
M7	NMOS	20u	0.4u	1	1
M8	NMOS	20u	0.4u	1	1
M9	NMOS	20u	0.4u	1	1
M10	NMOS	20u	0.4u	1	1
M11	NMOS	20u	0.4u	1	1
M12	NMOS	20u	0.4u	1	1
M13	NMOS	20u	0.4u	1	1
M14	NMOS	20u	0.4u	1	1

Figure 4.7 shows the layout of the trans-impedance amplifier which is drawn using the components in Table 4.1 and 4.2. All CMOS layouts in this study are drawn using common centroid technique where the effect of thermal or linear process gradients is reduced.

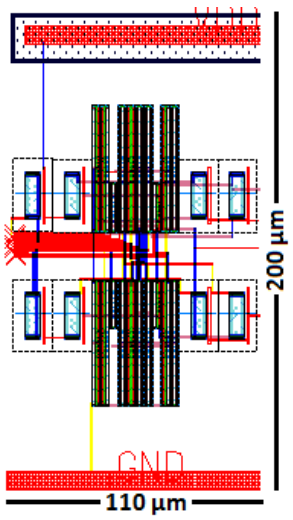


Figure 4.7. Layout of trans-impedance amplifier.

4.1.3. Equalizer

The equalizer design is required since the bandwidth of the light coming onto the receiver is not high and therefore it is necessary to increase the amplitude of the high frequency components. The frequency response of the light source LED is similar to a low-pass filter. The equalizer circuit must show constant gain at low frequencies and the gain must increase with frequency after a certain frequency. In this case, the frequency response of the corresponding equalizer circuit must be like a high-pass filter. Active continuos time linear equalizer with source degeneration structure is used for this purpose. The schematic design of the equalizer selected for CMOS IC implementation is given in Figure 4.8. This circuit uses outputs of the fully differential TIA circuit (given in Figure 4.3) as its inputs.

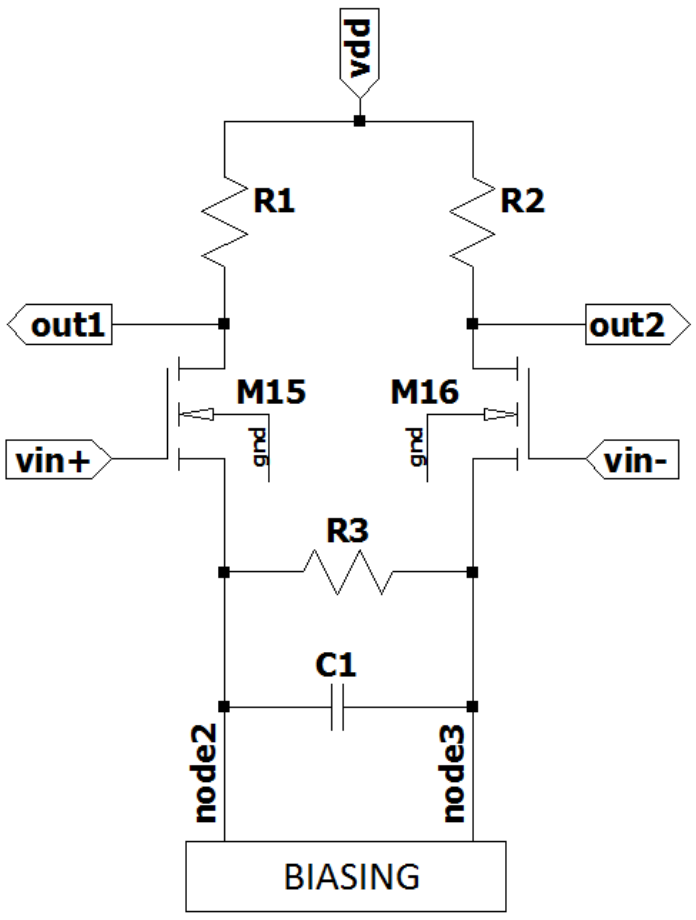


Figure 4.8. Schematic of Equalizer circuit.

The transistors M15 and M16 in the circuit are used in order to produce proportional currents with driving voltages V_{in+} and V_{in-}, respectively. The resistance and capacitance between the drains of the transistors M15 and M16 ensure source degeneration. At low frequencies, the equivalent impedance value increases due to the increase in the impedance of the capacitor as the frequency decreases. Therefore, high resistance is obtained for low frequencies. At high frequencies, the equivalent impedance value decreases due to the decrease in the impedance of the capacitor as the frequency increases. Therefore, low resistance is obtained for high frequencies. Thus, as the frequency increases, the ratio of the output to the input will increase. The resistance and capacitance values have no effect on the DC operating point of the circuit. In addition, these resistance and capacitance values create poles. The nodes Vin+ and Vin- marked as ports are the outputs of the previous block (trans-impedance amplifier) and the AC signal is supplied to the equalizer circuit from these nodes. 180 degrees phase different outputs of the circuit are taken from Out1 and Out2 nodes.

In addition, current mirror is implemented with a low voltage topology in order to saturate the transistors in the circuit. This low voltage current mirror is shown in Figure 4.9 where the current of transistor M7 is copied to the transistors M19 and M21.

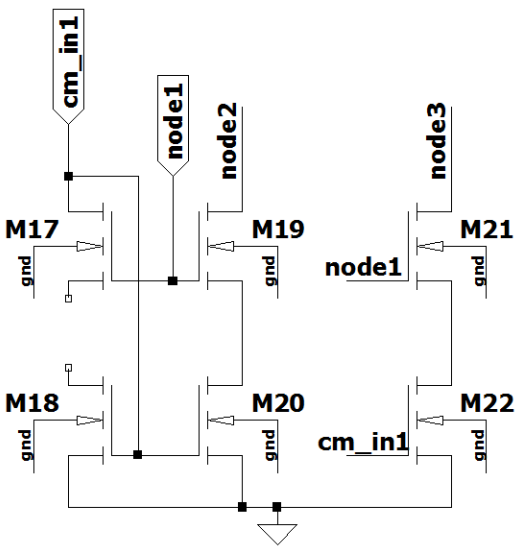


Figure 4.9. Schematic of low voltage current mirror.

In order to observe the low frequency gain and the zero frequency of the Equalizer (explaned in section 2.3.2 in detail), degeneration resistor is swept. Figure 4.10 shows the effect of the degeneration resistor on low frequency gain and zero frequency.

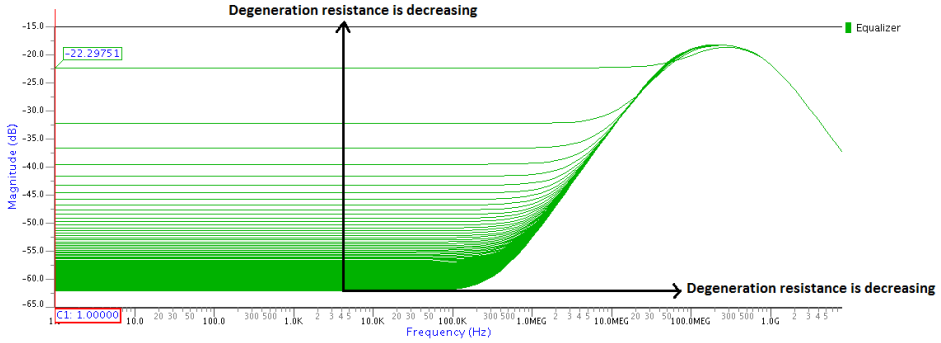
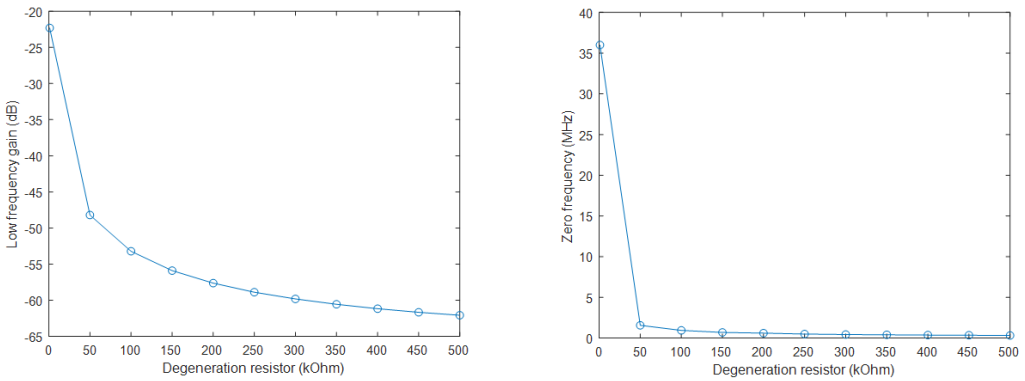


Figure 4.10. Effect of degeneration resistor on low frequency gain and zero frequency.

Figure 4.11 (a) shows degeneration resistor (R3 in Figure 4.8) versus low-frequency gain of the Equalizer. It is obtained by taking 11 low-frequency gain values which are acquired by sweeping the degeneration resistance from 1 kΩ to 500 kΩ at 50 kΩ intervals. Figure 4.11 (b) shows degeneration resistor (R3 in Figure 4.8) versus zero frequency of the Equalizer. This plot is generated by taking 11 zero frequency values which are acquired by sweeping the degeneration resistance from 1 kΩ to 500 kΩ at 50 kΩ intervals.



(a) (b)

Figure 4.11. (a) Degeneration resistor versus low frequency gain, (b) Degeneration resistor versus zero frequency.

In order to observe the first pole frequency and the zero frequency of the Equalizer, degeneration capacitor (C1 in Figure 4.8) is swept. Figure 4.12 shows the effect of the degeneration capacitor on the first pole and zero frequency.

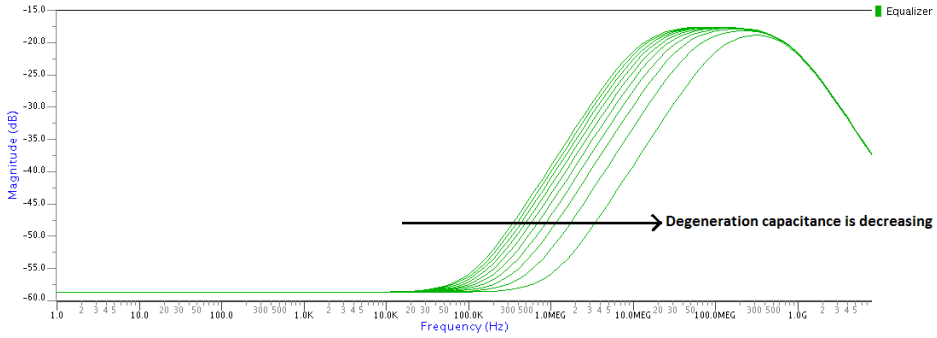
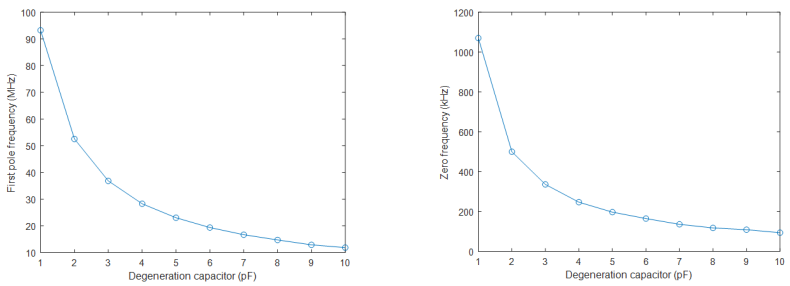


Figure 4.12. Effect of the degeneration capacitor on the first pole frequency and zero frequency.

Figure 4.13 (a) shows degeneration capacitor (C1 in Figure 4.8) versus the first pole frequency of the Equalizer. It is obtained by taking 10 first pole frequency values which are acquired by sweeping the degeneration capacitance from 1 pF to 10 pF at 1 pF intervals. Figure 4.13 (b) shows degeneration capacitor (C1 in Figure 4.8) versus zero frequency of the Equalizer. This plot is generated by taking 10 zero frequency values which are acquired by sweeping the degeneration capacitance from 1 pF to 10 pF at 1 pF intervals.



(a) (b)

Figure 4.13. (a) Degeneration capacitor versus first pole frequency, (b) Degeneration capacitor versus zero frequency.

In order to observe the second pole frequency, load capacitor is swept. Figure 4.14 shows the effect of the load capacitor on the second pole frequency.

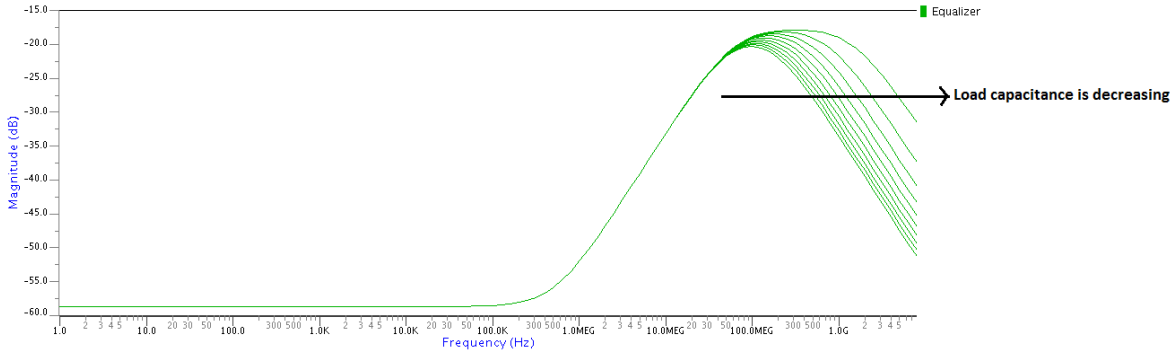


Figure 4.14. Effect of the load capacitor on the second pole frequency.

Figure 4.15 shows load capacitor versus the second pole frequency of the Equalizer. It is obtained by taking 10 second pole frequency values which are acquired by sweeping the load capacitance from 1 pF to 10 pF at 1 pF intervals.

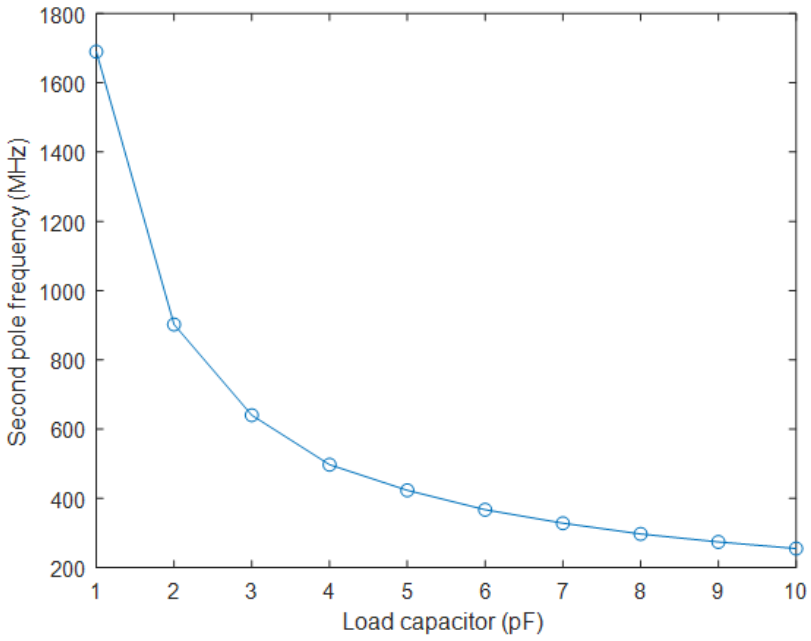


Figure 4.15. Load capacitance versus second pole frequency.

In view of the above graphs in Equalizer section, the components in the Table 4.3 below are selected for this Equalizer. N-12-HSL130E transistor model is used with the resistor models of RNNPO-RF and RNHR-RF. While from X9 to X14, RNNPO-RF resistor model is used, from X15 to X17 RNHR-RF resistor model is utilized. In addition, MOMCAPS-RF capacitor model is used. Sizing for all devices in Figure 4.8 is shown in the Table 4.3. In Figure 4.8 the resistance of R1 is equal to 103.21 Ω which is obtained by connecting X9, X10 and X11 (Table 4.3) in parallel. The resistance of R2 is equal to 103.21 Ω which is obtained by connecting X12, X13 and X14 (Table 4.3) in parallel. The resistance of R3 is equal to 100 kΩ which is obtained by connecting X15, X16 and X17 (Table 4.3) in series. In addition, the capacitance of C1 is equal to 2 pF which is obtained by connecting 30 67.752 fF capacitor in parallel (30 multiplier is chosen, Table 4.3).

Table 4.3. Component values of Equalizer.

Device	**Type**	**Width**	**Length**	**Multiplier**	**Finger**
M15	NMOS	5u	0.4u	2	1
M16	NMOS	5u	0.4u	2	1
X9	309.602 Ω	5u	2u	1	-
X10	309.602 Ω	5u	2u	1	-
X11	309.602 Ω	5u	2u	1	-
X12	309.602 Ω	5u	2u	1	-
X13	309.602 Ω	5u	2u	1	-
X14	309.602 Ω	5u	2u	1	-
X15	44.455 k	20u	0.5u	1	-
X16	44.455 k	20u	0.5u	1	-
X17	11.094 k	5.32u	0.5u	1	-
X33	67.752 fF	20u	-	30	10

Similar to the previous procedure, the components in the Table 4.4 below are selected for the low voltage current mirror. N-12-HSL130E transistor model is used. While the transistors (M19, M20, M21 and M22) have 5.60 um width, 0.4 um length, 1 finger and 1 multiplier, the transistors (M17 and M18) have 20 um width, 0.4 um length, 1 finger and 1 multiplier. In order to obtain 70 μA, 5.60 um width is chosen, since drain current flowing through transistors M17 and M18 is equal to 250 μA and these transistors have 20 um width.

Table 4.4. Component values of low voltage current mirrors.

Device	**Type**	**Width**	**Length**	**Multiplier**	**Finger**
M17	NMOS	20u	0.4u	1	1
M18	NMOS	20u	0.4u	1	1
M19	NMOS	5.60u	0.4u	1	1
M20	NMOS	5.60u	0.4u	1	1
M21	NMOS	5.60u	0.4u	1	1
M22	NMOS	5.60u	0.4u	1	1

Figure 4.16 shows the layout of the equalizer which is drawn using the components in Table 4.3 and 4.4.

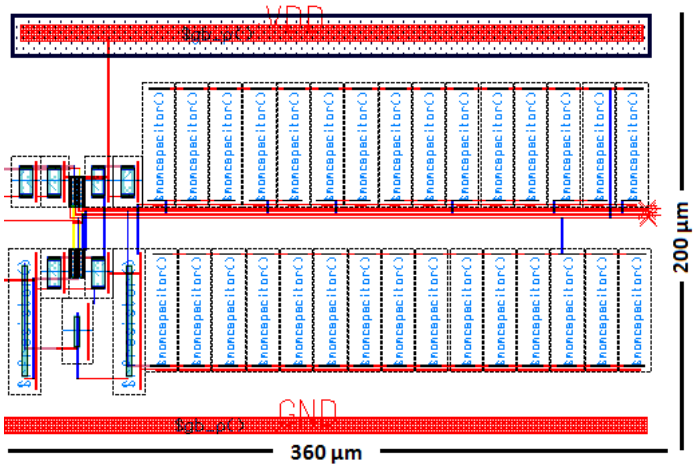


Figure 4.16. Layout of Equalizer circuit.

4.1.4. Integrated CMOS Receiver System

Figure 4.17 shows all the blocks and their connections used in the Integrated CMOS Receiver System. It consists of blocks of photodiode, current mirror inputs, trans-impedance amplifier bias voltages, supply voltage, current mirror, trans-impedance amplifier, equalizer and load.

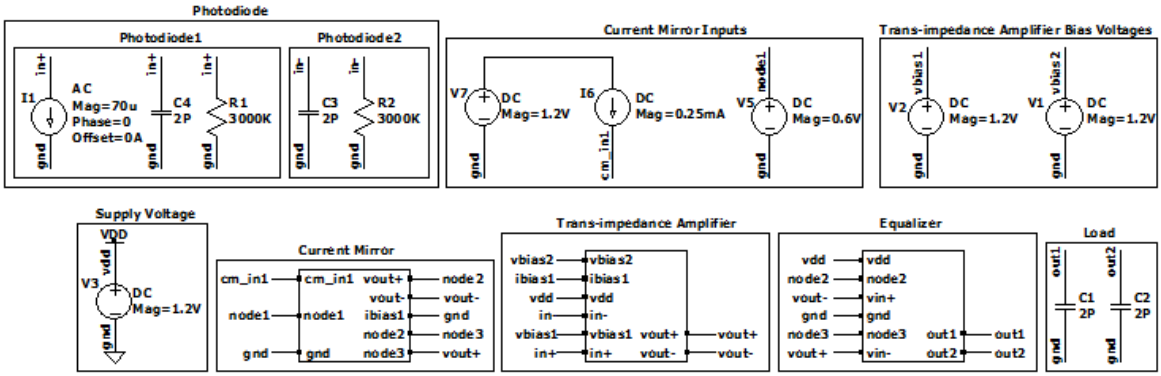


Figure 4.17. Schematic of receiver circuit.

Layout of the whole receiver is given in Figure 4.18 below.

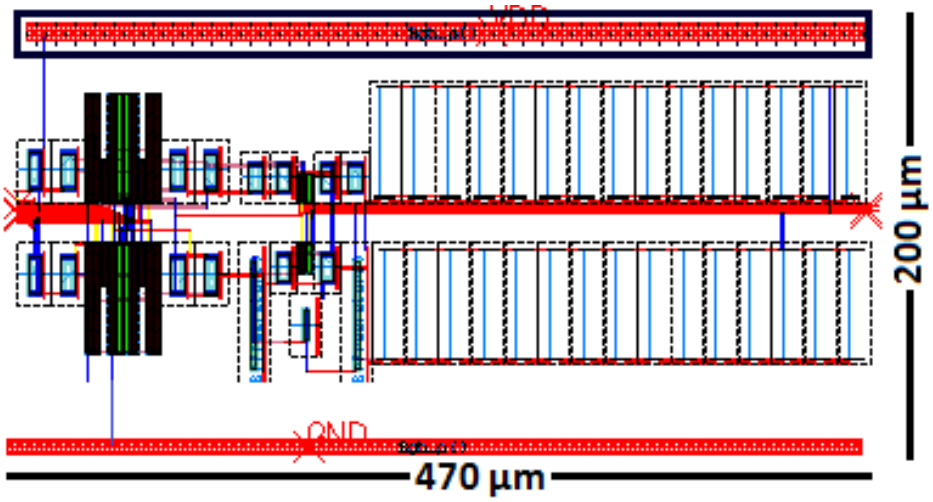


Figure 4.18. Layout of receiver circuit.

4.2. IC Pre-Layout Simulation Results

4.2.1. Photodiode

Figure 4.19 shows the test bench of the photodiode where the first photodiode is modelled with a current source in parallel with a juntion capacitor and shunt resistor. The second photodiode is modelled with a junction capacitor in parallel with a shunt resistor. Values of these components are shown in Figure 4.19.

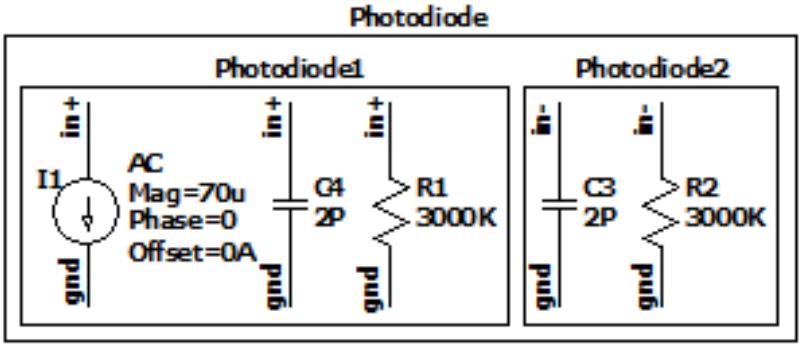


Figure 4.19. Photodiode Testbench.

4.2.2. TIA

Figure 4.20 shows the test bench of the TIA.

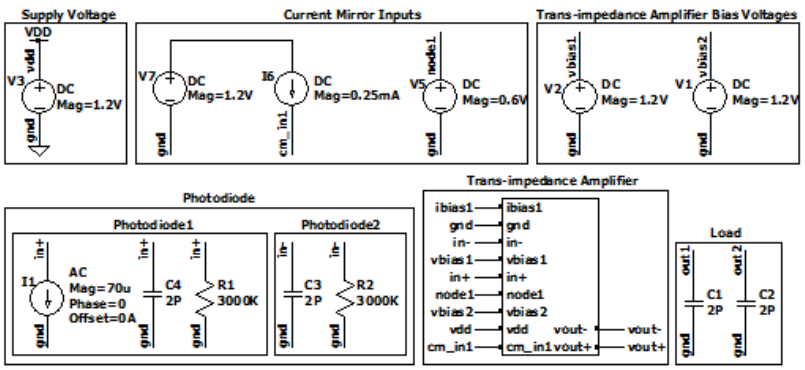


Figure 4.20. Test bench of the TIA for the AC simulation.

Frequency response of the TIA usig a juntion capacitance of 2 pF is shown in Figure 4.21. The 3-dB frequency of the trans-impedance amplifier circuit is 197.56 MHz and the gain is 51.11 dBΩ.

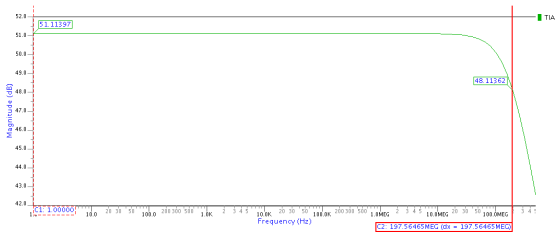
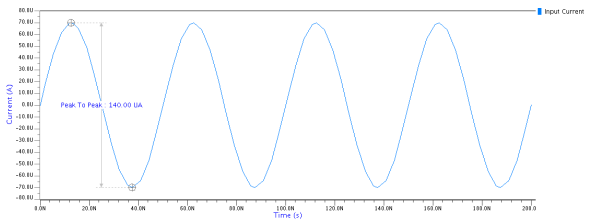
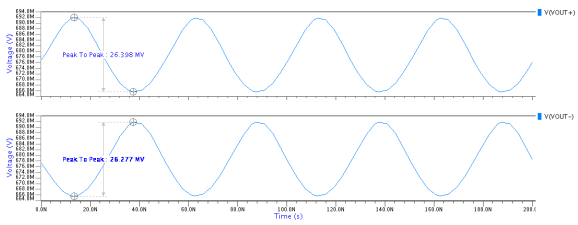


Figure 4.21. AC simulation result of the TIA obtained using 2 pF photodiode junction capacitance.

Peak-to-peak 140 μA current of sinusoidal wave at 20 MHz (Figure 4.22 (a)) is applied to the input of the TIA and the output is examined. Figure 4.22 (b) shows the sinusoidal outputs of the TIA at 20 MHz. The peak-to-peak voltage values of the two outputs are equal to 26.40 mV and 26.28 mV respectively.



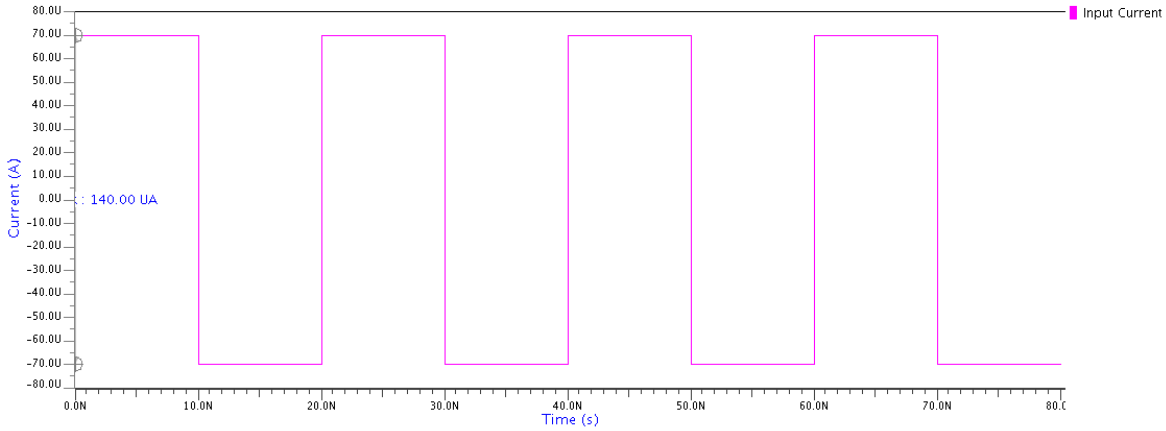
(a)



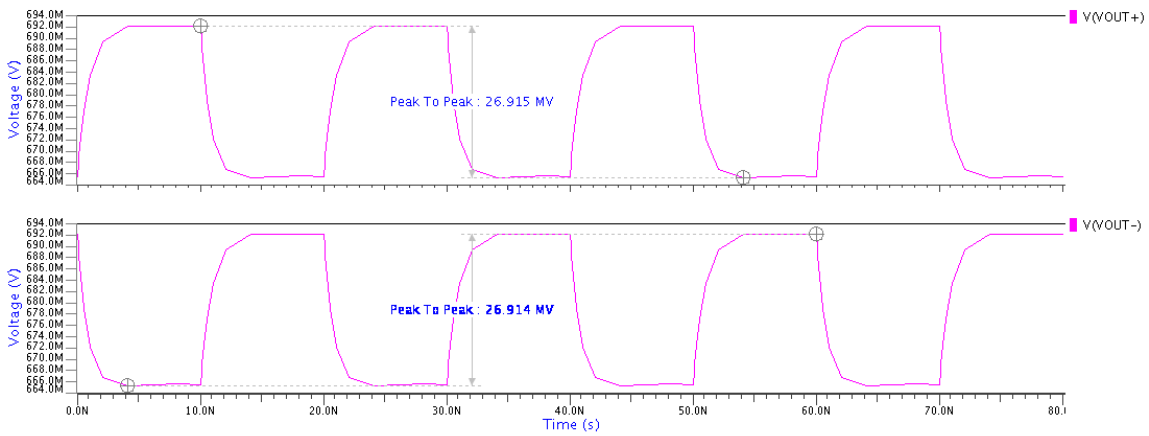
(b)

Figure 4.22. (a) Sinusoidal input current of the TIA at 20 MHz using 2 pF photodiode junction capacitance, (b) Sinusoidal output voltages of the TIA at 20 MHz using 2 pF photodiode junction capacitance.

Figure 4.23 (a) and (b) show the applied peak-to-peak 140 μA square wave input and the outputs at 20 MHz respectively. As can be seen from Figure 4.23 (b), since the frequency is within the bandwidth, the output waveform appears as a square wave.



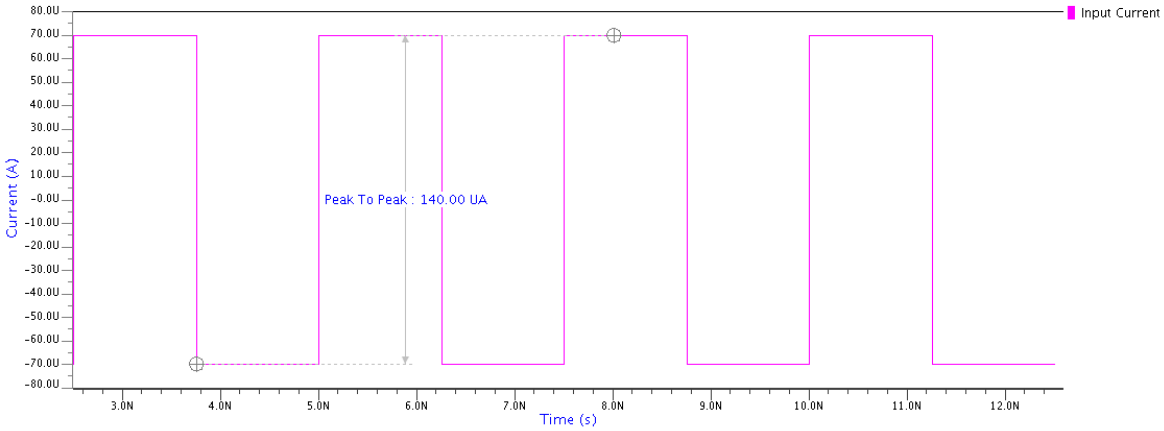
(a)



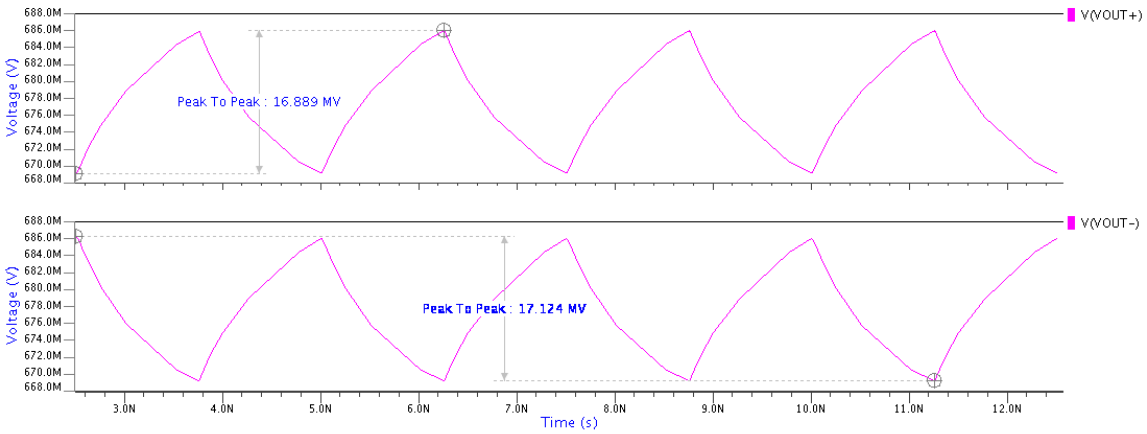
(b)

Figure 4.23. (a) Square wave input of the TIA at 20 MHz using 2 pF photodiode junction capacitance, (b) Output response of the TIA at 20 MHz using 2 pF photodiode junction capacitance.

Figure 4.24 (a) and (b) show the applied peak-to-peak 140 μA square wave input and the outputs at 400 MHz respectively. As can be seen from Figure 4.24 (b), the output waveform is distorted because the frequency is out of the bandwidth.



(a)



(b)

Figure 4.24. (a) Square wave input of the TIA at 400 MHz using 2 pF photodiode junction capacitance, (b) Output response of the TIA at 400 MHz using 2 pF photodiode junction capacitance.

The input and output density of the CMOS TIA is shown in Figure 4.25. This figure is obtained by performing noise analysis in Mentor Graphics.

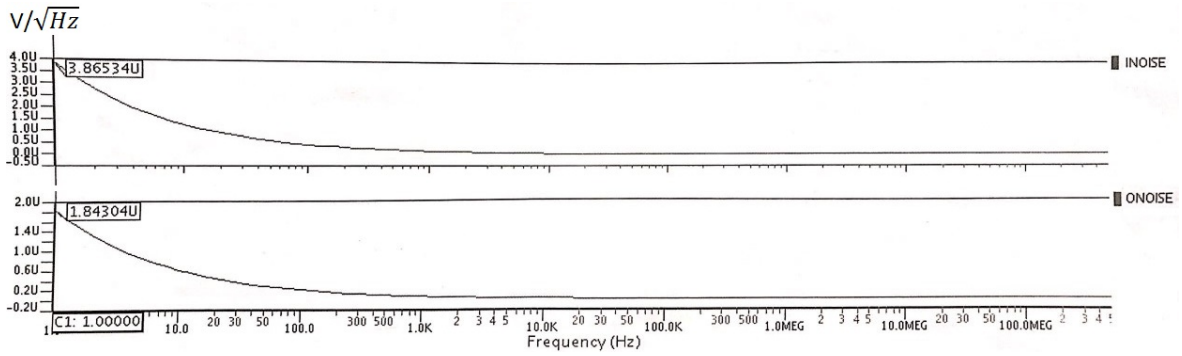


Figure 4.25. The input and output noise density of the CMOS TIA.

Pre-Layout simulation summary of TIA is given in Table 4.5 below.

Table 4.5. Pre-Layout simulation summary of TIA.

Midband gain	51.12 dBΩ
3-dB frequency	197.56 MHz
Rise time	2.8 ns
Fall time	2.8 ns
Bias current	250 μA
Power consumption	0.9 mW
Noise (input referred)	9.2 nA/$\sqrt{Hz}$
Layout area	110 μm x 200 μm

4.2.3. Equalizer

Figure 4.26 shows the test bench of the Equalizer created in Mentor Graphics. It consists of supply voltage, current mirror inputs, TIA bias voltages, photodiode, TIA and load.

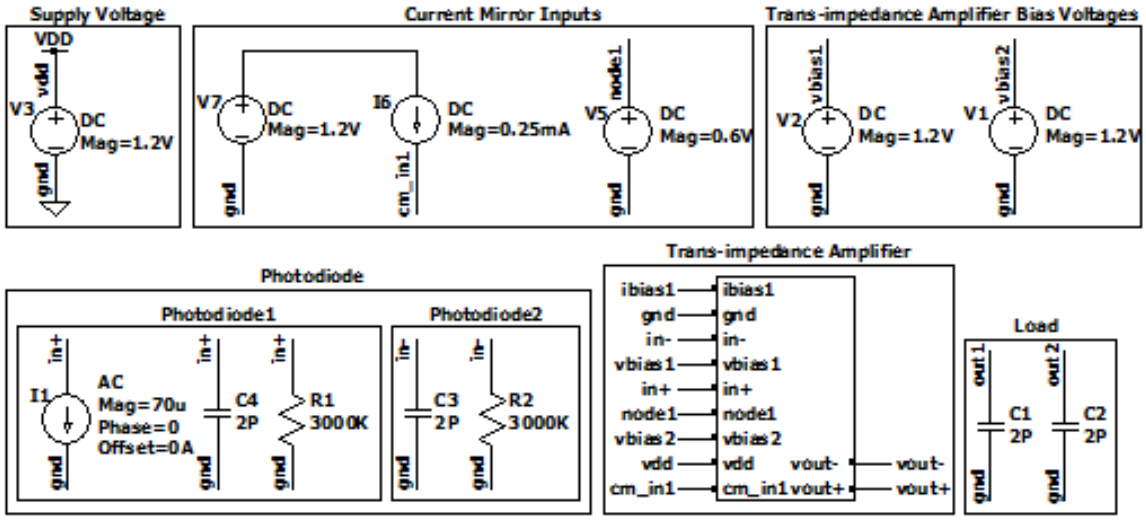


Figure 4.26. Test bench of the Equalizer for the AC simulation

Frequency response of the equalizer is shown in Figure 4.27. The zero frequency is equal to 500.26 kHz. The first and second pole frequencies are equal to 52.59 MHz and 904.56 MHz respectively.

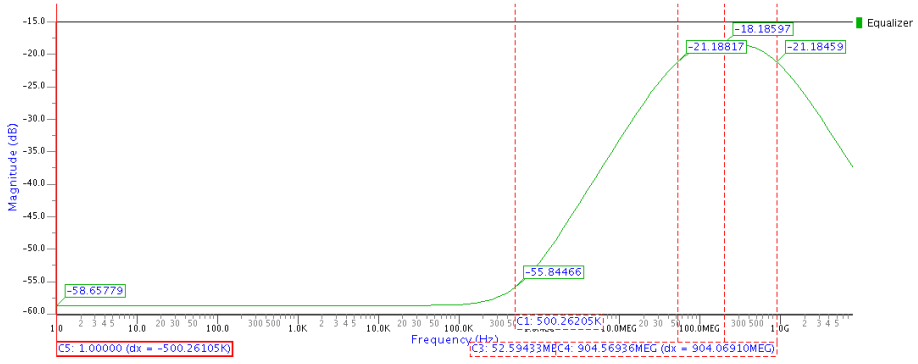
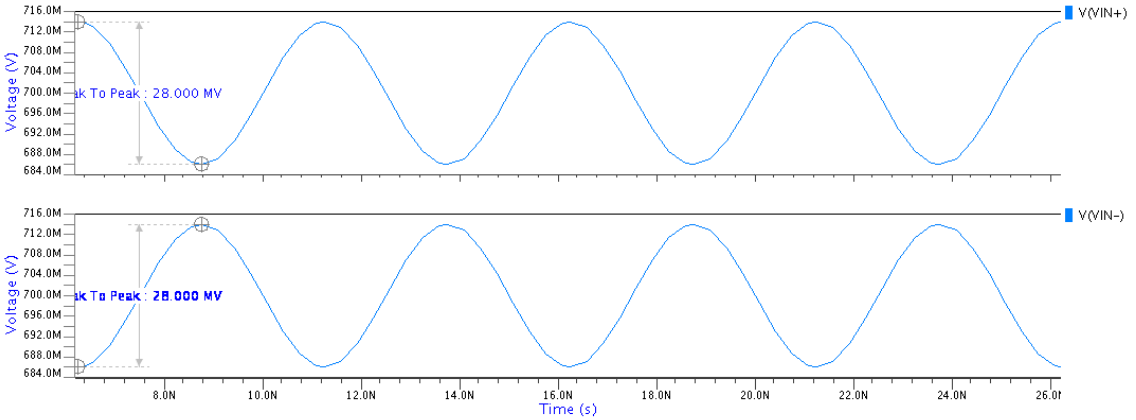
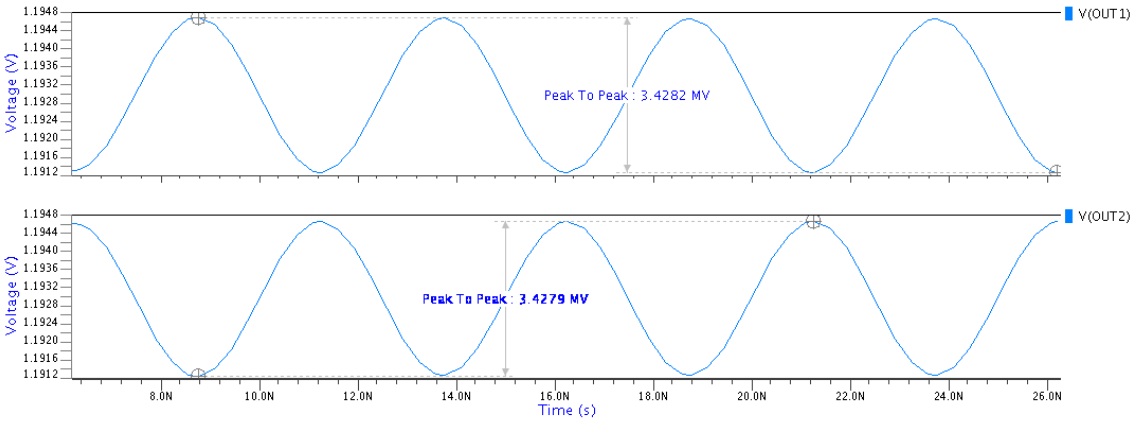


Figure 4.27. AC simulation result of the Equalizer.

Sinusoidal waves of 28 mV at 200 MHz (Figure 4.28 (a)) are applied to the inputs of the Equalizer and the outputs are examined. Figure 4.28 (b) shows the sinusoidal outputs of the Equalizer at 200 MHz. The peak-to-peak voltage values of the two outputs are equal to 3.42 mV and 3.43 mV respectively.



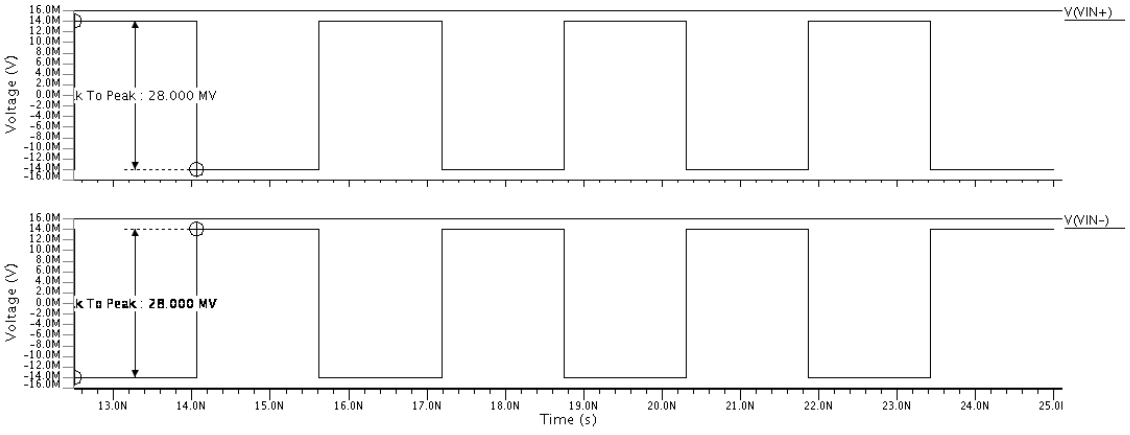
(a)



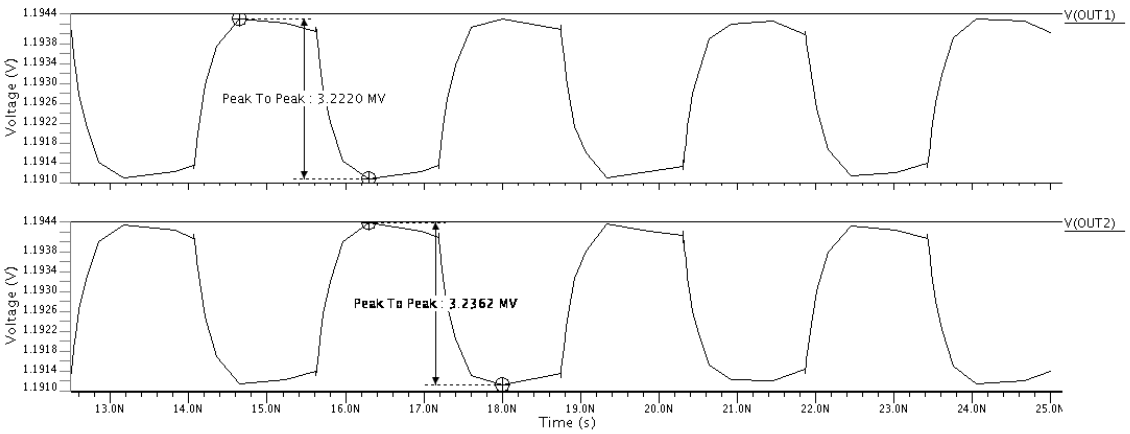
(b)

Figure 4.28. (a) Sinusoidal input voltages of the Equalizer at 200 MHz, (b) Sinusoidal output voltages of the Equalizer at 200 MHz.

Figure 4.29 (a) and (b) show the applied peak-to-peak 28 mV square wave inputs and the relevant outputs of the equalizer at 320 MHz. As can be seen from Figure 4.29 (b), since the frequency is within the bandwidth, the output waveform appears as a square wave.



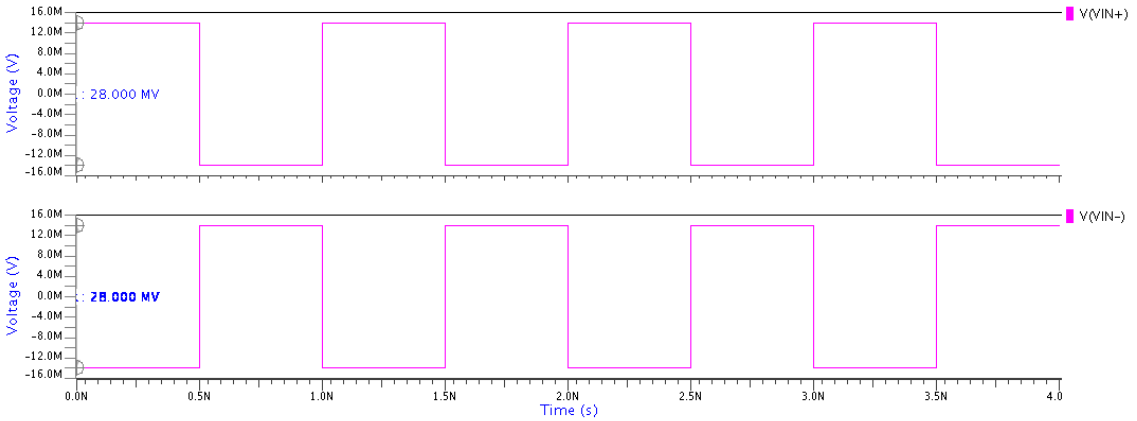
(a)



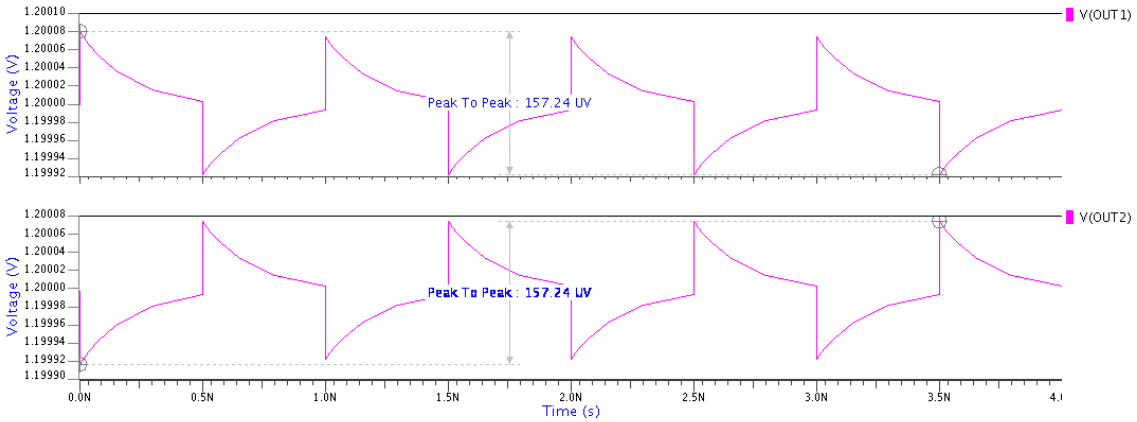
(b)

Figure 4.29. (a) Square wave inputs of the Equalizer at 320 MHz, (b) Square wave outputs of the Equalizer at 320 MHz.

Figure 4.30 (a) and (b) show the applied peak-to-peak 28 mV square inputs and the relevant outputs of the equalizer at 1 GHz respectively. As can be seen from Figure 4.30 (b), the output waveform is distorted because the frequency is out of the bandwidth.



(a)



(b)

Figure 4.30. (a) Square wave inputs of the Equalizer at 1 GHz, (b) Square wave outputs of the Equalizer at 1 GHz.

Pre-Layout simulation summary of Equalizer is shown in Table 4.6 below.

Table 4.6. Pre-Layout simulation summary of Equalizer.

Peaking gain	40.47 dB
Zero frequency	500.26 kHz
First pole frequency	52.59 MHz
Second pole frequency	904.57 MHz
Rise time	0.6 ns
Fall time	0.6 ns
Bias current	70 μA
Power consumption	0.17 mW
Layout area	360 μm x 200 μm

4.2.4. Integrated CMOS Receiver System

Figure 4.31 shows the test bench of Integrated CMOS Receiver System created in Mentor Graphics. This test bench consists of photodiode, current mirror inputs, TIA bias voltages, supply voltage, current mirror, TIA, equalizer and load.

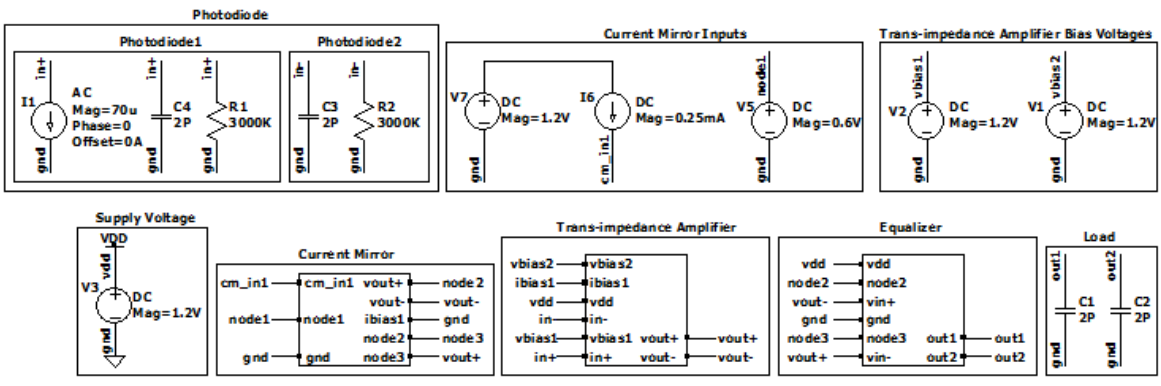


Figure 4.31. Schematic of receiver circuit.

Frequency response of the Integrated CMOS Receiver System, obtained using 2 pF photodiode junction capacitance, is shown in Figure 4.32. The zero frequency is equal to 500.29 kHz. The first and second pole frequencies are equal to 39.41 MHz and 278.18 MHz respectively.

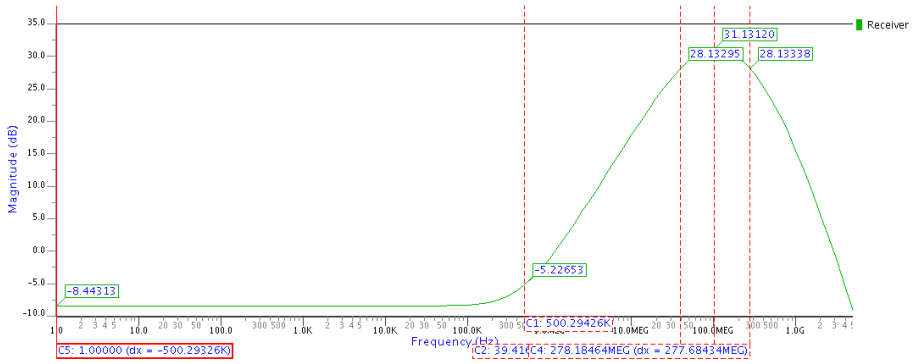
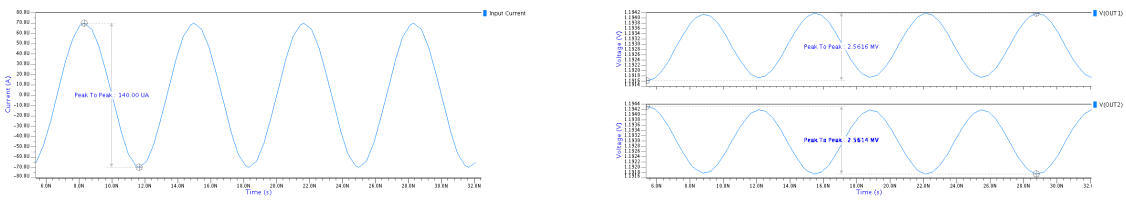


Figure 4.32. AC simulation result of the CMOS Receiver System using 2 pF photodiode capacitance.

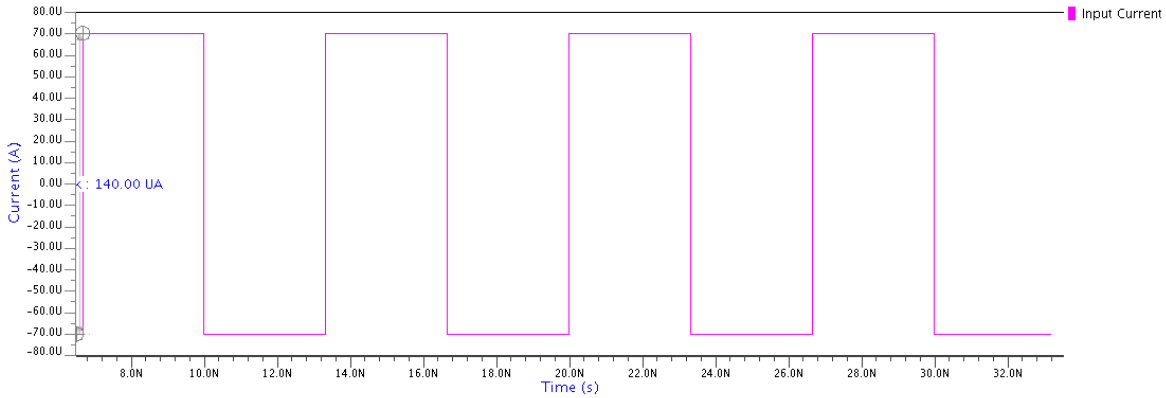
Peak-to-peak 140 μA current of sinusoidal wave at 150 MHz (Figure 4.33 (a)) is applied to the input of the CMOS Receiver System and the outputs are examined. Figure 4.33 (b) shows the sinusoidal outputs of the Integrated CMOS Receiver System at 150 MHz. The peak-to-peak voltage values of the two outputs are equal to 2.56 mV and 2.56 mV respectively.



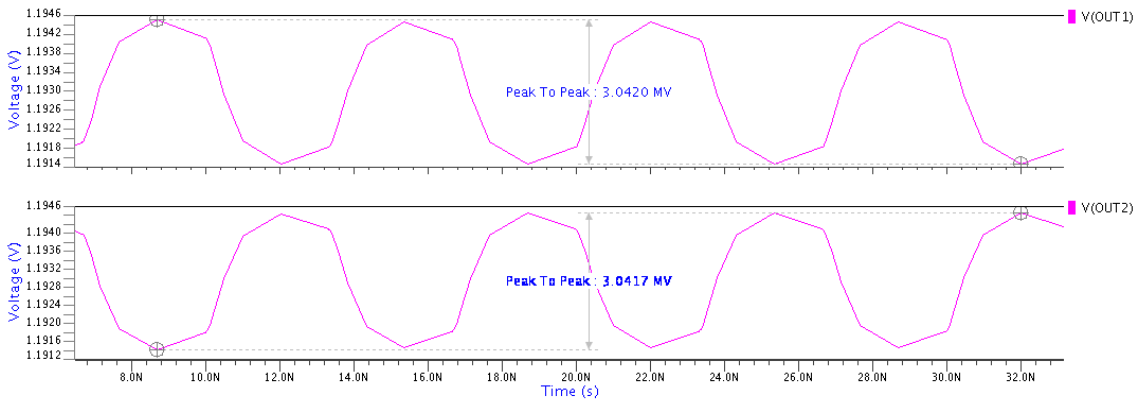
(a) (b)

Figure 4.33. (a) Sinusoidal input current of the Integrated CMOS Receiver System at 150 MHz using 2 pF photodiode junction capacitance, (b) Sinusoidal output voltages of the Integrated CMOS Receiver System at 150 MHz using 2 pF photodiode junction capacitance.

Figure 4.34 (a) and (b) show the applied peak-to-peak 140 μA square wave input and the outputs at 150 MHz respectively. As can be seen from Figure 4.34 (b), since the frequency is within the bandwidth, the output waveform appears as a square wave.



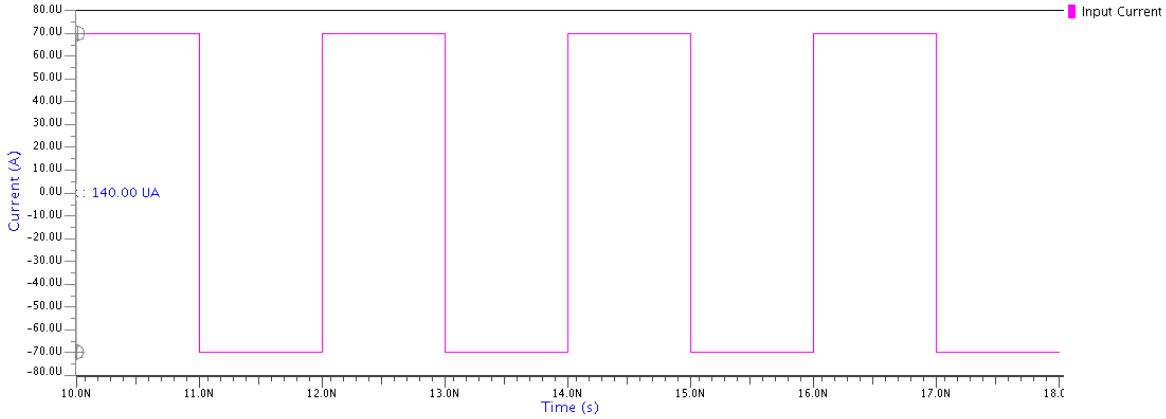
(a)



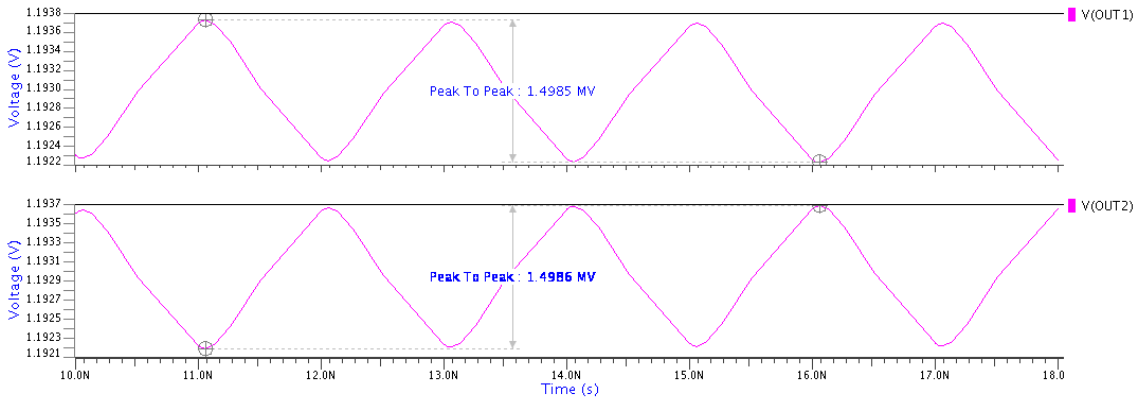
(b)

Figure 4.34. (a) Square wave input of the Integrated CMOS Receiver System at 150 MHz using 2 pF photodiode junction capacitance, (b) Square wave outputs of the Integrated CMOS Receiver System at 150 MHz using 2 pF photodiode junction capacitance.

Figure 4.35 (a) and (b) show the applied peak-to-peak 140 μA square wave input and the outputs at 500 MHz respectively. As can be seen from Figure 4.35 (b), the output waveform is distorted because the frequency is out of the bandwidth.



(a)



(b)

Figure 4.35. (a) Square wave input of the Integrated CMOS Receiver System at 500 MHz using 2 pF photodiode capacitance, (b) Square wave outputs of the Integrated CMOS Receiver System at 500 MHz using 2 pF photodiode junction capacitance.

Pre-Layout simulation summary of Integrated CMOS Receiver System is shown in Table 4.7 below.

Table 4.7. Pre-Layout simulation summary of Integrated CMOS Receiver System.

Peaking gain	39.57 dBΩ
Zero frequency	500.29 kHz
First pole frequency	39.41 MHz
Second pole frequency	278.18 MHz
Rise time	1.1 ns
Fall time	1.1 ns
Bias current	320 μA
Power consumption	1.07 mW
Layout area	470 μm x 200 μm

4.3. IC Post-Layout Simulation Results

4.3.1. Integrated CMOS Receiver System

Frequency response of the Integrated CMOS Receiver System, obtained using 2 pF photodiode capacitance, is shown in Figure 4.36. The zero frequency is equal to 500 kHz. The first and second pole frequencies are equal to 38.97 MHz and 128.83 MHz respectively.

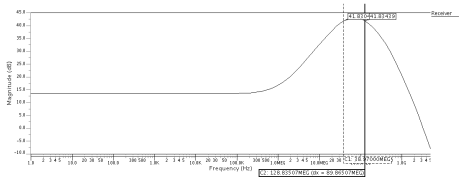
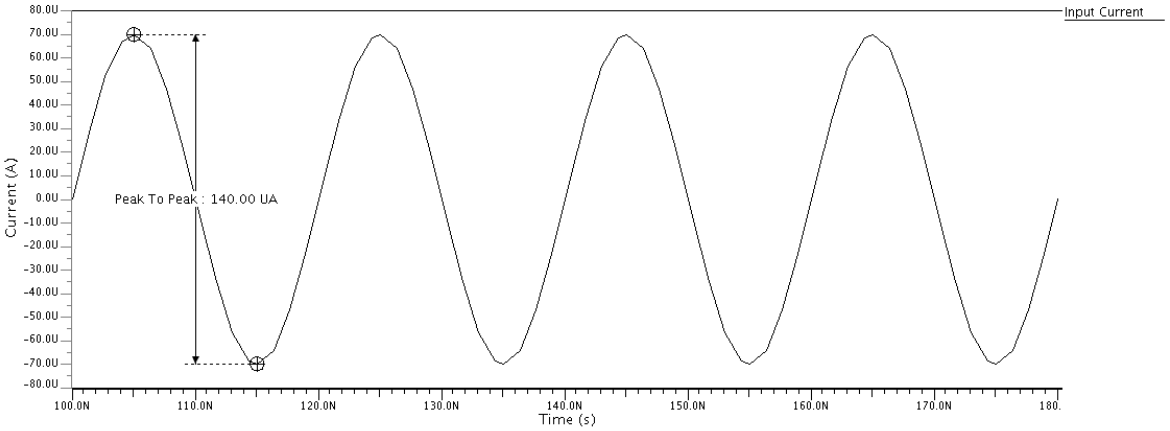
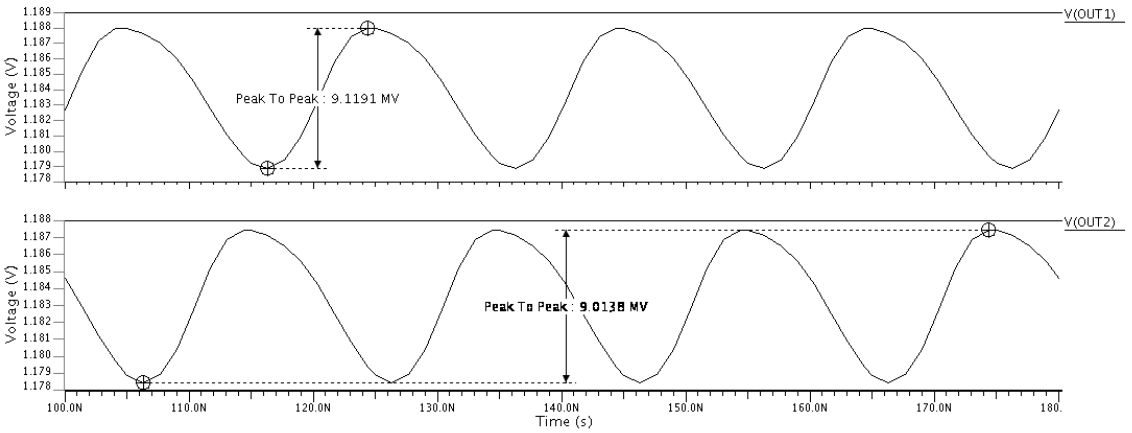


Figure 4.36. AC simulation result of the CMOS Receiver System using 2 pF photodiode junction capacitance.

Peak-to-peak 140 μA current of sinusoid wave at 50 MHz (Figure 4.37 (a)) is applied to the input of the Integrated CMOS Receiver System and the outputs are examined. Figure 4.37 (b) shows the sinusoidal outputs of the Integrated CMOS Receiver System at 50 MHz. The peak-to-peak voltage values of the two outputs are equal to 9.12 mV and 9.02 mV respectively.



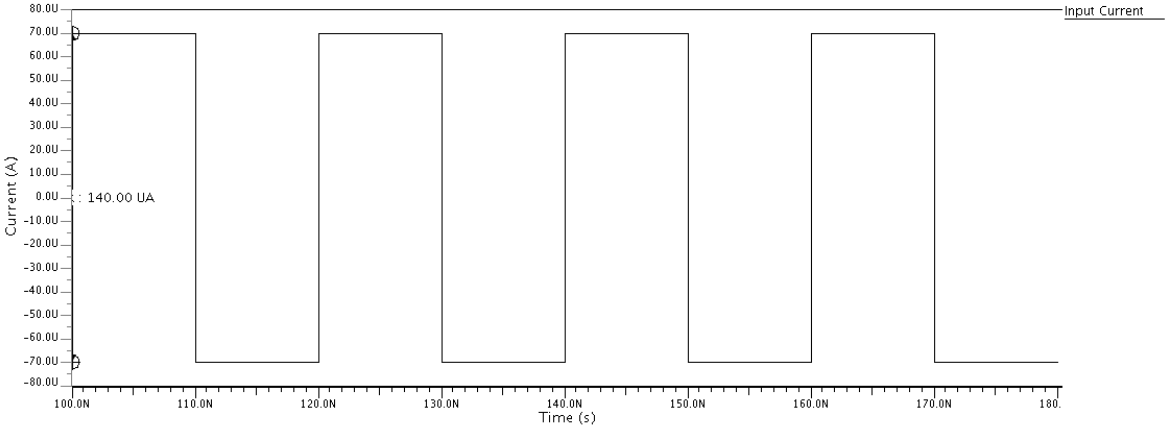
(a)



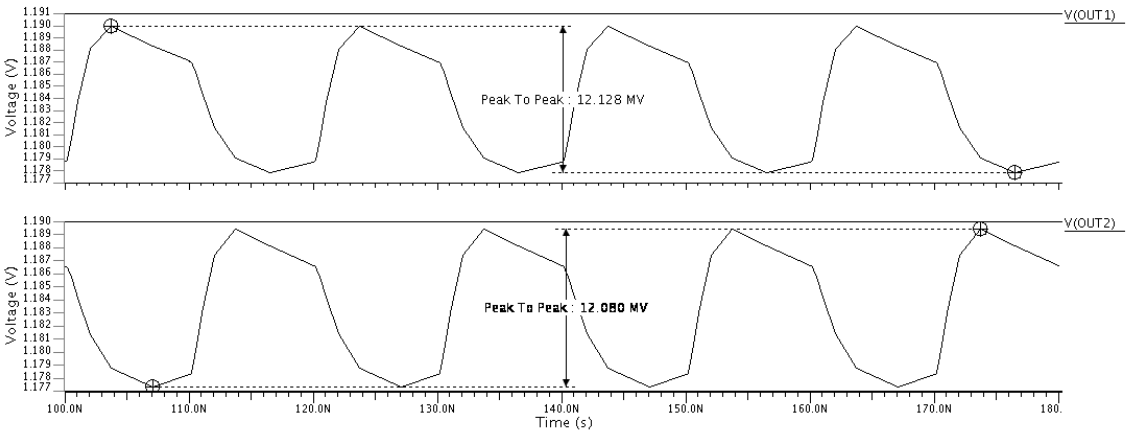
(b)

Figure 4.37. (a) Sinusoidal input current of the Integrated CMOS Receiver System at 50 MHz using 2 pF photodiode junction capacitance, (b) Sinusoidal output voltages of the Integrated CMOS Receiver System at 50 MHz using 2 pF photodiode junction capacitance.

Figure 4.38 (a) and (b) show the applied peak-to-peak 140 μA square wave input and the outputs at 50 MHz respectively. As can be seen from Figure 4.38 (b), since the frequency is within the bandwidth, the output waveform appears as a square wave.



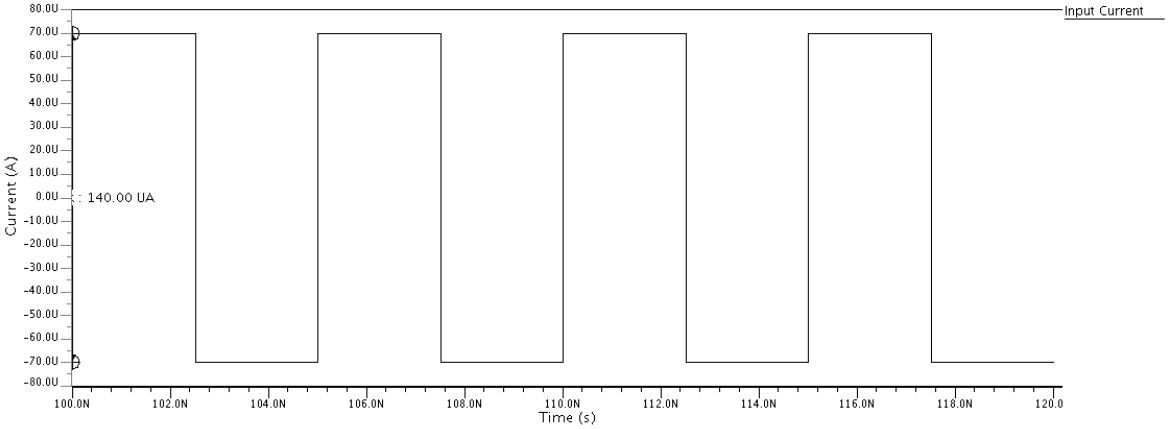
(a)



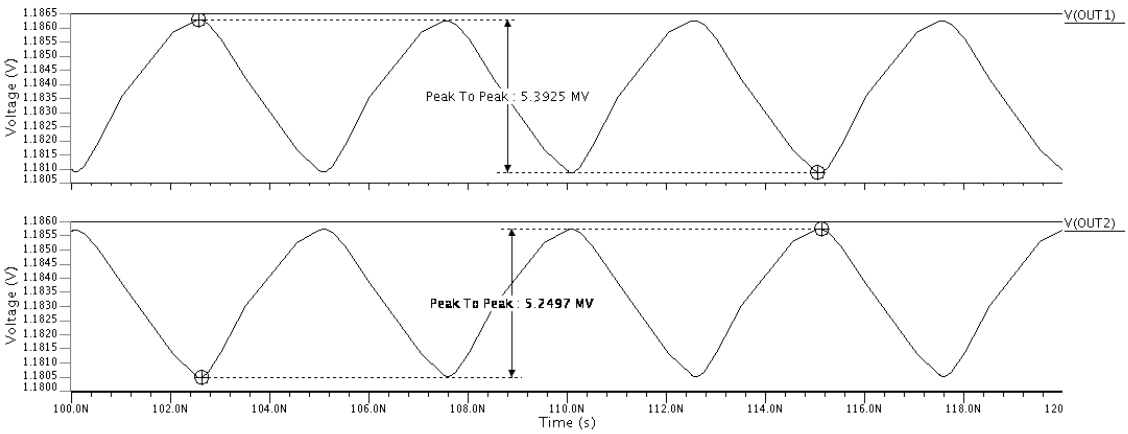
(b)

Figure 4.38. (a) Square wave input of the Integrated CMOS Receiver System at 50 MHz using 2 pF photodiode junction capacitance, (b) Square wave outputs of the Integrated CMOS Receiver System at 50 MHz using 2 pF photodiode junction capacitance.

Figure 4.39 (a) and (b) show the applied peak-to-peak 140 μA square wave input and the outputs at 200 MHz respectively. As can be seen from Figure 4.39 (b), the output waveform is distorted because the frequency is out of the bandwidth.



(a)



(b)

Figure 4.39. (a) Square wave input of the Integrated CMOS Receiver System at 200 MHz using 2 pF photodiode junction capacitance, (b) Square wave outputs of the Integrated CMOS Receiver System at 200 MHz using 2 pF photodiode junction capacitance.

Post-simulation summary of CMOS Receiver System is shown in Table 4.8 on the next page.

Table 4.8. All simulation result of CMOS IC.

		Pre-Layout	Post-Layout
TIA	Midband gain	51.12 dBΩ	-
	3-dB frequency	197.56 MHz	-
	Rise time	2.8 ns	-
	Fall time	2.8 ns	-
	Bias current	250 μA	-
	Power consumption	0.9 mW	-
	Layout area	110 μm x 200 μm	-
	Noise (Input referred)	9.2 nA/$\sqrt{Hz}$	-
Equalizer	Peaking gain	40.47 dB	-
	Zero frequency	500.26 kHz	-
	First pole frequency	52.59 MHz	-
	Second pole frequency	904.57 MHz	-
	Rise time	0.6 ns	-
	Fall time	0.6 ns	-
	Bias current	70 μA	-
	Power consumption	0.17 mW	-
	Layout area	360 μm x 200 μm	-
Integrated CMOS Receiver System	Peaking gain	39.57 dBΩ	26 dBΩ
	Zero frequency	500.29 kHz	500.01 kHz
	First pole frequency	39.41 MHz	38.97 MHz
	Second pole frequency	278.18 MHz	128.83 MHz
	Rise time	1.1 ns	1.5 ns
	Fall time	1.1 ns	1.5 ns
	Bias current	250 μA	250 μA
	Power consumption	1.07 mW	1.07 mW
	Layout area	470 μm x 200 μm	470 μm x 200 μm

5. CONCLUSION AND FUTURE WORK

In this study, firstly, a Trans-impedance Amplifier and Discrete Receiver System circuits were designed using discrete elements. Then they were simulated, produced and measured. A passive equalizer circuit was used in order to increase the limited bandwidth of the LED. It was shown that the limited 3-dB bandwidth of the LED could be increased from 500 kHz to 50.12 MHz by using the passive equalizer circuit.

Secondly, Pre-Layout and Post-Layout simulations for the Integrated CMOS Receiver System were performed. An active CTLE circuit was used in order to increase the limited bandwidth of the LED. It was shown that the limited 3-dB bandwidth of the LED could be increased from 500 kHz to 128.83 MHz by using the active equalizer circuit.

Visible Light Communication has many application areas which are security, augmented reality, localized advertising, underwater communication, intelligent transportation systems and connectivity, sensitive data.

For the above application areas, it is necessary to transmit and receive the data of image, video, audio and message. These data must be transmitted at high speed for high quality.

In this thesis, analog equalization circuits are especially focused on. They were used at the receiver side. As shown in Figure 2.15, the equalization can be done digitally. Furthermore, equalization can be made at both the transmitter and receiver sides.

In order to perform equalization at both transmitter and receiver sides and to transmit and receive image, video, audio and message, the ready-made blocks in SDRs (Software-defined radio) called radio communication systems can be used. These SDRs can be used in a pre-installed setup with signal processing algorithms within

the transceiver units. Once this system is seen to be operational, the necessary circuits can be designed as PCB and Integrated Circuit. Then, this system can be converted into a product for a specific application area. In addition, Intel SOC FPGA's can be used in order to implement the digital filter such as FIR which can be utilized as an equalization technique both at the transmitter and receiver side.

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