DESIGN OF 180nm CMOS IMPULSE RADIO ULTRA WIDEBAND TRANSMITTER FOR BIOMEDICAL IMAGING

by

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ABSTRACT

DESIGN OF 180nm CMOS IMPULSE RADIO ULTRA WIDEBAND TRANSMITTER FOR BIOMEDICAL IMAGING

This thesis is about the design of radio-frequency (RF) integrated circuits for Impulse Radio Ultra-Wideband (IR-UWB) transmitter which is a system of ultra-low power pulse shaping methods for achieving low energy per pulse (EPP). The proposed transmitters are composed of all digital single pulse generator, multiple controlled digital delay lines, a pulse combination circuit, and pulse shaping stages with a pulse shaping capacitor and wire-bond inductor at the output. The generated mono pulse width and the consecutive mono pulse positions are determined by the delay lines. The proposed transmitter architectures are designed in 180 nm CMOS technology, and supply voltage is 1.8V. Use of UWB provides more bandwidth that is necessary for high data rates at 2.4 GHz for biomedical applications. The simulation results show that the energy required to generate the Gaussian mono-cycle, triplet, and quintuplet pulses are 29 pJ, 47 pJ, and 65 pJ respectively at 200 MHz pulse repetition frequency without band pass filter (BPF). The required energies utilizing a BPF to generate output signals are 36 pJ, 54 pJ, and 72 pJ respectively. The motivation of the thesis is to generate the Gaussian quintuplet signal with low power consumption and high data rate without using BPF.

ÖZET

BİYOMEDİKAL GÖRÜNTÜLEME İÇİN 180nm CMOS ULTRA GENİŞ BANTLI DARBE RADYO VERİCİ TASARIMI

Bu tez, darbe başına düşük enerji (EPP) elde etmek için düşük güçlü darbe şekillendirme yöntemlerinin bir sistemi olan Darbe Radyo Ultra Geniş Bant (IR-UWB) verici tasarımı için radyo frekansı (RF) entegre devrelerin tasarımına odaklanmaktadır. Önerilen vericiler, tamamen dijital tek darbe üreteci, çoklu kontrollü dijital gecikme hatları, bir darbe kombinasyon devresi ve bir darbe şekillendirme kapasitörü ve çıkışta tel-bağ indüktörü ile darbe şekillendirme aşamalarından oluşur. Üretilen tekli darbe genişliği ve ardışık tekli darbe konumları gecikme hatları tarafından belirlenir. Önerilen verici mimarileri 180 nm CMOS teknolojisinde tasarlanmıştır ve besleme gerilimi 1.8V'dur. Ultra geniş bant kullanımı, biyomedikal uygulamalar için 2,4 GHz'de yüksek veri hızı için gerekli olan daha fazla bant genişliği sağlar. Simülasyon sonuçları, Gauss tek devirli, üçlü ve beşli darbeli sinyalleri üretmek için gereken enerjinin, bant geçiren filtresi (BPF) olmadan 200 MHz darbe tekrarlama frekansında sırasıyla 29 pJ, 47 pJ ve 65 pJ olduğunu göstermektedir. Çıkış sinyallerini üretmek için bir BPF kullanıldığında gerekli enerjiler sırasıyla 36 pJ, 54 pJ ve 72 pJ'dir. Tezin motivasyonu Gaussian beşli sinyalini düşük güç tüketimiyle ve yüksek veri hızıyla üretimini genş bant filtre kullanılmadan gerçekleştirmektir.

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LIST OF SYMBOLS

C	Capacitor/Capacitance
C_{ps}	Pulse Shaping Capacitor
L	Inductance
L_{wb}	Wire-bond Inductance
T_s	Pulse Repetition Period
η	Efficiency
Ω	Ohm

LIST OF ACRONYMS/ABBREVIATIONS

BW	Bandwidth
BPF	Bandpass filter
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CP	Charge Pump
DC	Direct Current
EPP	Energy Per Pulse
FCC	Federal Communications Commission
IR-UWB	Impulse Radio Ultra Wide Band
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MRI	Magnetic Imaging Resonance
N-MOSFET	N-type Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor
UMC	United Microelectronics Corporation
UWB	Ultra Wide Band
VCDL	Voltage Controlled Delay Line
OOK	On-Off Keying
PAs	Power Amplifiers
PD	Phase Detector
P-MOSFET	P-type Metal Oxide Semiconductor Field Effect Transistor
P-MOS	P-type Metal Oxide Semiconductor
PSD	Power Spectral Density
PW	Pulse Width
RF	Radio Frequency
WBAN	Wireless Body Area Network
WPAN	Wireless Personal Area Network
WSN	Wireless Sensor Network

1. INTRODUCTION

Due to innovations and advances in field of medical diagnosis, medical doctors have been able to identify numerous diseases painlessly since 1960s. Medical imaging modalities can be specified as Radiography, Magnetic Resonance Imaging (MRI), Nuclear Medicine, Tomography, and Ultrasound. These medical imaging methods can be used both for pre-surgery patients and post-surgery patients. Although medical imaging technologies are becoming more popular in order to diagnose various diseases more precisely, the current medical imaging technologies lack high data rate transmission and low power consumption. Also, some technologies have negative effects on human health in real time imaging; therefore, the future imaging technologies need harmless and low-cost methods with more precision, lower power consumption, and high data rate transmission [7].

A portable probe can be designed to display various layers inside the human body by using ultrasound technology. This project is concerned with the design of a transmitter to integrate it in ultrasonic imaging applications using portable probes. This will allow imaging the human body harmlessly and at low cost. Considering the portable nature of the probe system for ultrasonic imaging, this design must be miniaturized, and the power must be supplied by a small battery. Due to the miniaturization, an integrated circuit must be used to implement this project.

In this thesis, the aim is to design an Ultra Wide Band (UWB) transmitter for high data rate transfer and low power consumption. UWB transmitters have a wide range of applications as wireless network systems. In the literature, the UWB transmitter designs are commonly used in a charge-pump (CP) [8] and in wireless body area network (WBAN) technology for transmission of medical data [9]. Additionally, a phase detector (PD) [10] can be used in the UWB transmitters. In this project, analog-digital mixed UWB design is used to transmit an image as a signal to a receiver. Impulse radio ultra-wideband (IR-UWB) systems have a wide range of applications such as low power, high data rate, and robust wireless personal area networks (WPAN), wireless body area networks (WBANs) [11], wireless sensor networks(WSN), ranging, through wall imaging, breath detection, etc [8].

As mentioned before, the ultrasound device requires high efficiency and low power consumption wireless communication circuit. The aim of the proposed design in this thesis is to find solutions to these challenges with pulse combination method that can reduce BW. It can be tuned in the design so that the design meets FCC limits. The thesis study is about UWB transmitters that work at 2.4 GHz with 180nm CMOS technology and that meet the necessary spectral limitations. The UWB transmitter design is robust against any distortion as a result of paramater control such as time delay and pulse width(PW).

This research is organized as follows. Introduction of research is covered in Chapter 1. Background and literature of UWB design techniques is given in Chapter 2. The proposed transmitter architecture, the associated circuitry, and post-layout simulation results are shown in Chapter 3. The tuning algorithm is presented in Chapter 4. This research ends with conclusion and future works in Chapter 5.

2. BACKGROUND

Impulse radio ultra-wideband (IR-UWB) systems have a wide range of applications such as low power, high data rate and robust wireless personal area networks (WPAN), wireless body area networks (WBAN) [12], wireless sensor networks (WSN), ranging, through wall imaging, breath detection, etc [8]. In order to operate at low power, IR-UWB transmitters use very narrow nanosecond pulses. Hence, the transceiver is operated in a very short time period and the power requirement is greatly reduced. Moreover, UWB can also co-exist with other wireless technologies because of its wide bandwidth and low spectrum occupancy.

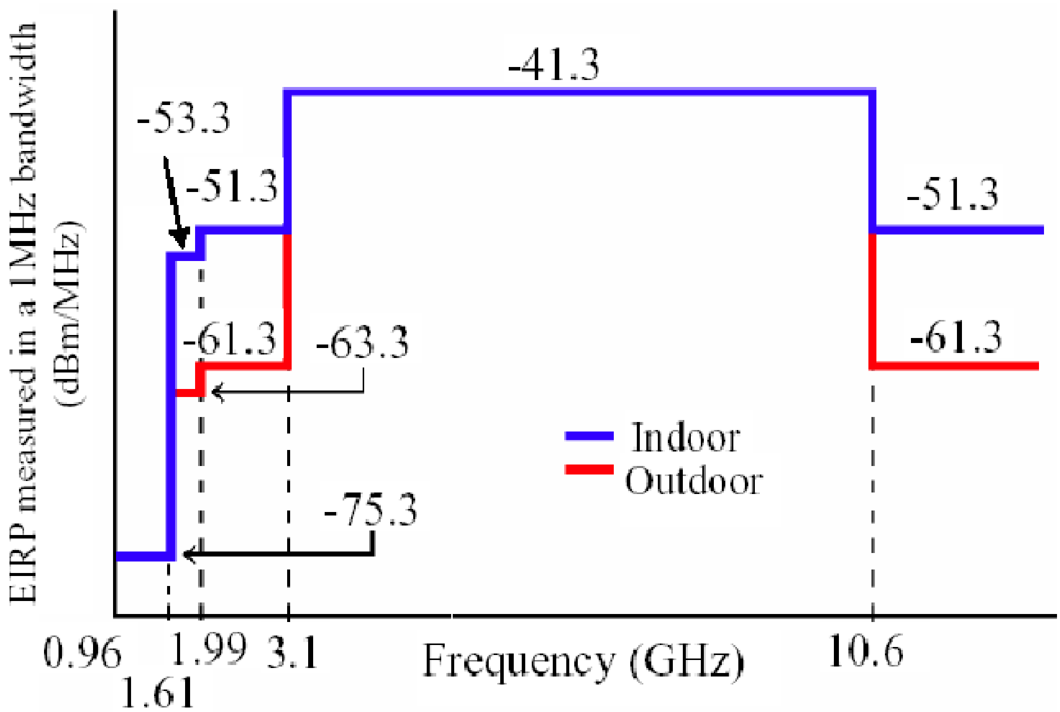

Figure 2.1. UWB spectral mask and FCC Part 15 limits [1].

The bandwidth of UWB signals equals to 500 MHz or must have greater than %20 of its center frequency [8]. The duration of UWB pulses are typically between a few hundred picoseconds and a few nanoseconds. These narrow pulses naturally generate very wide bandwidth in the range of a few GHz in frequency domain as shown in Fig. 2.3. [13]. The 10 dB transmission bandwidth of the UWB transmitter must follow the designated Federal Communications Commission (FCC) UWB spectrum limits [14]. FCC Part 15 limits and the mask in a frequency domain is depicted in Fig. 2.1. Illustration of BW for UWB transmitters can be seen in Fig. 2.2.

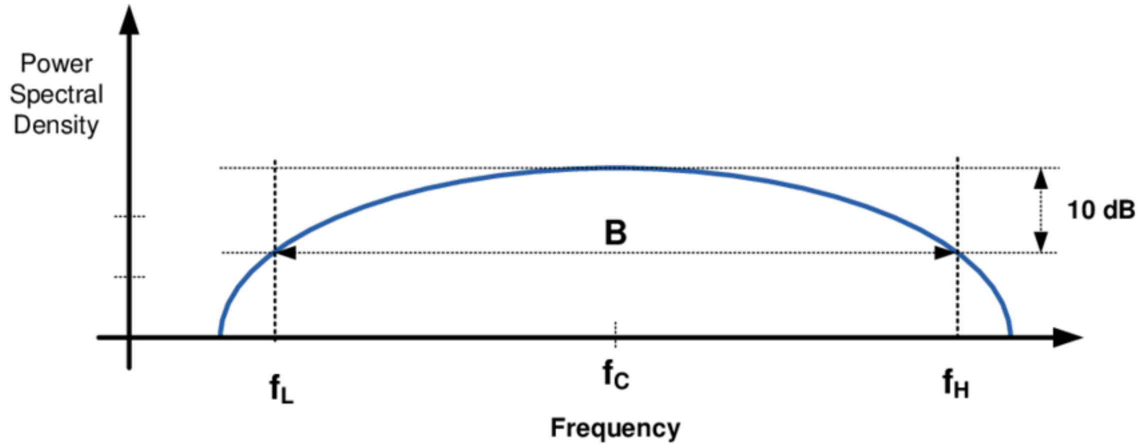

Figure 2.2. Illustration of BW(Bandwidth) of PSD of UWB [2].

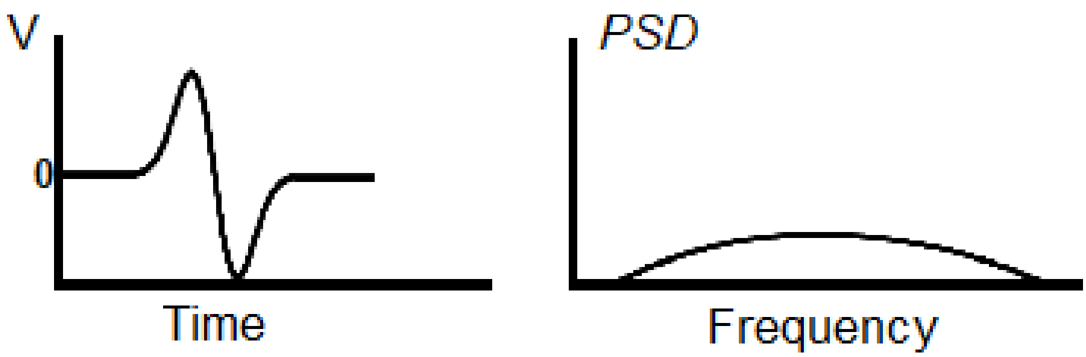

Figure 2.3. A typical Transient UWB pulse (left), PSD in frequency domain (right).

The most common IR-UWB pulse generation techniques in the literature can be divided in three categories; the LC and active loaded oscillators, all digital pulse combination and pulse shaping architectures, and the ring oscillator based pulse generation techniques. A commonly used analog pulse generation method is the LC tank oscillator is switched on and off to generate the required pulse [9]. In LC based pulse generators, large bandwidth and high efficiency can be obtained at the expense of high power consumption [3,15]. On the other hand, digitally controlled ring oscillators, where the ring is only operated for a brief amount of time is an all digital architecture [16]. Although, good EPP values are possible, these circuits have high static power consumption and hence EPP increases for low data rate [17], which is not suitable for applications such as WSN and WBAN that require low standby current. Also, the pulse shapes obtained are not optimal. On the other hand, simple digital circuitry is needed in pulse combination and pulse shaping circuits compared to other methods. The pulses are delayed and combined to generate Gaussian mono-cycle or higher order pulses [11]. Therefore, the very short pulses can be generated in time domain with a low power consumption and high repetition rate.

Some common parameters are required to be selected as a figure of merit to compare various UWB transmitter designs. These parameters can be listed as follows; power consumption, efficiency, minimum feature size of production technology, data rate, peak to peak output voltage signal on a 50 ohm antenna, and EPP(Energy Per Pulse).

EPP can be calculated as:

$$EPP = P_{avg} * T_s \tag{2.1}$$

where T_s is pulse repetition period.

The efficiency, η can be calculated as:

$$\eta = \frac{OutputPeakPower \times PulseWidth(J)}{DCEnergyConsumptionPerPulse(J/Pulse)} \tag{2.2}$$

2.1. UWB Gaussian Pulse Shaping Technique

There are several methods for generating UWB pulses, the sole purpose of which is to develop designs to generate and transmit power within FCC limits. Although the structures of the UWB designs differ in each, the whole aim is to produce Gaussian mono-cycle pulses or their derivatives. Filters are also used to fit PSD of the output signal into FCC limits. The bandwidth can be increased to lower the power consumption which can be achieved by reducing the effective time interval of the pulse in the transient. It is known that when pulse width is reduced, the frequency domain representation is expanded. The ratio of the energy of the pulse produced to the energy consumed by the whole system is called efficiency because it is very important to know how much extra power the system consumes to produce output pulse and is often used as a figure of merit to compare with other UWB transmitter designs.

Gaussian pulse shaping is the most frequently used method for very low power consumption. However, it is not as good as the LC oscillator method in terms of efficiency. Nevertheless it enables us to reach much larger BW. On the other hand, it is also difficult to attain a high peak to peak output signal voltage by using the pulse shaping method. It has a pulse shaping capacitor charged and discharged by using control pulses with different transient positions, thus it provides a Gaussian mono-cycle. Another critical point of the pulse shaping method is that each size of production technology has different mobilities such as 130nm and 180nm technologies. Generally, different fabrication technologies have different DC source values. Because of this, the limitation of the peak to peak voltage depends on value of DC source for pulse shaping method. For instance, generally, VDD is 1.8 V for 180nm technology, and VDD is 1.2 V for 130nm technology.

In the pulse shaping method, there are several critical points to obtain an exact Gaussian mono-cycle. Gaussian mono-cycle and pulse shaping method is shown in Fig 2.4. First, care has to be taken in sizing the PMOS transistor charging the capacitor because this transistor determines the peak voltage of the positive side of Gaussian mono-cycle. The NMOS transistor discharging the capacitor determines the peak voltage of negative side of the Gaussian mono-cycle. As it is known, digital pulses do not form a peak for negative voltages; they can only range between 0 and V_{DD}. By using pulse shaping capacitor, C_{PS}, DC level is blocked and a Gaussian mono-cycle can be produced. Also, positioning of the control pulses of NMOS and PMOS transistor provide smooth and useful UWB pulses. Due to the size of the transistors, C_{PS} value, and positioning of control pulses determine the peak to peak output voltage. The sizing of the PMOS transistor controls the level of positive peak voltage. The sizing of the NMOS transistor controls the level of negative peak voltage. Increasing peak voltage levels depend on the current flow in the transistors. Therefore, large Width/Length ratios are required for high peak voltages. To obtain equal peak voltage values, NMOS and PMOS transistors should be sized taking into account their different mobility values.

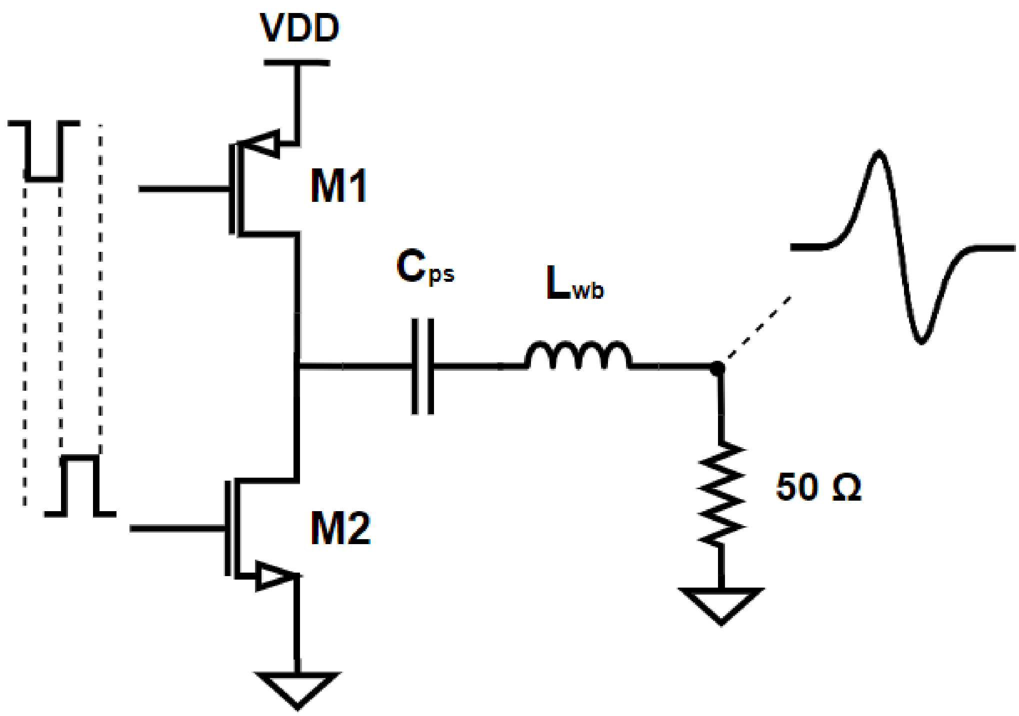

Figure 2.4. Pulse Shaping Method.

2.2. LC Oscillation based UWB Pulse Generation Technique

The most common method used in IR-UWB pulse generation transmitters is the LC oscillator based UWB transmitter method. In this method, an LC tank is used to generate oscillation. LC oscillators generate a sinusoidal signal with a constant frequency due to the LC pair.

As shown in Fig. 2.5, the rising edge of input digital data A triggers a digital pulse generator to generate a nano-second wide digital pulse B. The pulse train B will control the tail current source of the LC oscillator, and consequently an UWB pulse train is generated at C. After amplification by the driver amplifier, the output pulses D will be sent to a matched antenna [3].

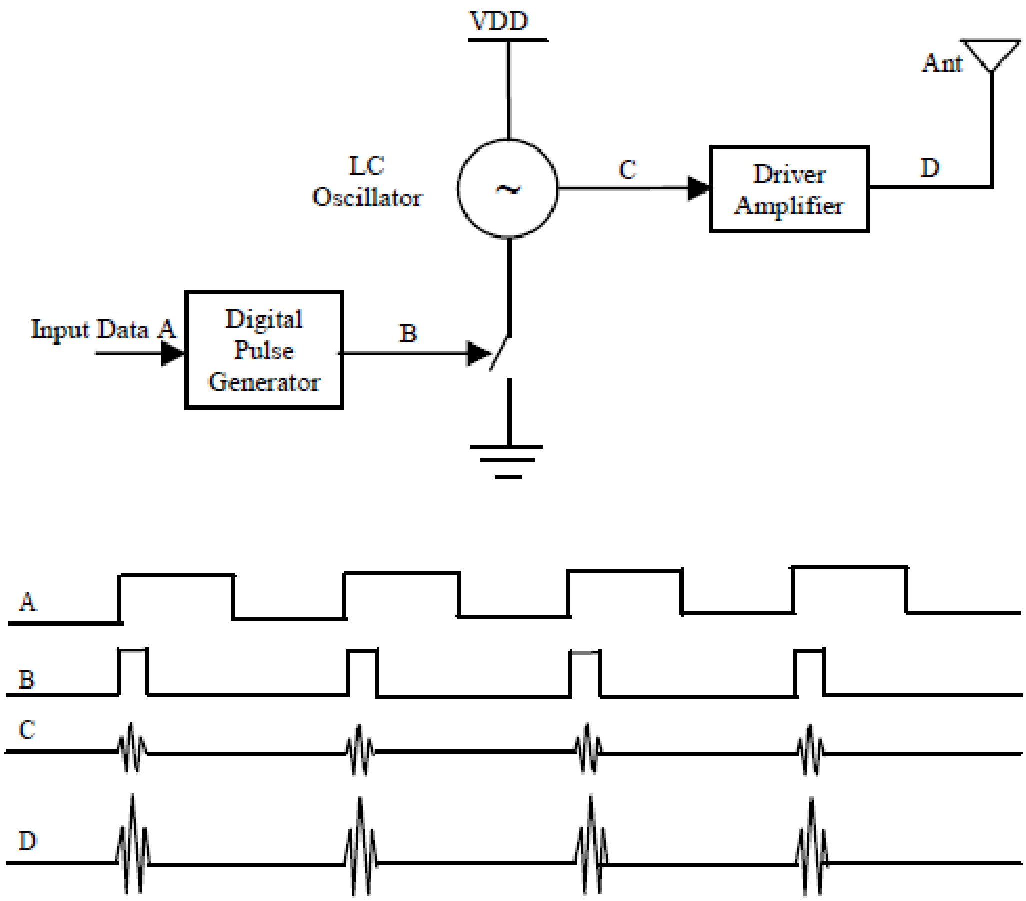

Figure 2.5. LC Oscillator Based UWB Pulse Generation Method [3].

In this type of pulse generators, as depicted in Fig. 2.5, there are several critical points for obtaining the desired high efficiency and a high peak to peak output signal D. The first is that the generated B signal must be able to drive the transistor under the LC tank and driver can be large sized design, so either the transistor must be of small size or the width of the B pulse must be wide. Since it is desired to generate UWB signal, a very large duration oscillation can't be used. For this reason, the transistor should be small, and the start-up time must be fast because the DC power consumption can be low due to fast start-up time of oscillator. Therefore, the efficiency can be high. Additionally, the Driver Amplifier must have high gain and also be able to drive the antenna. Therefore, it is necessary to increase the current at the output stage, which increases the power consumption. There are also several different designs developed using LC oscillator.

2.3. IR-UWB 15th derivative Gaussian pulse generator

There are several methods to produce derivatives of the Gaussian mono-cycle. An effective method for UWB is shown and explained in this section. There are very similar to the UWB pulse generation architectures described in the literature, differ in terms of methods, but the expected spectrum and parameters are almost exactly the same.

Briefly stating the most special contributions of literature: the structure shown in Fig. 2.6 is designed to eliminate the use of filters and PAs like other all-digital tunable transmitters [18–20]. It is a design produced with CMOS 180nm technology and has an adjustable frequency. Fig. 2.6(c) also shows that it complies with FCC limits. In the design, the control circuits consist of a digital structure [4]. This type of pulse combination systems must have a digital tuning system overcome to process variations.

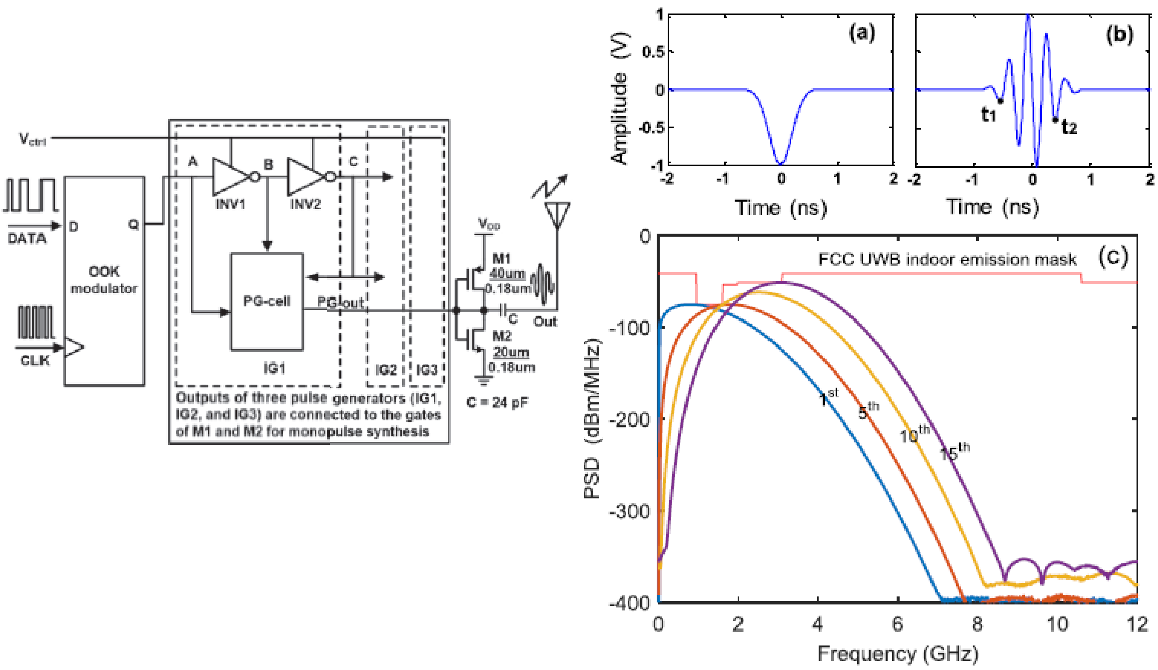

Figure 2.6. In left, block diagram of design. In right part, a Gaussian pulse waveform, (b) an approximate 15th derivative Gaussian pulse waveform with three peaks and four troughs, and (c) spectra of different orders of derivative Gaussian pulses [4].

2.4. Motivation of Thesis

By using the Gaussian pulse-shaping generator output stage mentioned in Section 2.1, two types of pulse combination methods were intended to be developed to generate UWB signal which complies with FCC limits without use of BPF. First method shown in Fig. 2.7 is the single output stage pulse shaping design to increase the pulse width of the output signal, this makes frequency response narrowing by combination of pulses. These combined pulses have equal peak to peak voltage at the output, because of using a single output stage. A single stage has the disadvantage of not being able to adjust all peak voltages individually because all control inputs of the pulse combination stage pass through only single PMOS and NMOS transistors. By using this method, PSD of UWB signal meets FCC limits. The resulting output signals are shown in Fig. 2.7.

The second proposed method is as follows: The pulse positions are adjusted right after the pulse generator and these pulses are combined in multiple pulse shaping stages

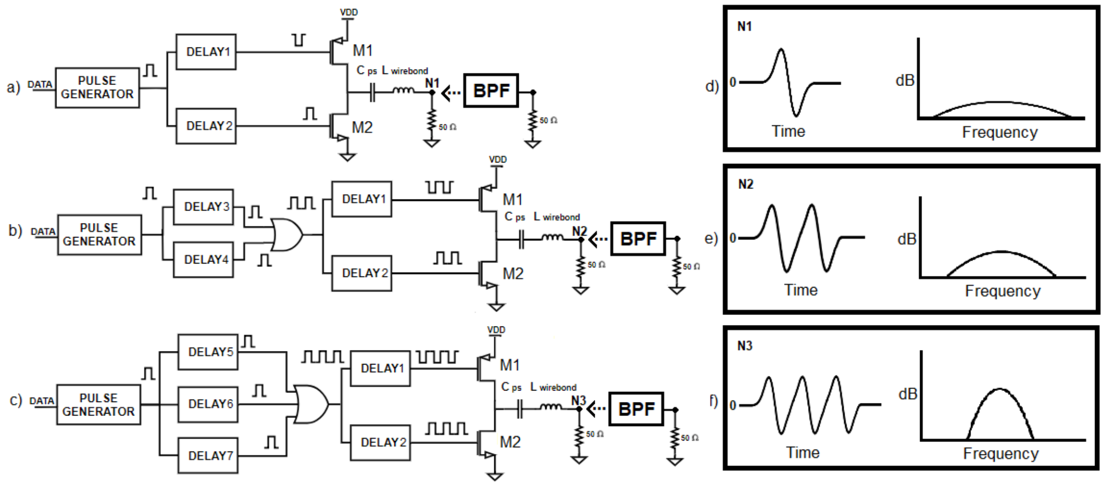

Figure 2.7. Transmitter architectures for the a) Gaussian mono-cycle, b) triplet-cycle, c) quintuplet-cycle pulses and time-frequency response of the d) Gaussian mono-cycle, e) triplet-cycle, f) quintuplet-cycle pulses [5].

to generate multiple output structure as shown in Fig. 2.8, The main objective is to obtain FCC compatible PSD of the output without using a BPF. In the second proposed design in Fig. 2.8, it is predicted that four times as many of digitally controlled delay line blocks and driver stages will be required to provide tuning, and this will increase the power consumption, decrease the efficiency, and increase the area occupied by the transmitter in the microchip. By comparing second proposed design with the first proposed design, it has been seen that the single stage pulse combination UWB design is the best one to implement.

The Gaussian mono-cycle in the proposed output signal of the transmitter can be generated as in Fig. 2.7(a). As mentioned previously in Section 2.1, the proposed pulse combination method has a great advantage to eliminate the use of the BPF because pulse width of signal is increased by combining two or three Gaussian mono-cycle signals, hence reducing the BW of the output signal to meet FCC limits. This combined signal is illustrated in Figure 2.7(b,c). In addition to reducing the BW of the signal, these combined signals have an advantage of increasing the peak-to-peak voltage of transmitted signals.

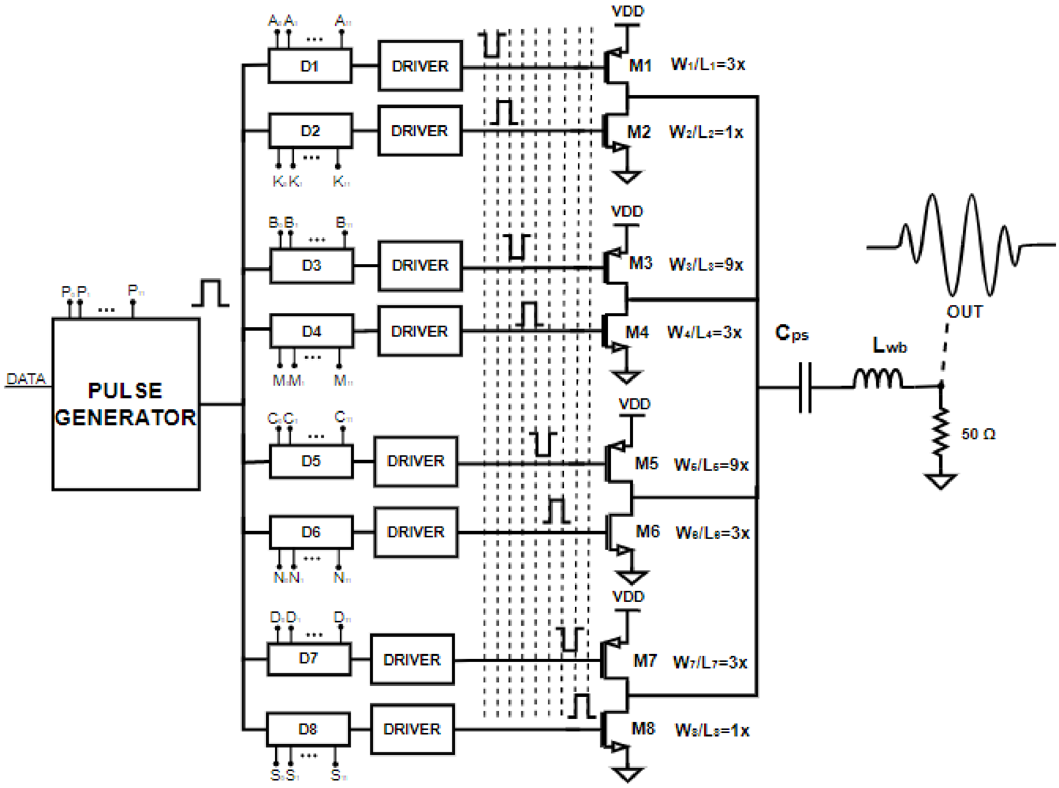

Figure 2.8. Multiple Output Stage Gaussian Pulse Combination Method.

The transient simulation results of the Multiple Output Stage Pulse Combination Method can be depicted in Fig. 2.9. Briefly, the principle of the circuit in Fig. 2.8 based on independent sizing of the PMOS and NMOS transistors on each branch. Therefore, individual peaks in the pulses can be controlled by the sizes and the current flow of charging and discharging of C_{PS}. If all digital controlled and robust circuit is desired, then the number of stages can be increased. Therefore, we can adjust all peaks value with the enabled control pulses by using parallel transistors as in [21]. The control time must be different each transistor to generate desired UWB at output signal in Fig. 2.8. The simulation reslts of the designed circuit for the desired signals are depicted as in Fig. 2.9. The PSD of multiple output stage pulse combination method can be seen in Fig. 2.10. The results prove that the design can be used as an UWB transmitter. However, as mentioned earlier, the complexity of this design greatly reduces its practicality. The main proposed design in the thesis is described in Chapter 3.

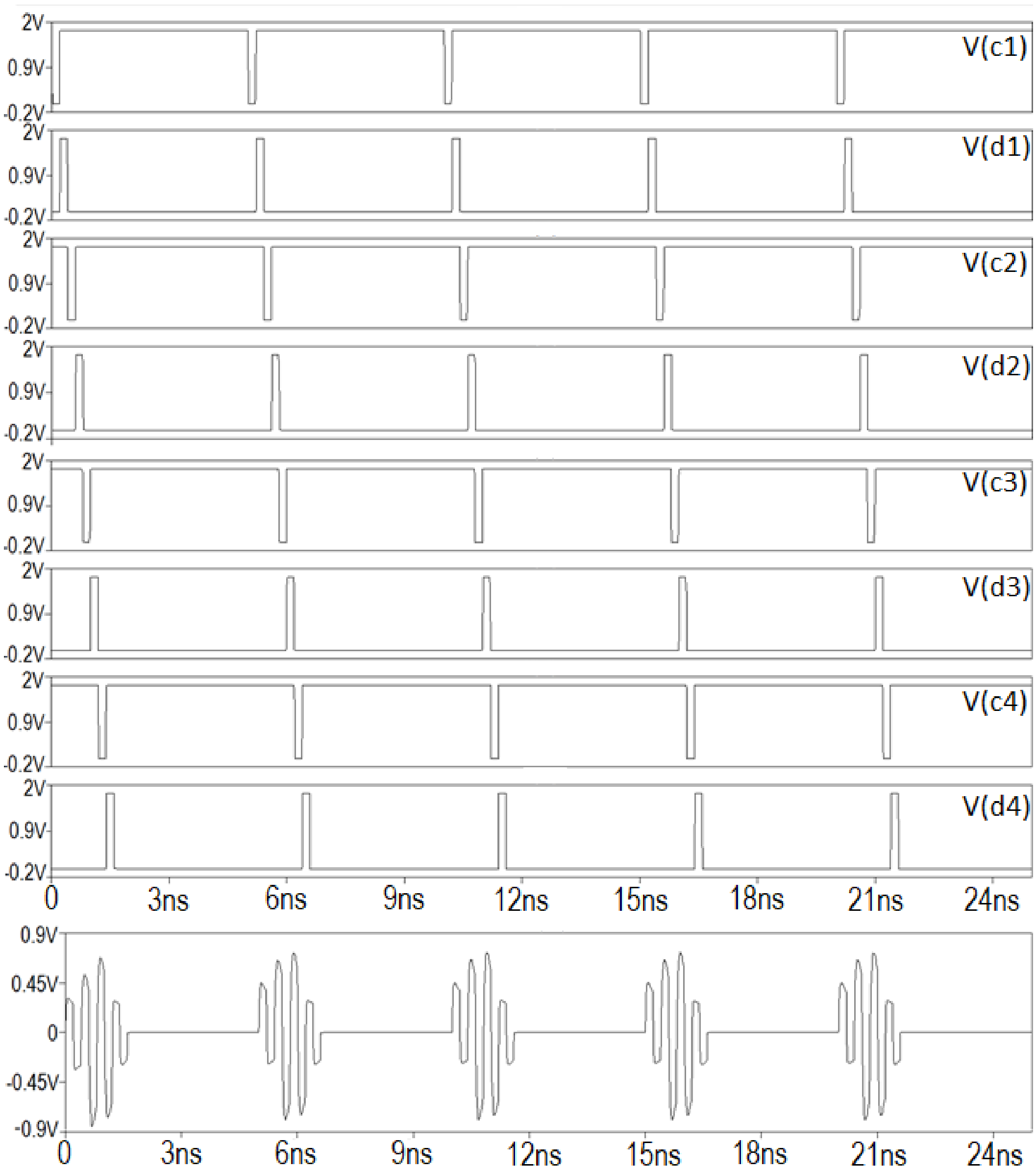

Figure 2.9. Simulation Results of Multiple Output Stage Pulse Combination Method.

The generated UWB pulse is a Gaussian mono-cycle signal which is then band pass filtered. It is a significant part of the project to compare each architecture to choose the most suitable one in the project. The BPF can also be used in the design, which generates combination of two or three Gaussian mono-cycle to obtain higher peak to peak voltage for the desired output UWB signal. In order to reduce the power consumption, enable input is used for switching each signal after the pulse generator block.

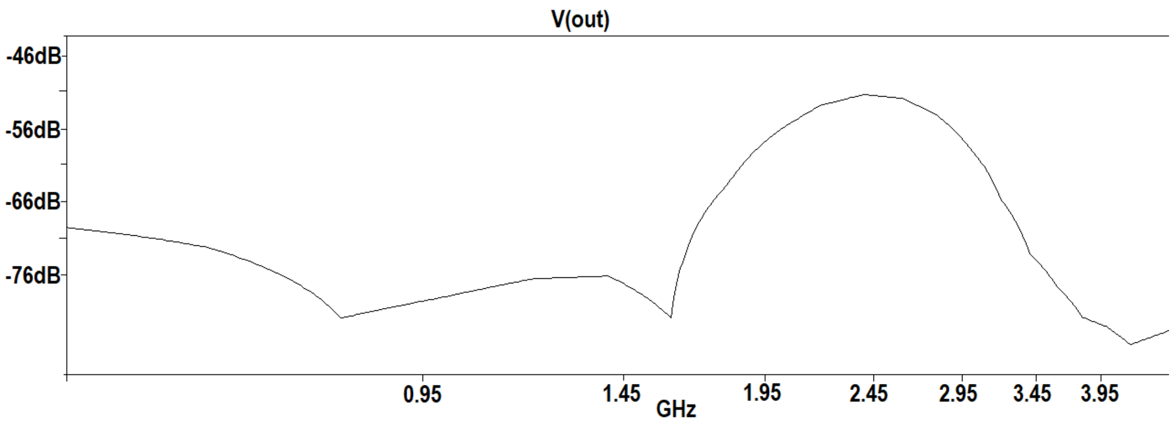

Figure 2.10. PSD of Multiple Output Stage Pulse Combination Method.

On the other hand, the process variation is very important in IC design. Five corners are typically used in Corner analysis. Industry uses two letters to describe the corners: 1^{st} letter is for NMOS device, 2^{nd} letter is for PMOS device. The five classic corners are FF(Fast-Fast), SF(Slow-Fast), SS(Slow-Slow), FS(Fast-Slow), and TT(Typical-Typical) as shown in Fig. 2.11. Processes are tuned to TT. In this thesis, another objective is to be able to compensate for all the process corners to be able to obtain similar performance to TT case.

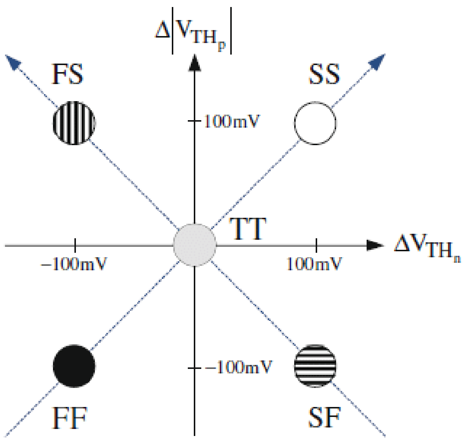

Figure 2.11. Corner process variations.

To have a robust transmitter, pulse positioning technique is very important to compensate for all the process variations. The digital controlled delay lines are used for pulse positioning as presented in Chapter 3.

3. DESIGN AND SIMULATION

In this chapter, the system and the circuit design, and layout design of each block in the thesis, and the simulation results are presented. The simulation results for three different types of Gaussian cycles such as Gaussian mono-cycle, triplet-cycle, and quintuplet-cycle are given. Both transient simulations and the power spectral densities of all three IR-UWB output signals are depicted and explained in the figures. The sub-blocks of all systems are explained in respective sub-sections and the simulation results of the sub-blocks are shown as well. Moreover, the entire system has been implemented in UMC 180 nm technology by using Mentor Graphics CAD tool.

3.1. Proposed IR-UWB Transmitter System Design

The generation of Gaussian mono-cycle is good way to obtain for high data rate and wide band transmitter with On-Off Keying (OOK). The designs must follow the FCC limits [14]. Many UWB transmitters in the literature utilize internal or external filters to generate pulses that comply with the FCC limits. In this thesis, we propose a new approach in designing pulse combination transmitter that relaxes and even removes the BPF requirement to comply with FCC mask by increasing the order of Gaussian pulses in time domain. The method is developed by combining multiple Gaussian mono-cycles consecutively to reduce bandwidth. In order to find the optimum number of cycles required for a specific application, a flexible transmitter design is made to increase the number of cycles. UWB Gaussian mono-cycle has bandwidth exceeding the FCC limits. Although UWB Gaussian quintuplet-cycle can achieve FCC limits, power consumption rises to 13 mW at 200 Mbps data-rate. Also, Gaussian mono-cycle has 5.9 mW power consumption at 200 Mbps, and Gaussian triplet-cycle design has 9.4 mW power consumption at 200 Mbps. In order to obtain low power transmission without requiring band pass filtered transmitter architecture, Gaussian triplet-cycle and quintuplet-cycle can be suitable for FCC limits. Moreover, Gaussian quintuplet-cycle can be the most efficient for 2.4 GHz application. We choose this center frequency because the most of the medical applications are designed at 2.4 GHz center frequency.

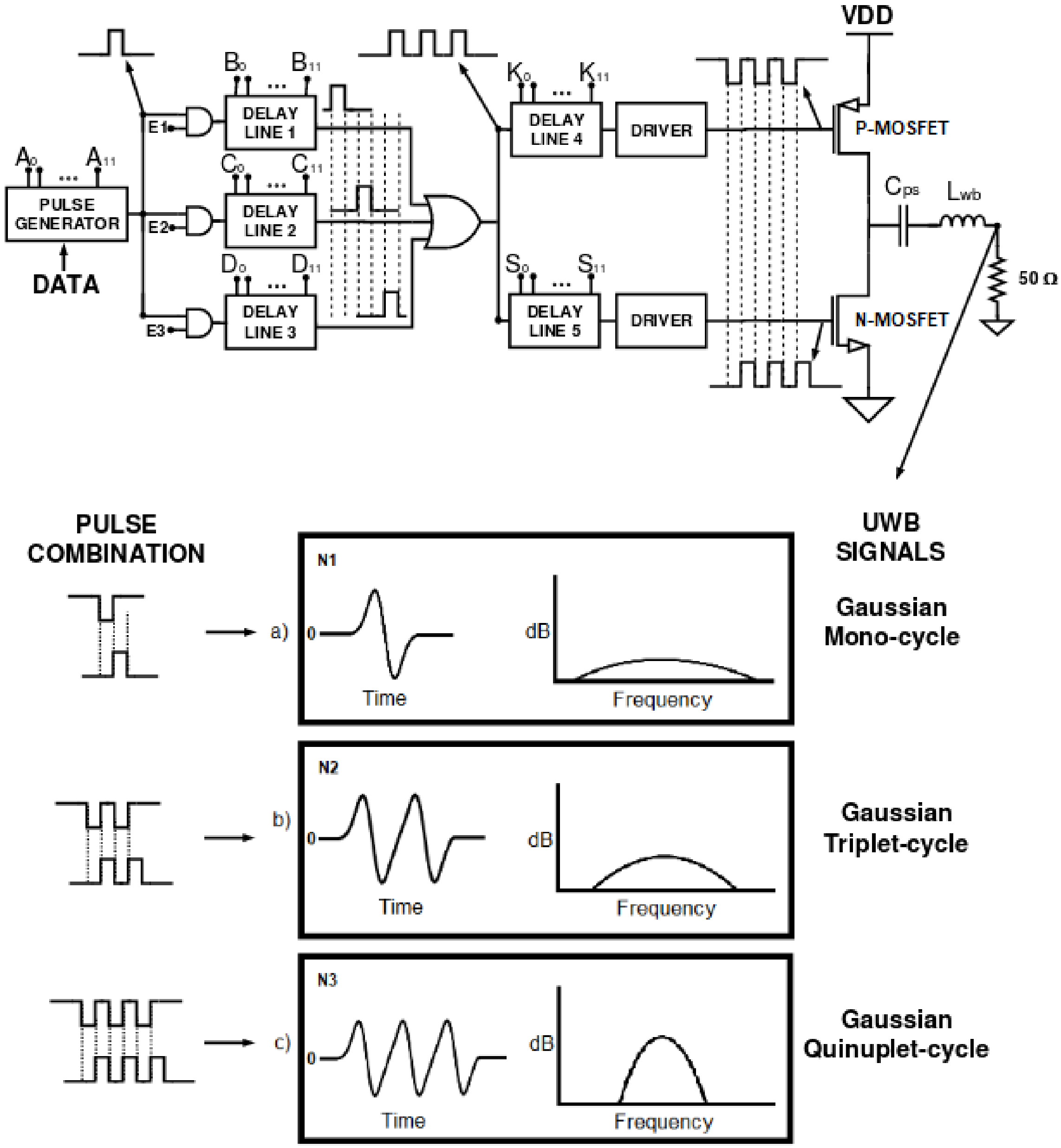

Figure 3.1. Tunable IR-UWB transmitter design.

Initially, the data coming in the form of a square wave triggers the pulse generator. However, the resulting pulse is ready to be enabled at the entrance of three separate digital controlled delay lines: Delay Line 1, 2 and 3. Each activated pulse is retained in the desired transient position, while preserving the PW generated by digital controlled delay lines. As shown in Fig. 3.1, the transient position of the output pulse of Delay

Line 1 can be tuned by the digital codes from B_0 to B_{11}. Additionally, the transient position of output pulse of Delay Line 2 can be tuned by dynamic digital codes from C_0 to C_{11}. Also, the transient position of output pulse of Delay Line 3 can be tuned by dynamic digital codes from D_0 to D_{11}. Then, the pulses are combined by using OR gate. The Gaussian mono-cycle, triplet-cycle and quintuplet-cycle signals can be activated or deactivated by enable, so there will be different UWB output signals on 50 Ω load can be observed with a single circuit. Since the design does not utilize three separate and different circuits, it is an area efficient re-configurable circuit. This will also reduce extra power consumption for this transmitter.

The effect of enabling system could be explained as follows: As shown in Fig. 3.1, enable signals are defined as E1, E2, and E3. When E1 is enabled, only one pulse is generated and Gaussian mono-cycle is obtained, it can be seen in Fig. 3.1(a). When E1 and E2 are enabled, Gaussian triplet-cycle signal is obtained in Fig. 3.1(b) . When all of them are enabled, the Gaussian quintuplet-cycle is generated in Fig. 3.1(c). The time and frequency response of the generated Gaussian mono-cycle, triplet-cycle and quintuplet-cycle can be observed in Fig. 3.1(a), Fig. 3.1(b) and Fig. 3.1(c).

As it can be seen in Fig. 3.1, three different impulses tuned by using Delay Line 1, 2, and 3 are combined by using the OR gate and then connected to two separate current controlled digital delay lines such as Delay Line 4 and 5. An inverted pulse chain is generated at the output of the Delay Line 4 and Driver block in order to drive the P-MOSFET. The Driver(buffer) blocks are necessary due to large P-MOSFET-N-MOSFET gate capacitances at the output stage. In order to avoid N-MOSFET and P-MOSFET turn on at the same time, more delay is introduced to the N-MOSFET driving signal. This ensures low power consumption. If both P-MOSFET and N-MOSFET on the output pulse shaping stage operate at the same transient position, current flow is increased and pulse shape is not suitable for transmitter design, and power consumption is unacceptabley high. Because of the increase of power consumption, efficiency will be reduced and the waveform of desired UWB signal will be distorted. The reason is that current flow can be from the source to the ground through the transistors. A driver is also designed for N-MOSFET at the output stage.

In Fig. 3.1, the circuit at the top is tuning transient position of the control pulses of charging and discharging to generate the desired UWB signals at the output. It depends on Delay Line 4 and 5. These delay line blocks have digitally dynamic codes. For instance, Delay line 4 has K_0 to K_{11} digital control pins to obtain desired pulse position for controlling P-MOSFET to charge pulse shaping capacitor. On the other hand, Delay Line 5 has S_0 to S_{11} digital control pins for tuning pulse position of N-MOSFET to get suitable control pulse for discharging pulse shaping capacitor. The capacitor value is very critical to get desired 2.4 GHz due to constant wire-bond inductance known as 2.2 nH. Pulse shaping capacitor value is set as 2 pF to get 2.4 GHz and to match 50 Ω load by calculating with the equation 3.1.

$$frequency = \frac{1}{2\pi\sqrt{LC}} \tag{3.1}$$

The total width of the P-MOSFET transistor is 240 μm, and the length is 0.18 μm. However, for reducing parasitic capacitance, the number of fingers is chosen as 40 and the multiply number is set as 6. Therefore, P-MOSFET has transistors multiplied by 6 and each transistor has 40 μm width and 40 fingers. In the same way, total width of N-MOSFET is 160 μm, length is 0.18 μm. Also, N-MOSFET has transistors multiplied by 4 and each transistor has 40 μm width and 40 fingers. These values are set in order to decrease the gate capacitances. This will help reduce the size of the inverter chain used at driving these large P-MOSFET and N-MOSFET output stages.

Post-layout transient simulation of UWB Gaussian mono-cycle signal are depicted in Fig. 3.2. Post-layout PSD simulation of UWB Gaussian mono-cycle can be seen in Fig. 3.3. Post-layout transient simulations of UWB Gaussian triplet-cycle signal are depicted in Fig. 3.4. Post-layout PSD simulation of UWB Gaussian triplet-cycle can be seen in Fig. 3.5. Post-layout transient simulations of UWB Gaussian quintuplet-cycle signal are depicted in Fig. 3.6. Post-layout PSD simulation of UWB Gaussian quintuplet-cycle can be seen in Fig. 3.7. The layout of the whole system are shown in Fig. 3.8.

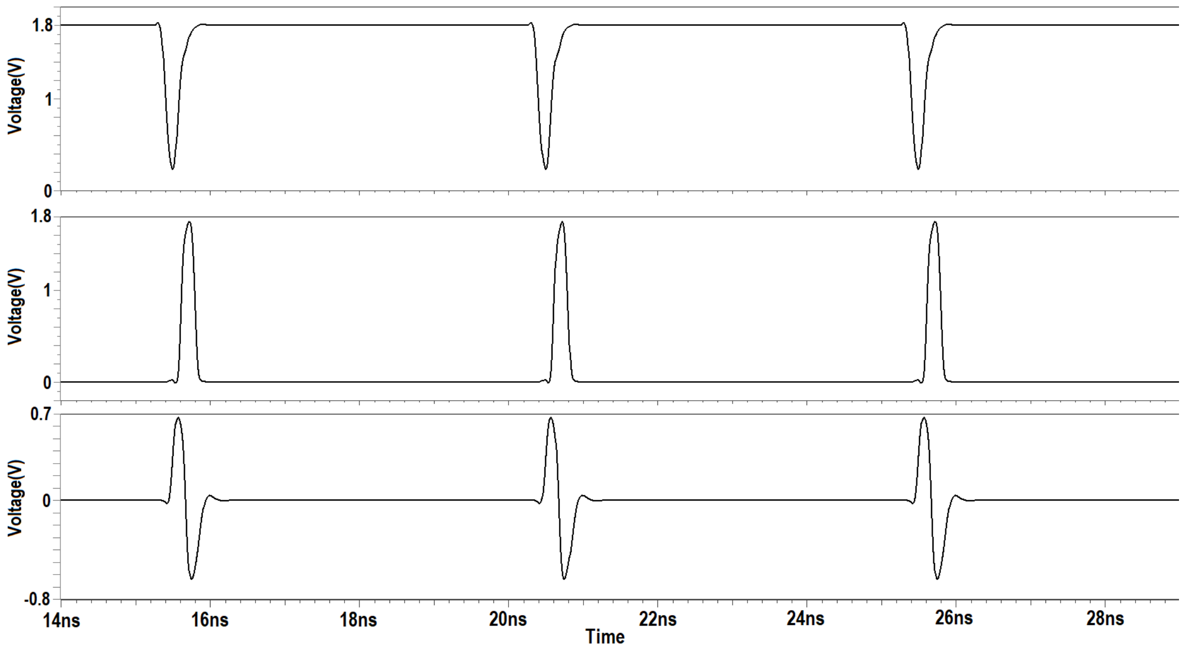

Figure 3.2. Transient simulation result of UWB Gaussian mono-cycle.

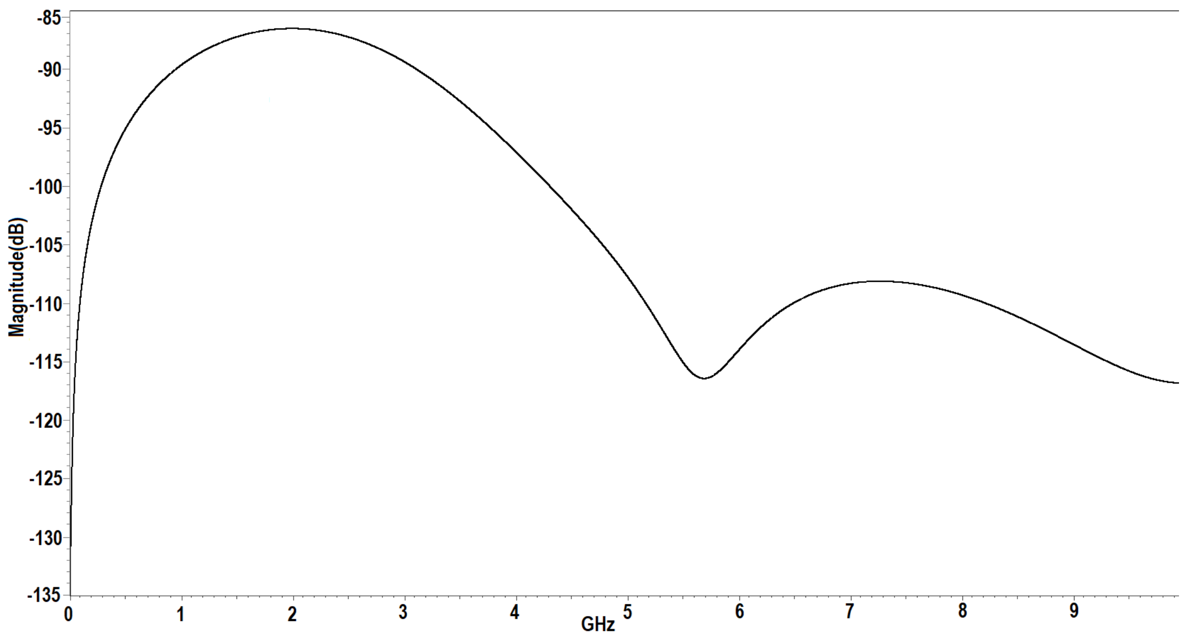

Figure 3.3. PSD of UWB Gaussian mono-cycle.

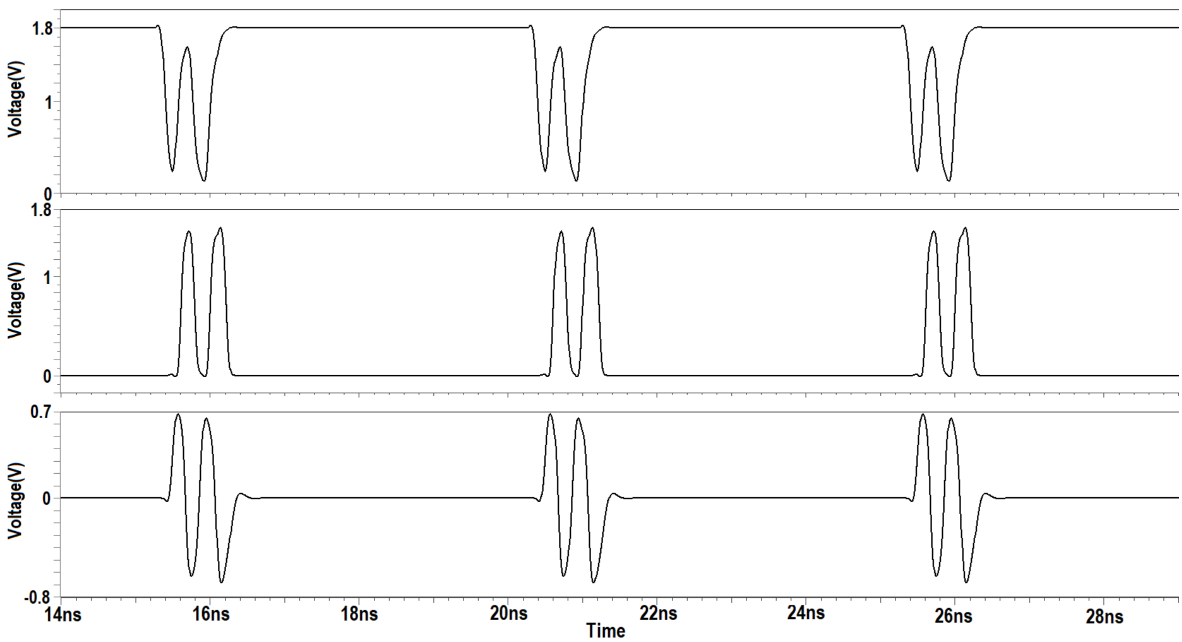

Figure 3.4. Transient simulation result of UWB Gaussian triplet-cycle.

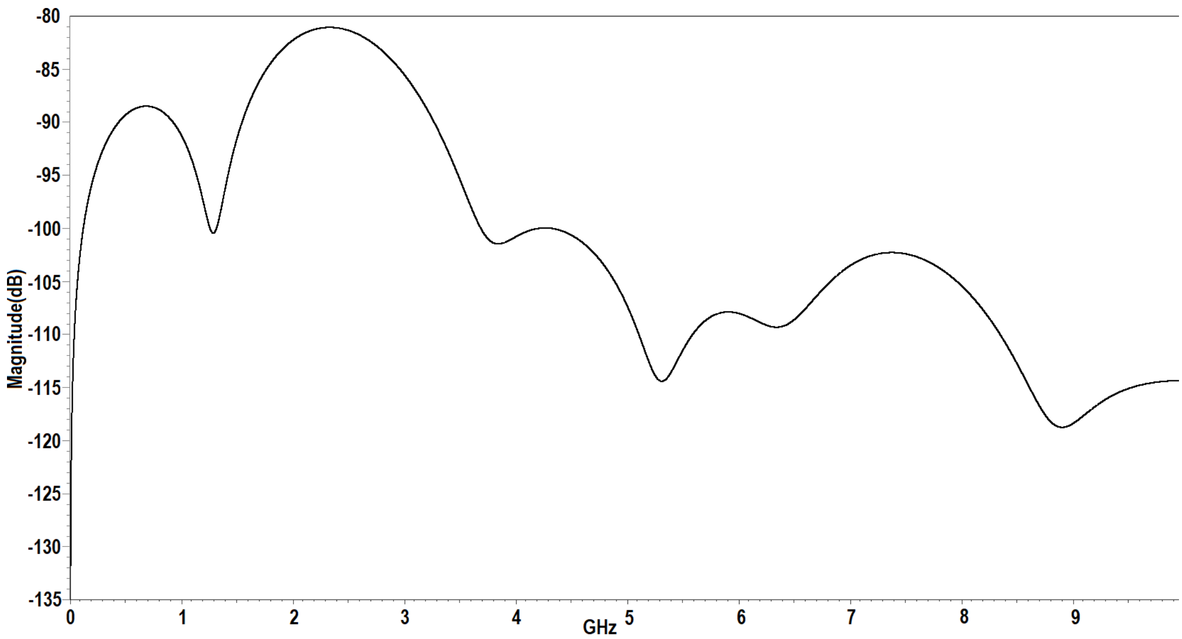

Figure 3.5. PSD of UWB Gaussian triplet-cycle.

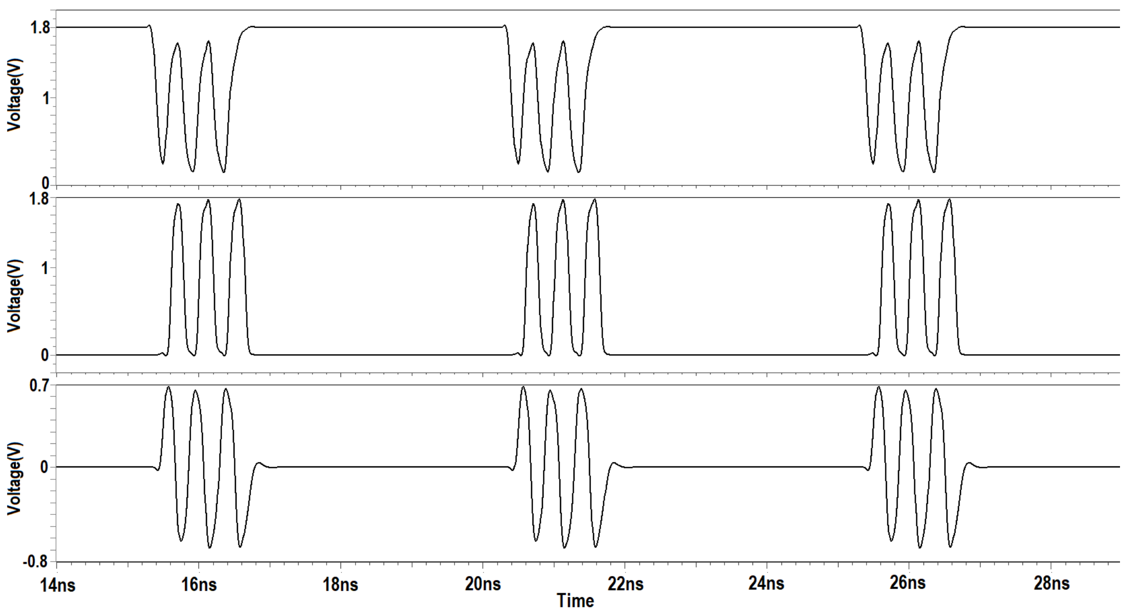

Figure 3.6. Transient Simulation Result of UWB Gaussian quintuplet-cycle.

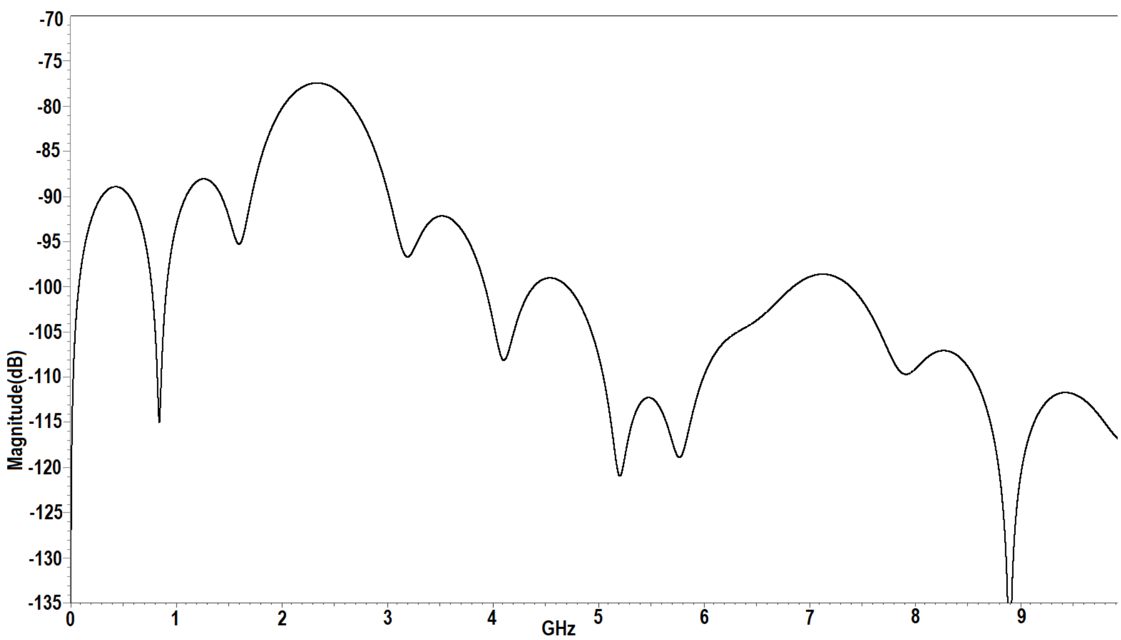

Figure 3.7. PSD of UWB Gaussian quintuplet-cycle.

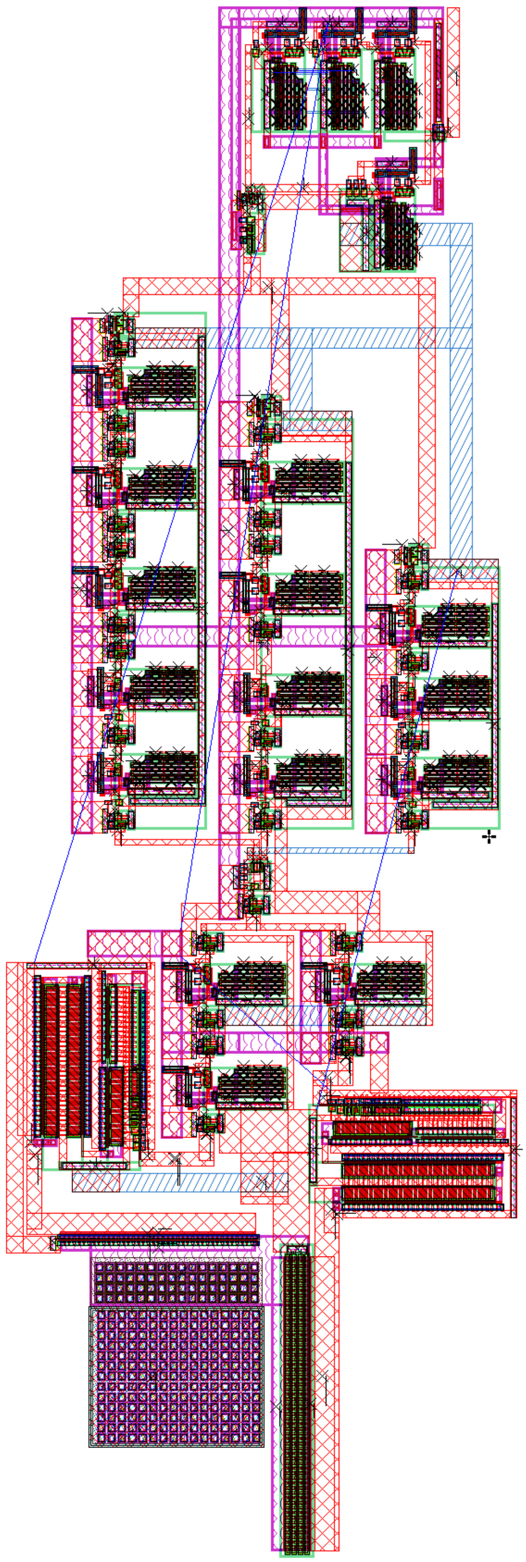

Figure 3.8. Layout of tunable IR-UWB transmitter design.

Table 3.1. Performance Comparison.

Ref.	**Tech. (nm)**	**TX BW (GHz)**	**TX BW with BPF (GHz)**	**Data Rate (Mbps)**	**Vpp. (V)**	**Vpp. with BPF (V)**	**Efficiency (%)**	**Efficiency with BPF (%)**	**EPP (pJ)**	**EPP with BPF (pJ)**
Mono-cycle	180	0.9 - 3.7	2 - 3	0-500	1.4	0.32	6.2	2.85	29	36
Triplet-cycle	180	1.75 - 3.1	2.05 - 2.95	0-1000	1.42	0.6	7.4	5.37	47	54
Quintuplet-cycle	180	1.9 - 2.9	2.1 - 2.75	0-900	1.45	0.77	8.2	6.5	65	72
[9]	130	3.1 - 6	-	200	0.26	-	-	-	20	-
[11]	130	-	3.1 - 5	10	-	0.53	-	4.8	-	26
[15]	180	3 - 5	-	1	7.2	-	10.5	-	224	-
[22]	180	-	0.25 - 0.65	5	0.75	-	-	-	35	-
[23]	180	3.5 - 6.5	-	250	1	-	26.2	-	86	-

3.1.1. Discussion

The performance comparison of the proposed transmitter architectures for Gaussian mono-cycle, triplet-cycle, and quintuplet-cycle are shown with the literature in Table 3.1. The use of BPF is necessary for the Gaussian mono-cycle transmitter due to not complying with FCC limits. However, it can be avoided in the triplet and quintuplet pulses as explained in previous chapter. In order to observe the difference between the transmitters, the BPF results are also added to the performance comparison in Table 3.1. Although 3-5 GHz and 0-960 MHz bands are very popular for UWB applications, 2-3.1 GHz band is selected due to low power consumption and high data rate.

The BW of the Gaussian mono-cycle design is nearly 4 GHz, it drops down to 1 GHz after using BPF. Nearly 1 GHz BW is also achieved without use of the BPF in the Gaussian quintuplet-cycle design. Moreover, the BW of the Gaussian triplet-cycle is around 1.3 GHz. The performances are given at 200 Mbps. The output voltage swing is nearly 1.4 voltage in all the designs. By using the BPF, the voltage swing decreases mostly on the Gaussian mono-cycle. It has the lowest EPP, because it does not need a pulse combination stage, and only two pulses are used on the pulse shaping stage. However, the efficiency figure is the lowest compared amongst the proposed designs. Efficiency is calculated with the definition in [15].

As shown in Table 3.1, performances of Gaussian triplet-cycle and quintuplet-cycle are similar. Although the EPP value is high in Gaussian quintuplet-cycle design, it is the best option in order to comply with the FCC limits. Therefore, Gaussian quintuplet-cycle design is the best option for UWB transmitter due to avoid BPF and provide ultra low power consumption transmitter, the high output voltage swing. The comparison with the literature also shows that the proposed triplet architecture's EPP value is one of the best compared to transmitters in the literature. The average standby power consumption of the proposed transmitters are 2.5 mW because the constant current flow of delay lines.

3.2. Pulse Generation of UWB Transmitter

There are various digital pulse generator designs are suitable in this design. The pulse generator block is the most effective block in the all system because it is the first block of the design. If this block is not optimally designed, then desired pulses cannot be obtained, and it will affect all other signals that occur in the lines that follow the whole design and the desired UWB signal cannot be obtained. Therefore, one should carefully design the pulse generator.

3.2.1. Design of Pulse Generator

In this design, a mono pulse is generated by using the rise edge of the square wave digital data at the input using AND gate. In order to obtain the required pulse, the input square wave signals of an AND gate must be in a different transient position by using digitally controlled delay lines. Time delay difference produces a mono pulse. As seen in Fig. 3.9, the time delay difference between DUMMY signal and DELAYED signal is used to produce a pulse with a tunable PW. High frequencies can be achieved by with this short time pulse. Moreover, all delay lines that meet the needs in the transmitter system are designed as digitally tunable UWB transmitter. In this way, both corner process variations can be compensated, and the desired PW can be adjusted.

The simulation results of the pulse generator are described below, it can be seen in Fig. 3.11 and 3.12 that; a suitable pulse width range has been generated. With digital control input bits, a large number of pulse widths can be obtained. The desired digital code is determined. The pulse width of the desired frequency is obtained The pulse width is 213 ps which can be in the suitable range, as shown in Fig. 3.13. 213 ps desired in Fig. 3.12 and this value indicates that the pulse generator is in a linear range. The PW can be tuned by going to a lower bit number or a higher bit number when corner process variation occurs in the future. In order to make center frequency 2.4 GHz, the PW is selected around 213 ps. In this UWB transmitter method, the center frequency and the BW are two interconnected values. The Digitally controlled delay

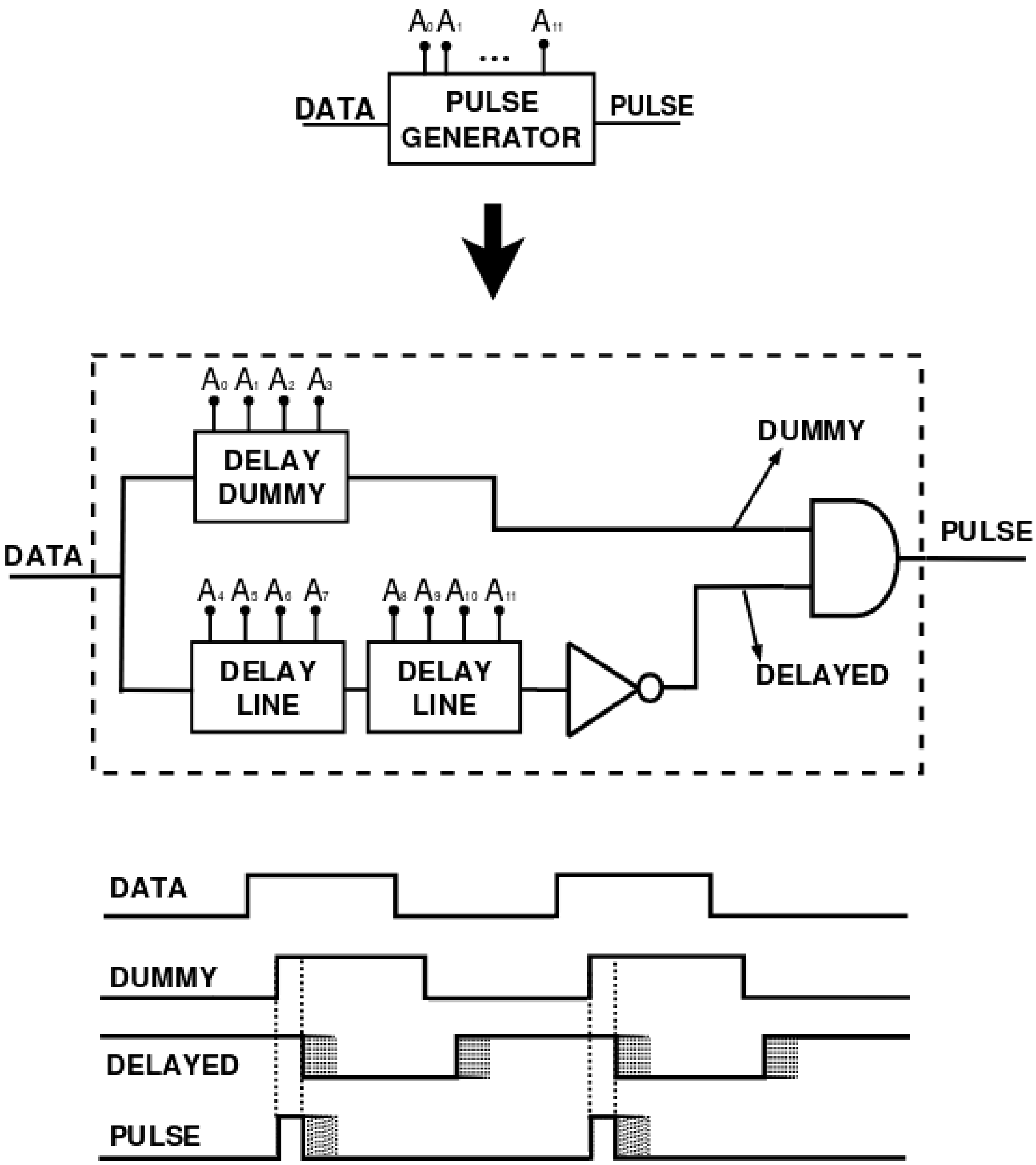

Figure 3.9. Square wave pulse generator design.

lines in Fig. 3.9 were used to tune the pulse to obtain the exact transient positions. Digitally controlled delay lines as seen in Fig. 3.9 can be examined in Fig. 3.14 in details.

The layout design can be seen in Fig. 3.10. On the other hand, the simulation results of the desired signals of the pulse generator is shown in Fig. 3.11 and in Fig. 3.13.

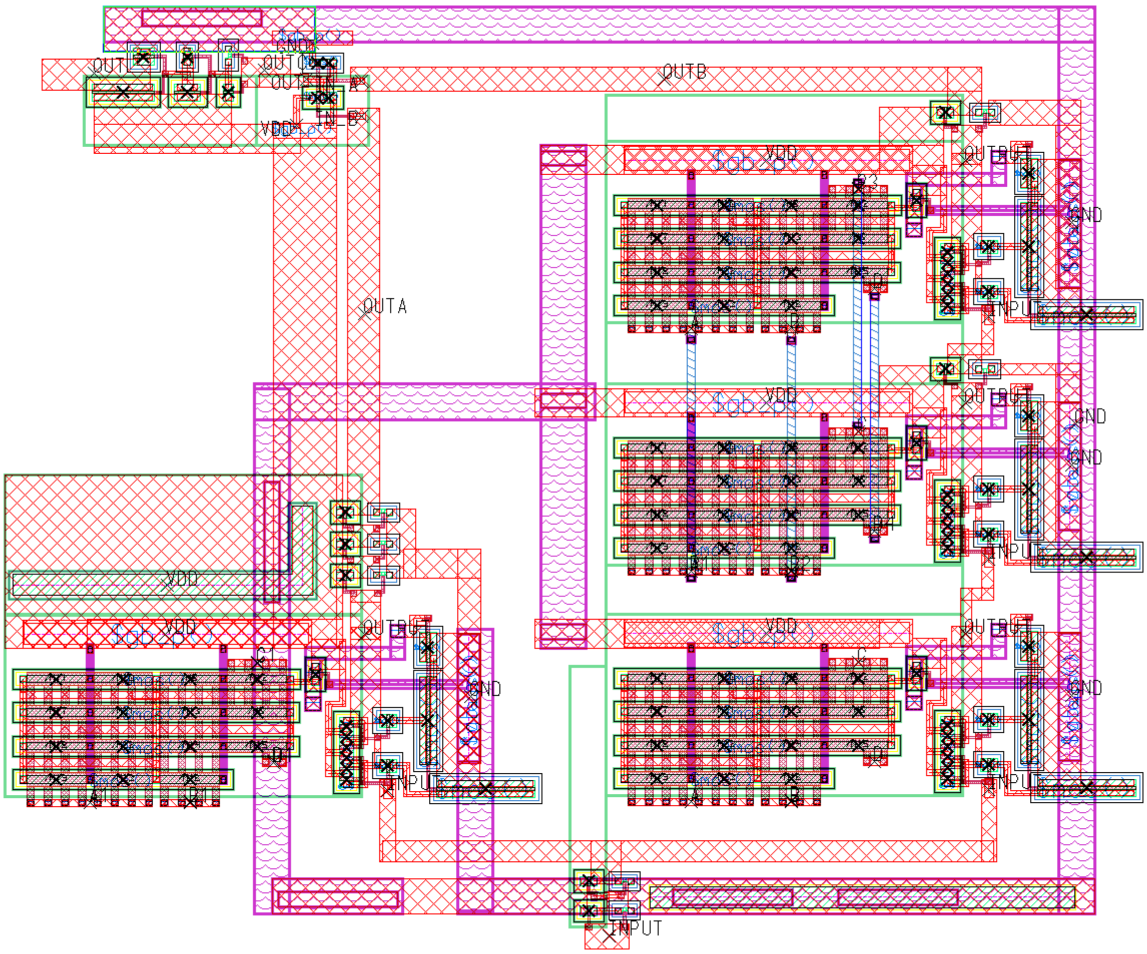

Figure 3.10. Layout of pulse generator design.

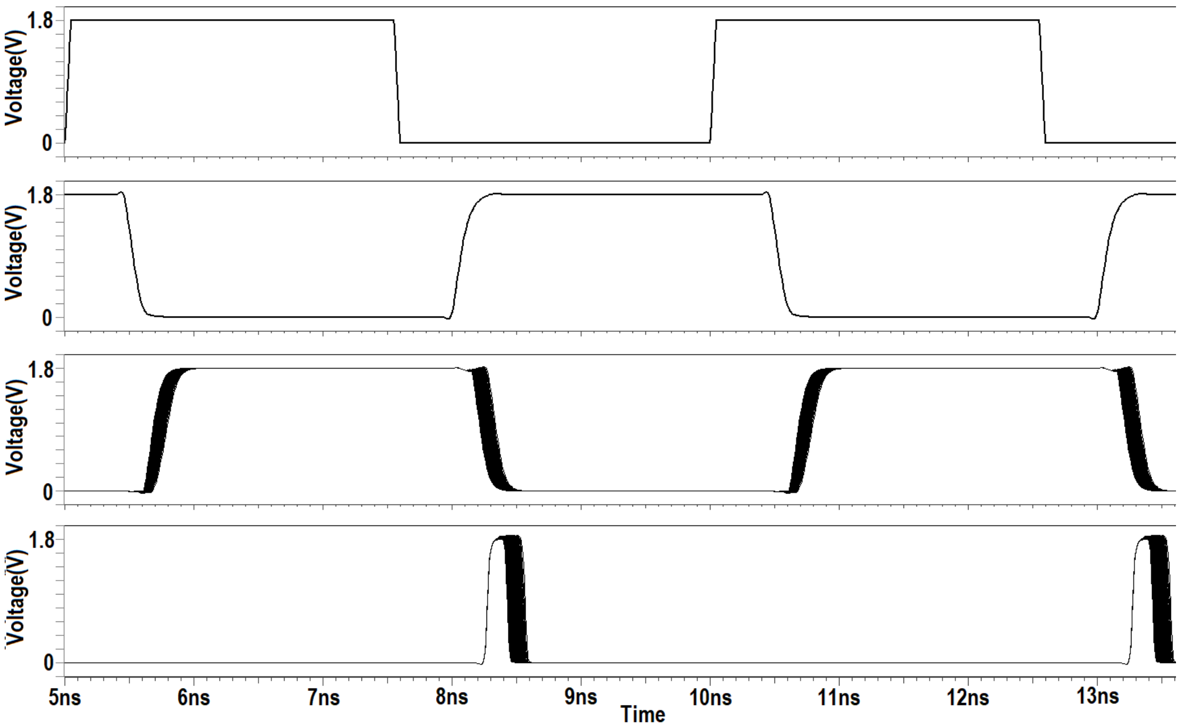

Figure 3.11. Pulse generator all pulses of simulation results.

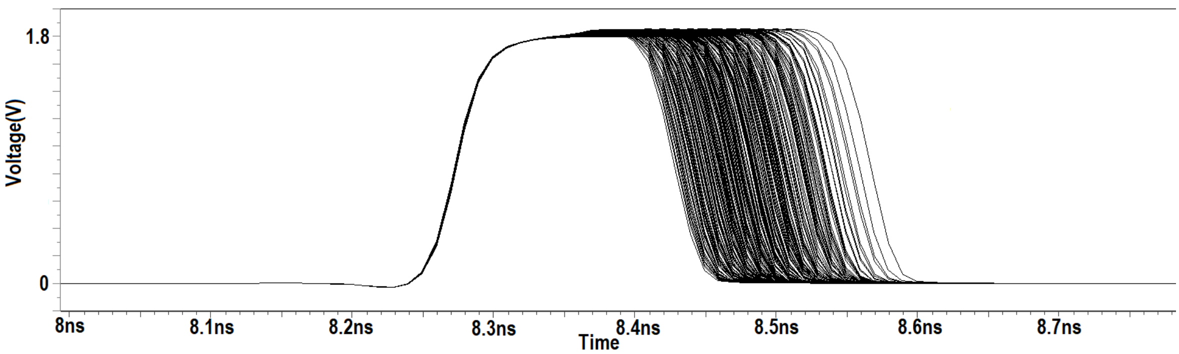

Figure 3.12. Output pulse simulation result of pulse generator block.

3.3. Digital Controlled Delay Line

There are various architectures to obtain digitally controlled delay lines in the literature. It is very important to bring the transient position of the pulses. This method is suitable in order to obtain the exact proposed UWB Gaussian cycles at the output only if the position of the control pulses of P-MOSFET and N-MOSFET in Fig. 3.1 are exactly as desired. To make this possible, digitally controlled delay lines

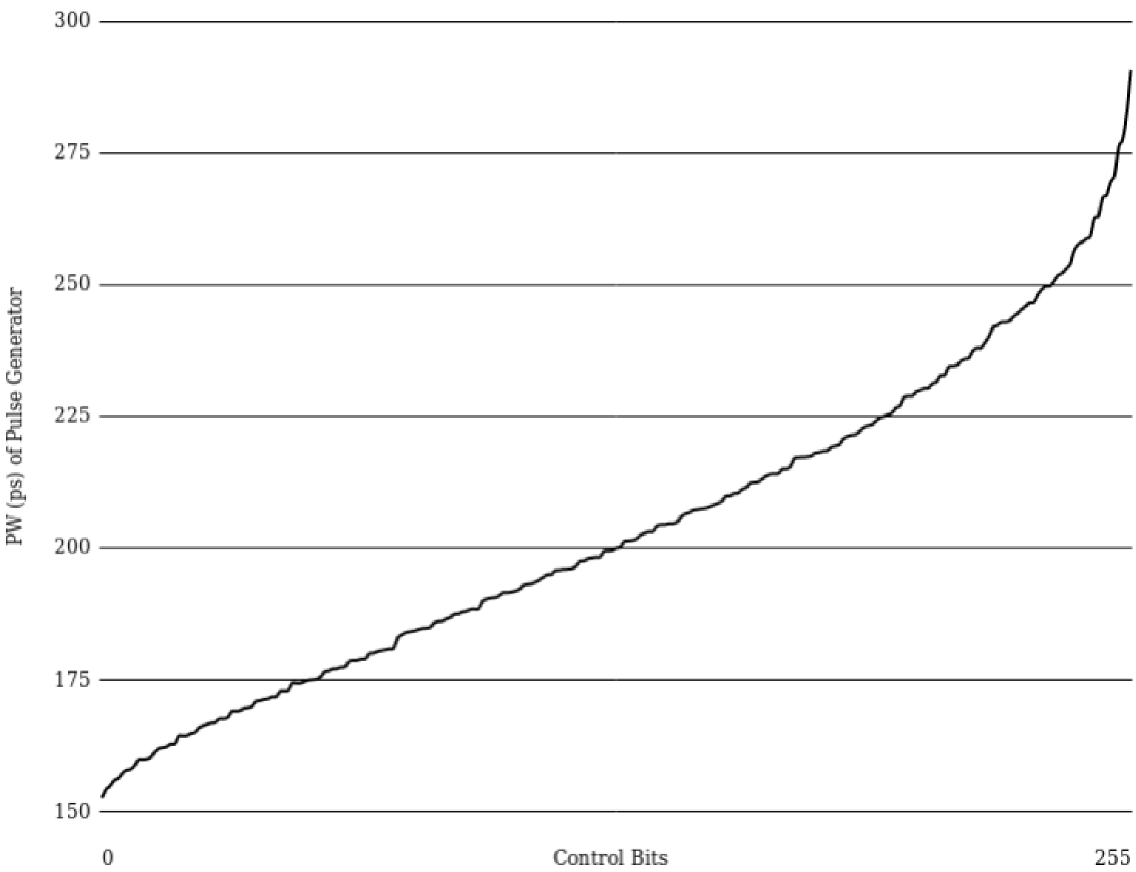

Figure 3.13. PW range of pulse generator simulation.

are used so that delayed pulses must have equal falling edge time delay and rising edge time delay. As a result, the PW is not lost and desired digitally controlled delay line prevents from both the expansion and contraction of the PW.

The digital pulses are delayed by two different methods. The first one is digitally controlled capacitive delay line, that is, delay time can be controlled by changing the capacitance value at the output of the inverter. The second one is current steering digitally controlled delay line. It is possible to delay the pulses by controlling the drain current flow in the inverters. It is important to note that the sizing and current mirror have a structure that will maintain the equality of falling edge time delay risk due to the mobility differences of NMOS and PMOS transistors. The structure is shown in Fig. 3.14. The current steering delay line is used due to a chip's area and power advantage in this thesis.

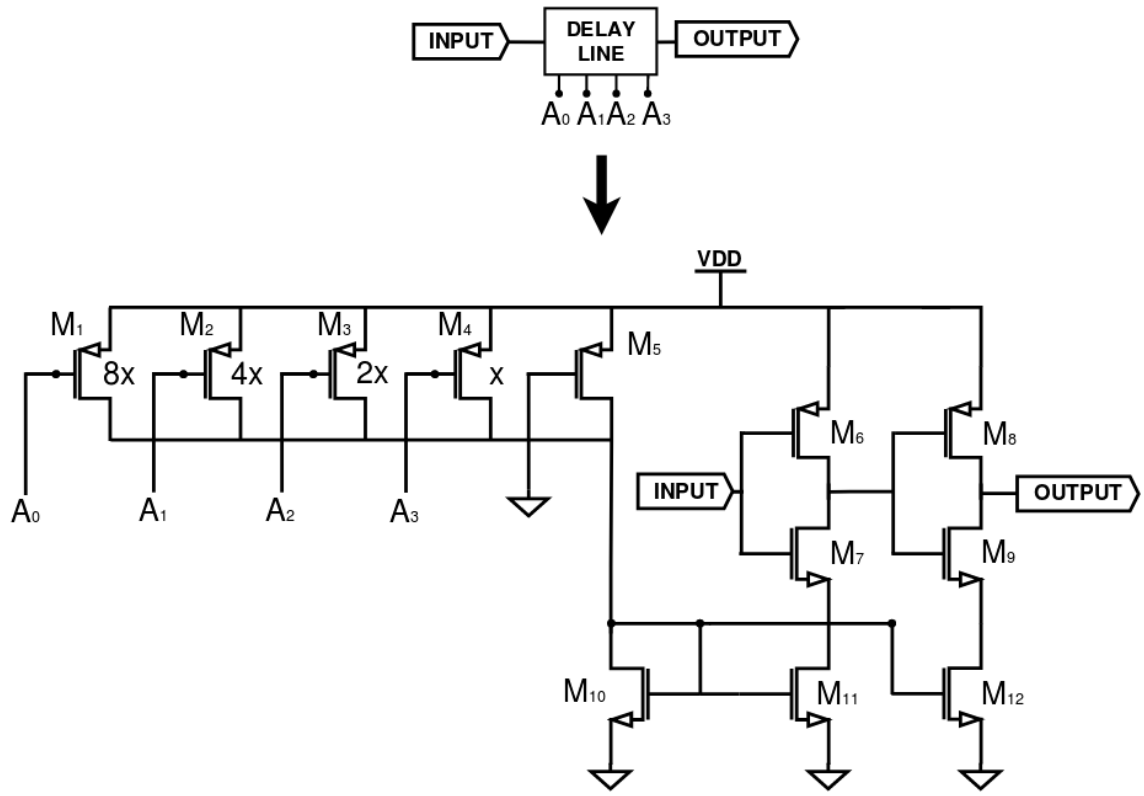

Figure 3.14. Current Controlled Digital Delay Line Design [6].

In the designed digitally controlled delay line, the current flow on the current mirror is changed by each digital bit. Thus, sixteen different transient pulse positions are obtained. To obtain 16 different values, the width over length ratios of M1, M2, M3 and M4 transistors are proportioned as 8x, 4x, 2x and x, respectively, as shown in Fig. 3.14. With the change of the current on the transistor M10 with each bit change, time delay can be controlled by the current mirrors integrated with the transistors M11 and M12 to the inverters' NMOSFETs. Both rise edge time delay and the fall edge time delay of the delayed pulse can be controlled with one current mirror. Due to this method, tunable pulse position is provided. M11 and M12 transistors are very meticulously dimensioned because rising edge delay time depends on the inverter's PMOS transistor, falling edge time delay also depends on the inverter's NMOS transistor. Since mobilities of these two types of MOSFET are different, the current passing through the desired PW cannot be protected if both inverters with the same value are

Table 3.2. Size of Transistors of Delay Cell.

Transistor	**Width (μm)**	**Length (μm)**
M1	4	4
M2	2	4
M3	1	4
M4	0.5	4
M5	0.5	0.5
M6	2.7	0.18
M7	0.9	0.18
M8	2.7	0.18
M9	0.9	0.18
M10	8	0.18
M11	6.7	0.18
M12	6	0.18

biased with current mirror. If falling edge time delay and rising edge time delay are not synchronized, the PW can expand or shrink, and this will not be a useful delay line. One of the most important blocks for the whole system to generate the desired UWB signal is the delay line. The layout design of digitally controlled delay cell is shown in Fig. 3.15

As a result of the simulation, the linearity is not very good at each control bit change. The aim is that the falling edge time delay and rising edge time delay are equal at each bit change. The time delay and pulse width are changed only by changing the temporal position at the input and output of all delay lines. In Fig. 3.17, delay line simulation results can be depicted as a graph in order to show non-linearity.

The dimensions of all transistors in the delay line cell are shown in Table 3.2. In Table 3.3, we can see simulation results of digitally controlled delay cell and time delay for each digital code. In Table 3.4, power consumption simulation results of digitally controlled delay cell are shown for each digital code.

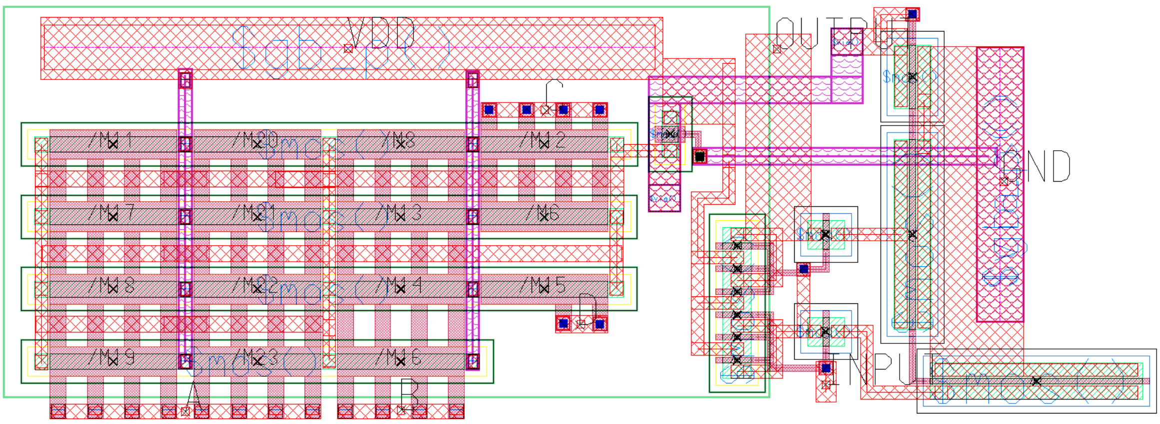

Figure 3.15. Layout design of Current Controlled Digital Delay Line.

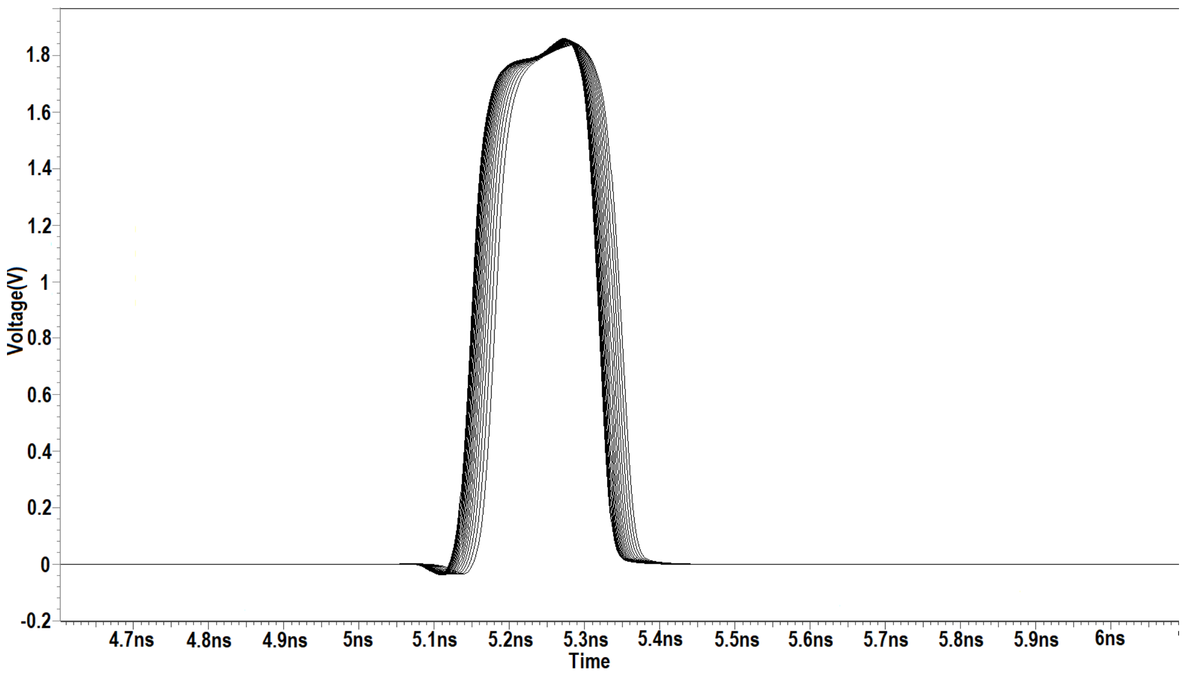

Figure 3.16. Current based digitally controlled delay line simulation results.

Table 3.3. Simulation Results of Delay Cell.

$A_0A_1A_2A_3$	$\tau_{drise}(ps)$	$\tau_{dfall}(ps)$
0000 - 0001	0.939	0.778
0000 - 0010	1.763	1.657
0000 - 0011	2.781	2.653
0000 - 0100	3.911	3.777
0000 - 0101	5.161	5.047
0000 - 0110	6.549	6.488
0000 - 0111	8.091	8.121
0000 - 1000	9.817	9.962
0000 - 1001	11.754	12.034
0000 - 1010	13.944	14.351
0000 - 1011	16.441	16.901
0000 - 1100	19.325	19.662
0000 - 1101	22.706	22.601
0000 - 1110	26.739	25.740
0000 - 1111	31.662	29.006

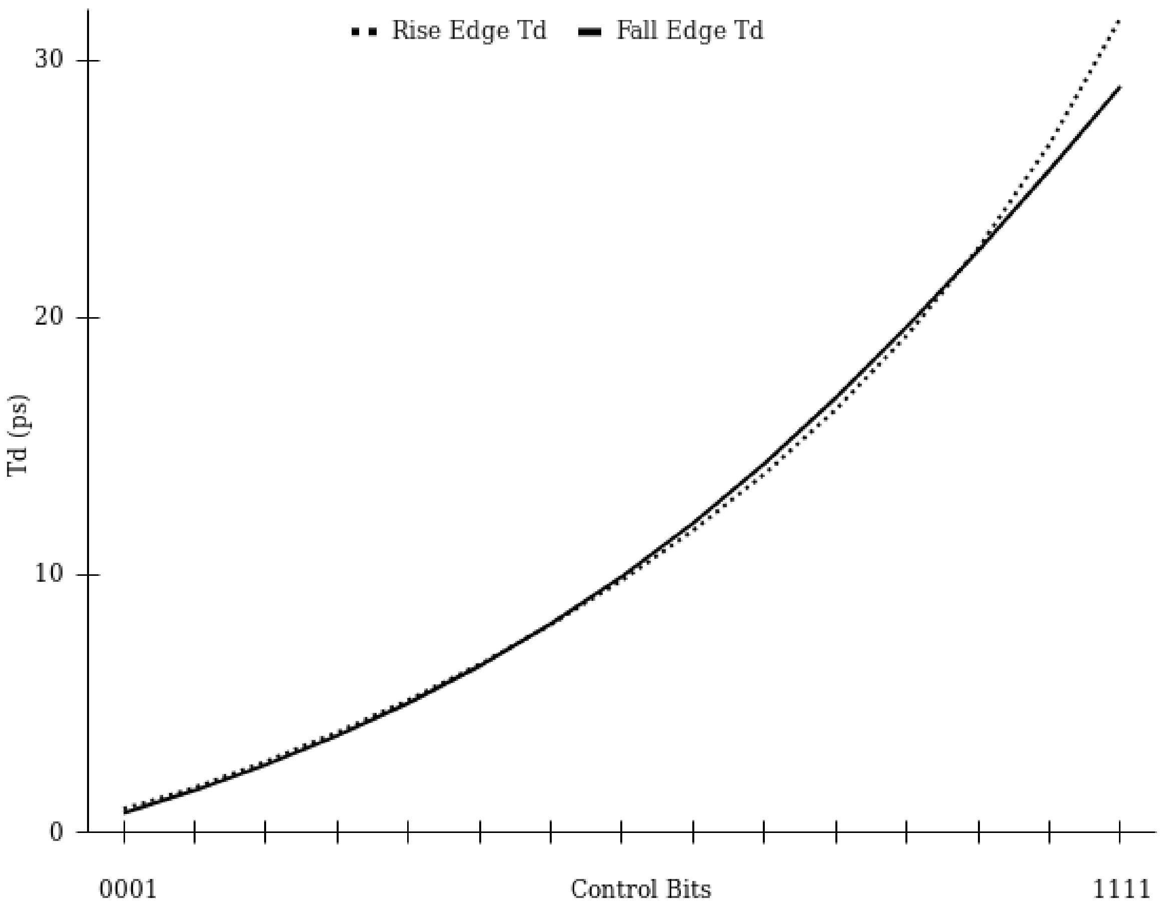

Figure 3.17. Current Controlled Digital Delay Line Simulation Results.

Table 3.4. DC power simulation results of delay cell with changing between 0000 to 1111.

$A_0A_1A_2A_3$	**Power Consumption** μW
0000	231.33
0001	222.43
0010	213.49
0011	204.52
0100	195.51
0101	186.47
0110	177.39
0111	168.27
1000	159.13
1001	149.94
1010	140.71
1011	131.41
1100	122.04
1101	112.59
1110	103.08
1111	93.509

4. TUNING ALGORITHM

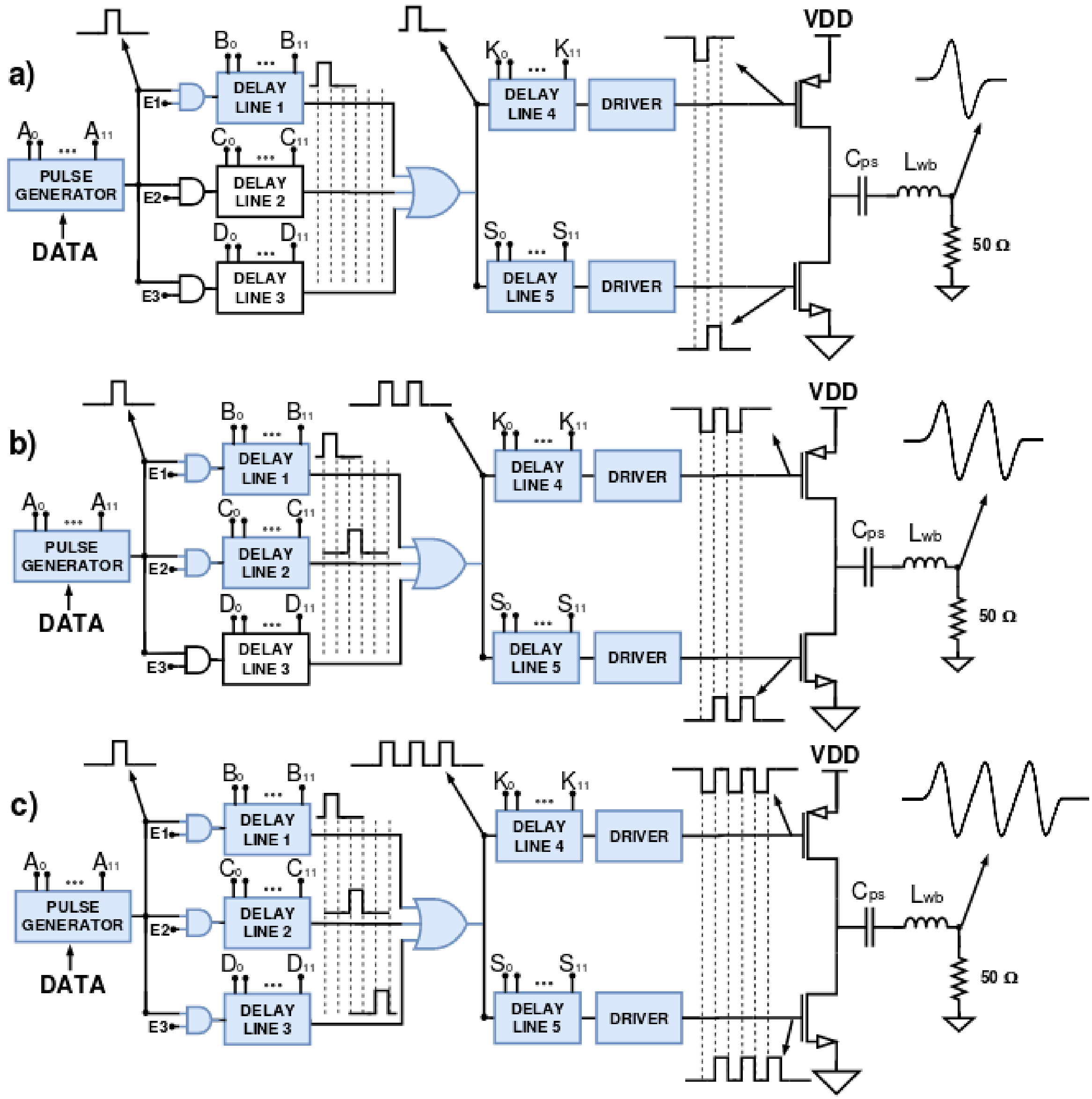

Figure 4.1. Tuning Algorithm Steps UWB Pulse Generator for Gaussian a) mono-cycle b) triplet-cycle c) quintuplet-cycle.

Due to the large number of digital control pins of the tunable UWB transmitter, register file should be created. The digital data consisting of a very high number of bit from a single serial port should be given to the input of the register files in order to activate all control inputs of digitally controlled delay lines in UWB transmitter.

In the design in Fig. 4.1 (a), since the number of digital control inputs is high and it is almost impossible to observe the desired quintuplet-cycle signal by trying all the control pins. The register file's input code required for the desired signal can be achieved by creating a tuning algorithm, then observing the signal at the output.

First of all, we can access a digital code by trying the control pins of the control generator. Delay Line 1, 4 and 5 which are aimed to generate a Gaussian mono-cycle signal. Thus, the pulse generator, Delay Line 1, 4 and 5's control code can be fixed. Delay Line 2 can be activated to find desired code. The number of attempts required to decode Delay Line 2 will be as few as Delay Line 1. In this way, the Gaussian mono-cycle will always be in the fixed and desired transient position.

While finding the control code of Delay Line 2 to generate triplet-cycle, the control code of the pulse generator's, Delay Line 1, 4 and 5's will never be changed. No distortion will occur on the part of the UWB signal on the output affected by these fixed codes. After the Gaussian triplet-cycle signal is created in this way, by using the same tuning algorithm method, the digital control code of Delay Line 1,2,4 and 5 is kept constant and an attempt is made to find the code of Delay Line 3 and solution is provided to generate quintuplet-cycle.

Microchip testing can be achieved more easily by fixing this code. The purpose of all this tuning algorithm method is to minimize the number of pins used for the transmitter of the microchip to be tested. In this way, the extra signals and effects coming from the pad of the microchip are also reduced.

5. CONCLUSION AND FUTURE WORK

This thesis presents an UWB transmitter design for medical imaging system. A configurable all digital UWB transmitter has been designed for high data rate and ultra low power applications. 200 Mbps data rate is achieved in proposed design. The power consumption at 200 Mbps for Gaussian mono-cycle, triplet-cycle and quintuplet-cycle are 5.9 mW, 9.4 mW and 13 mW respectively. These values translate to 6.2%, 7.4% and 8.4% efficiencies which is a very good value for an ultra-low power applications. Another challenge is process variation. In order to make design robust, the proposed UWB transmitter is designed as all digitally tunable architecture. The proposed design removes the requirement of a BPF. It could be possible by using pulse combination with pulse shaping method. Moreover, the simulation results of post-layout design are shown in the thesis to prove design working in desired specifications. As a future work, the proposed UWB transmitter design will be fabricated and tested for data transfer. The tuning algorithm will be applied to find digital control bits while testing. The register file can be integrated in the chip to reduce number of pads in chip. The UWB antenna will be selected as a commercial product.

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