A PRACTICAL APPROACH TO MIL-STD-1553 BUS TRANSCEIVER ANALOG FRONT END WITH DISCRETE COMPONENTS AND IC DESIGN UNDER UMC130NM PROCESS

by

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ABSTRACT

A PRACTICAL APPROACH TO MIL-STD-1553 BUS TRANSCEIVER ANALOG FRONT END WITH DISCRETE COMPONENTS AND IC DESIGN UNDER UMC130NM PROCESS

This thesis deals with the research and built of a commercially operational MIL-STD-1553 Bus Transceiver Analog front end in both PCB with discrete elements and CMOS IC design in Cadence under umc130nm technology which are used in various Avionics and aerospace applications. Although the functional block diagram of a bus transceiver is depicted and used in the literature widely, nevertheless, there is little close to none information on how one should implement such circuit. Companies such as Sital, Cobham, Holt integrated and DDC to name a few, build and commercially use 1553 BUS families without disclosing the schematic information of the circuit. This leaves us to build the receiver and the transmitter almost from scratch by benefiting from other line/transformer driving circuitry ideas used in LVDS [1], modem lines and other differential signaling methods [2]. The inductive and resonance behavior of the isolation transformer winding is widely discussed to be able to generate the optimum method for driving the terminals of the transceiver to meet the specific requirements dictated by 1553 standards back in 1973 by U.S.Air Force [3]. Also analytical solutions are presented for the method developed to help understand how the electrical requirements stated by 1553 can be tuned in the circuit. Altium PCB and Cadence layout design are shown with in-depth system testing and post layout simulations. The PCB board is manufactured and is successfully operational. The points of improvement on the board, backed up with reasoning, are discussed.

ÖZET

UMC130nm Süreci Altında Ayrık Bileşenler ve IC Tasarımı ile MIL-STD-1553 Veriyolu Alıcı-Vericisi Analog Ön Ucuna Pratik Bir Yaklaşım

Bu tez, çeşitli Aviyonik ve havacılık uygulamalarında kullanılan umc130nm teknolojisi altında Cadence'de hem ayrı elemanlara sahip PCB'de ticari olarak operasyonel bir MIL-STD-1553 Bus Transceiver Analog ön ucunun araştırılması ve inşa edilmesi ile ilgilidir. Bir veriyolu alıcı-vericisinin işlevsel blok diyagramı literatürde geniş çapta tasvir edilmiş ve kullanılmış olsa da, böyle bir devrenin nasıl uygulanması gerektiğine dair hiçbir bilgi hemen hemen hiç yoktur. Sital, Cobham, Holt entegre ve DDC gibi şirketler, devre hakkında şematik bilgi olmadan 1553 BUS ailesini inşa eder ve ticari olarak kullanır. Bu, LVDS'de [1], modem hatlarında ve diğer farklı sinyalleme yöntemlerinde kullanılan diğer hat / transformatör sürüş devresi [2] fikirlerinden yararlanarak alıcıyı ve vericiyi neredeyse sıfırdan inşa etmemize neden olur. İzolasyon transformatörü sargısının endüktif ve rezonans davranışı [3], 1973'te ABD Hava Kuvvetleri tarafından 1553 standartlarının belirlediği özel gereksinimleri karşılamak için alıcı-vericinin terminallerini sürmek için optimum yöntemi üretebilmek için geniş çapta tartışılmaktadır. Ayrıca, 1553'te belirtilen elektrik gereksinimlerinin devrede nasıl ayarlanabileceğini anlamaya yardımcı olmak için geliştirilen yöntem için analitik çözümler sunulmuştur. Altium PCB ve Cadence düzeni tasarımı, derinlemesine sistem testleri ve yerleşim sonrası simülasyonlarla gösterilmiştir. PCB kartı üretildi ve başarıyla çalışıyor. Kart üzerindeki iyileştirme noktaları konuşulup, tartışılmıştır.

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LIST OF SYMBOLS

A	Amperes
H	Henry
L_i	Inductance
R_i	Resistance
V	Volts
Z_i	Impedance
Ω	Ohms
μ	Micro
ω	Angular Frequency

LIST OF ACRONYMS/ABBREVIATIONS

MOSFET	Metal Oxide Silicon Field Effect Transistor
MIL	Military
NMOS	N-channel MOSFET
STD	Standard

1. INTRODUCTION

Mil-STD-1553 defines a set of standards which govern the specifications of the military and/or civil aircraft electronic and communication systems. Among them, it includes the data bus and terminal standards for data communication between different IP cores located in various locations of the aircraft. These IP cores communicate with each other electrically via a data bus, and the function of sending and receiving signals is solely upon the analog Transceiver (transmitter and receiver) front end. 1553 standards determine sets of specifications that have to be met at each terminal of the IP core. These standards therefore set important design specifications that have to be met by the transceiver front end. However, since the transceiver is connected to the terminal via an isolation transformer (and terminal to the bus by either transformer coupled or direct coupled stubs) ambiguities arise on what electrical specification should the transceiver and/or isolation transformer have in order to meet 1553 terminal specifications together. In this thesis, we will be designing, modeling and investigating possible transceiver typologies which differ mostly in transmitter part as well as an isolation transformer in order to get some idea on how to implement it with discrete components as well as using CMOS UMC130nm technology. In that regard, we will observe what modeling of isolation transformer is more suitable for our transceiver (in terms of turns ratio and coupling factor) and how 1553 specifications on the terminal affects the specifications of the transceiver alone. We will be focusing on the simulation and design parameters which arise from the terminal requirements using SPICE which eventually will be implemented on a PCB. Receiver and Transmitter will be discussed separately and finally their combined (parallel) connection as a whole transceiver block. Analog front end of 1553 design plays a very important role in operation of the terminal. An inadequate design in analog front end would lead to a marginal and inoperative terminal no matter how adequately the terminal is designed [4]. There are two major elements in the analog front end of a terminal. The receiver converts the waveform received from the terminal to a digital form for the IP core to process. The transmitter in the other hand takes TTL digital input signals and generates a proper signal to the

terminal which is connected to the BUS. All terminals make use of isolation transformer which is then makes a connection to the BUS via direct (with fault isolation resistors) or transformer coupled connection. Using the right method and modeling for meeting the terminal electrical requirements is essential and the challenges arising from those limitations is the main topic of this thesis. The discussed project has a highly industrial side to it, nevertheless, there is a demand for a practical approach on circuit design and calculations of a bus transceiver both on a PCB (with discrete elements) and using CMOS technology.

Chapter 2 goes through the literature and design. Receiver and transmitter are investigated separately and a design for each is discussed. They include subsections for the PCB and IC parts of the project separately. Challenges in the design and their appropriate solutions will be discussed. A mathematical model for the transmitter circuit will be looked over with a theoretical solution. In Chapter 3 the complete transceiver will be simulated for receiving and transmitting, for both PCB and IC in SPICE and Cadence ADE respectively. Also in Chapter 3 we will be testing the PCB board and post layout simulations will be shown for the IC part of the project. In Chapter 4, the shortcomings of the outcomes in Chapter 3 will be pointed out and future works for improvements will be presented. The design challenge and optimization techniques for least overshoot, as well as determining factors for proper waveform transmission is discussed in Chapter 2.

2. LITERATURE REVIEW AND DESIGN

The block diagram of the transceiver we are going to design is shown in Figure 2.1. MIL-HDBK-1553A handbook states that the receiver must sense a digital signal bit 1 (RCV_OUT high) if the terminal signal plus is sufficiently greater that terminal signal minus and digital signal bit 0 (RCV_OUT low) vice versa. The threshold at which this sensing occurs is a specification we will discuss later. The transmitter, on the other hand, will receive a digital data bit from the IP core and translate it into electrical signal meeting the 1553 analog specification. Both transmitter and receiver are required to work under 1MHz speed and that is what we will be considering throughout this thesis. The isolation transformer plays a huge role in specifying the terminal electrical properties, therefore it must be modeled and calculated carefully while designing the transceiver. In the upcoming sections the isolation transformer will be discussed more in depth. Before moving on to modeling and calculations, it is useful to have a table of the terminal specifications required by the 1553 standards mainly extracted from 1553A handbook. Table 2.1 shows them briefly; it also states design specifications which will be clear later on in the thesis.

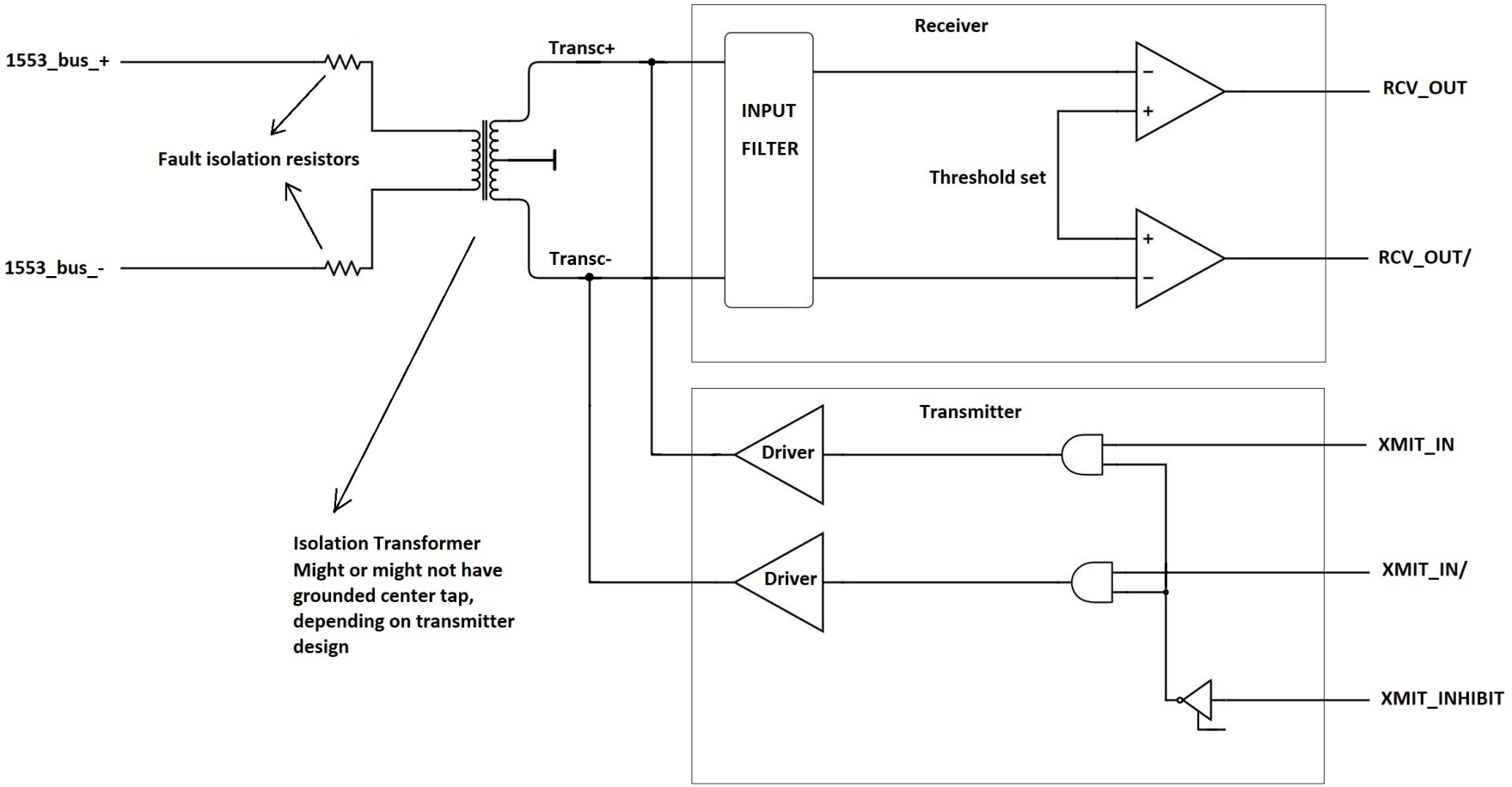


Figure 2.1. Transceiver Block [4]

Table 2.1: Transceiver Requirements [4]

Requirement Code	**Description**
HRS_001	1. TRANSCEIVER GENERAL REQUIREMENTS
HRS_002	Transceiver is required to work with 1MHz of speed. This has to be supported for both transmission and receiving signals.
HRS_003	Power supply required by the transceiver is 5Vdc for PCB part of the project and 5Vdc and 3.3Vdc for the IC part of the project.
HRS_004	Transceiver input impedance: Terminal input impedance is required to be atleast 1Kohms for transformer coupled stubs and 2Kohms for direct coupled stup. This puts a constraint of high input impedance on the analog front end transceiver since this impedance reflects to the terminal appearing as parallel with other impedances in the terminal such as transformer bus side and wiring. Transceiver input impedance itself is calculated by taking into parallel the transmitter output impedance and receiver input impedance. This value has to be as large as possible. 10KOhms is a typical value.
HRS_005	2. RECEIVER REQUIREMENTS.

Table 2.1: Transceiver Requirements [4](Cont)

Requirement Code	**Description**
HRS_006	2.1. RECEIVER GENERAL REQUIREMENTS.
HRS_007	Receiver input filter is a lowpass filter which starts to roll off between 1 and 2 MHz.
HRS_008	The receiver must be designed to produce an output of 1 (RCV_OUT high) when 1553_BUS_+ is sufficiently greater than 1553_BUS_—, and an output of 0 (RCV_OUT/ high) when 1553_BUS_— is sufficiently greater than 1553_BUS_+, and both outputs high (or low) when the terminal is at idle state. Under this constraint, the threshold voltage to which an input is detected has to be set to 0.43 Vp, in another word, input voltages between 0.43Vp and 14Vp must be sensed by the receiver. Voltages below 0.1 Vp should not arouse the receiver for an input.
HRS_009	The receiver must show both outputs either high (1) or low (0) when the terminal is at the idle state. i.e. when there is no signal on the terminals.

Table 2.1: Transceiver Requirements [4](Cont)

Requirement Code	**Description**
HRS_010	Receiving zero crossing distortion occurs when input signal to the receiver falls below the manufactured threshold levels. Typically values are above 300ns in those cases. Normally the zero crossing delay criteria is below 300ns.
HRS_011	3. TRANSMITTER REQUIREMENTS.
HRS_012	3.1. TRANSMITTER GENERAL REQUIREMENTS.
HRS_013	The transmitter is the element in the terminal that drives the bus. It receives digital signal from the encoder which is typically differential TTL, and produces a signal on the bus that abides the requirements of 1553 standards. Two drivers are usually used for each terminal end and are designed to control the rise and fall times and the waveshape of the outputs. Transmitter also contains an inhibit input (XMIT_lNHIBIT) by which it disables the transmission.
HRS_014	We will be using a current mode transmitter with isolation transformer center tap grounded. Current-mode transmitters tend to have lower power consumption, smaller packages, and lower cost.

Table 2.1: Transceiver Requirements [4](Cont)

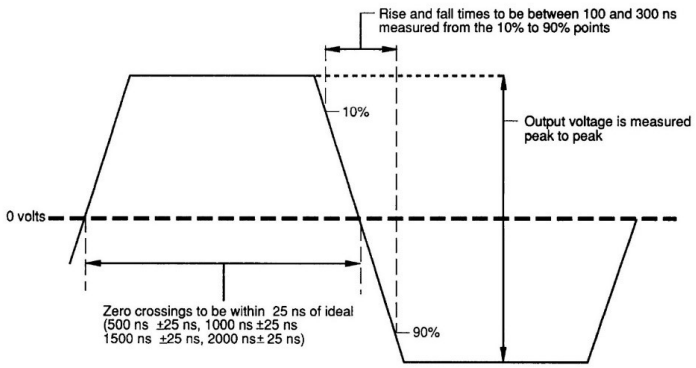
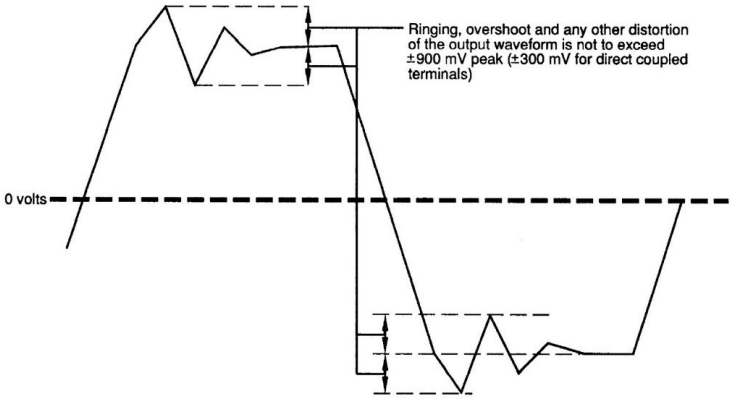
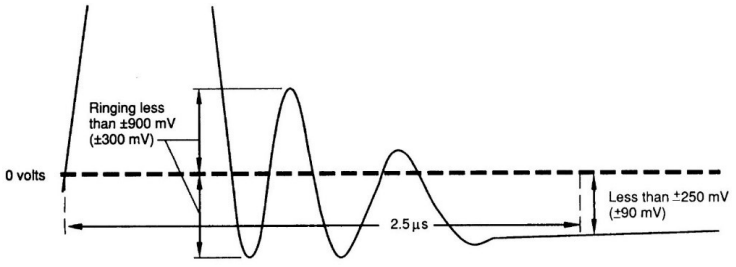
Requirement Code	Description
HRS_015	3.2. TRANSMITTER INPUT REQUIREMENTS.
HRS_016	Input voltage requirement: TTL logic (low:0 V, high:3.3 V).
HRS_017	3.3. TRANSMITTER OUTPUT VOLTAGE REQUIREMENTS.
HRS_018	Output voltage levels of the transmitter are required to be square wave between 22V and 27V peak to peak under 70ohms resistive terminal load. Loaded terminal voltage is measured between (1553_bus_+) and (1553_bus_-).
HRS_019	Output voltage rise and fall times must fall between 100ns to 300ns. Terminal voltage is measured between (1553_bus_+) and (1553_bus_-). 

Table 2.1: Transceiver Requirements [4](Cont)

Requirement Code	Description
HRS_020	Output voltage ringing and overshoot must be confined within 900mV between (1553_bus_+) and (1553_bus_-). 
HRS_021	Output voltage decaying tailoff: at the end of every transmission, at the moment when input to the transmitter is disabled the output voltage overshoot (if oscillations present) must be within 900mV. This oscillation and/or decaying must settle to at most +/- 250mV (0V ideally) within atmost 2.5us. Following image illustrates this requirement. 
HRS_022	Transmitter will be driving a 70Ω resistive load at the terminal ends.

There is a lower limit on the rise and fall times of the transmission signal for the purpose of limiting the harmonic content of the signal above 1MHz [7]. Regarding the receiver, both linear (CTLE) and non-linear (DFE) equalization techniques are appropriate for compensating channel loss and absorbing multiple reflections in a multi-drop bus environment [8], but such techniques are out of the scope of this thesis.

In an attempt to design the required transceiver, we will be investigating receiver and transmitter topologies in the following subsections. But first, we will model the isolation transformer, since both transmitter and receiver models will heavily depend on it. Isolation transformer should be applied in every DC drive [9]. The way in which we will be driving the terminal is similar to that of ADSL line-drivers. However, ADSL signals have a high peak-to-average voltage ratio [10]. In our case peak to average voltage is about 10-11 V. We model our transformer using ideal inductor models. High current inductor applications operating in the MHz range are generally limited to voltage regulator modules [11].

2.1. Center tapped isolation transformer

Since we are using current mode driver for transmitting, we made the choice of using a center tapped isolation transformer. This would have not been the case if we wanted to use voltage mode transmitter topology for transmission. Current mode transmission is chosen based on the reasons given in Table 2.1 HRS_014 requirement. Most simulations will be based on SPICE for both PCB and IC design. Therefore an adequate, but not necessarily an exact model is crucial for simulations and understanding of the circuit operations. 1553 standards for terminal isolation transformer is beyond the scope of this thesis, however, by making use of commercially available transformers and their circuit models we put the rest of the circuit simulation on the right path. SPICE model of a non ideal transformer consists of inductors and their relative couplings. In this part we will be approximating those values base on Q1553-45

commercially available chip. Figure 2.2 illustrates the final model of the transformer.

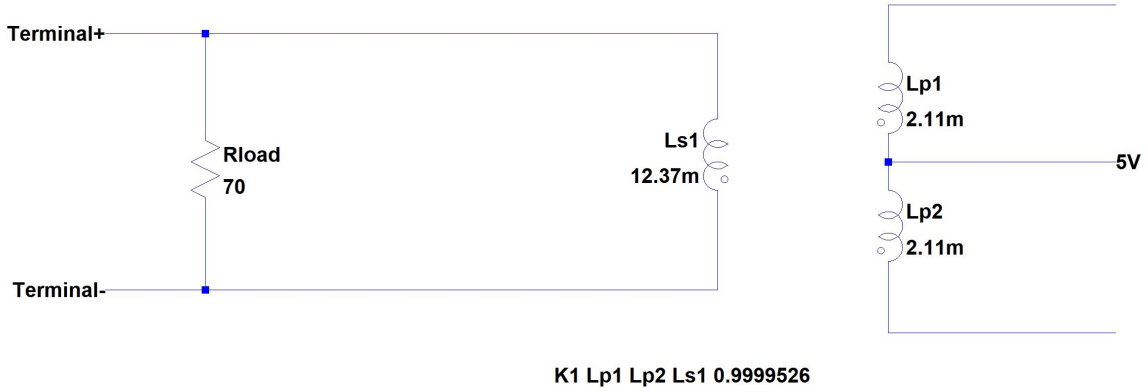


Figure 2.2. Center tapped isolation transformer

Values taken here for the inductors and their mutual couplings are based on [12]. The coupling factor is deduced from the relationship between the leakage and primary inductance values. Figure 2.3 illustrates the leakage inductance. The relation between the leakage inductance and the approximation used in this thesis is calculated in Equation 2.1:

$$\begin{aligned} (1-K)L_p &= L_{leakage} \\ K = 1 - \frac{L_{leakage}}{L_p} &= 1 - \frac{0.1\mu H}{2.11mH} = 0.9999526 \end{aligned} \tag{2.1}$$

The relation between the turns ratio and the inductance values of the transformer primary and secondary sides is given in Equation 2.2.

$$\begin{aligned} n &= \sqrt{\frac{L_{s1}}{L_{p1}}} \\ n &= \sqrt{\frac{12.37}{2.11}} = 2.42 \end{aligned} \tag{2.2}$$

It is also vital to consider the cantilever model of the transformer since it will be re discussed in the Transmitter section of the thesis. The extended cantilever model of an N winding transformer is given in Figure 2.4 [5].

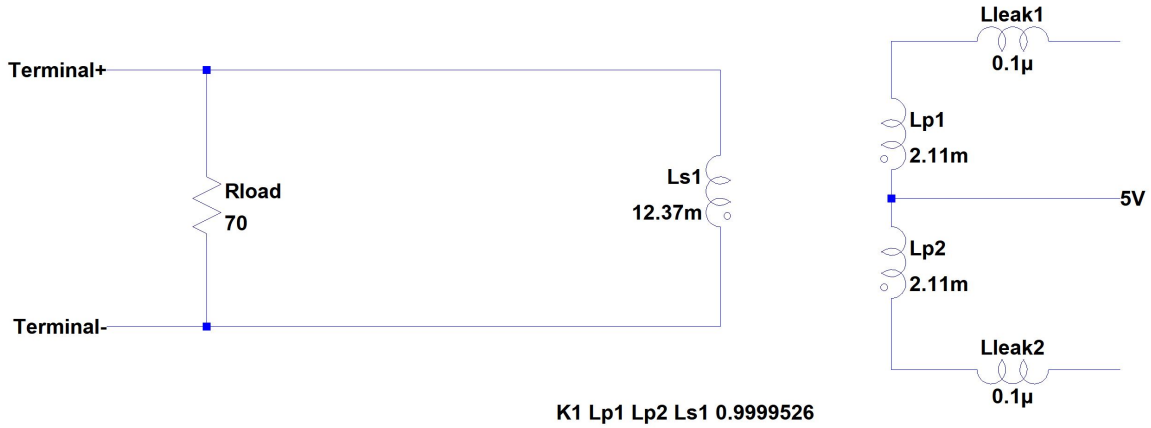


Figure 2.3. Center tapped isolation transformer leakage inductance

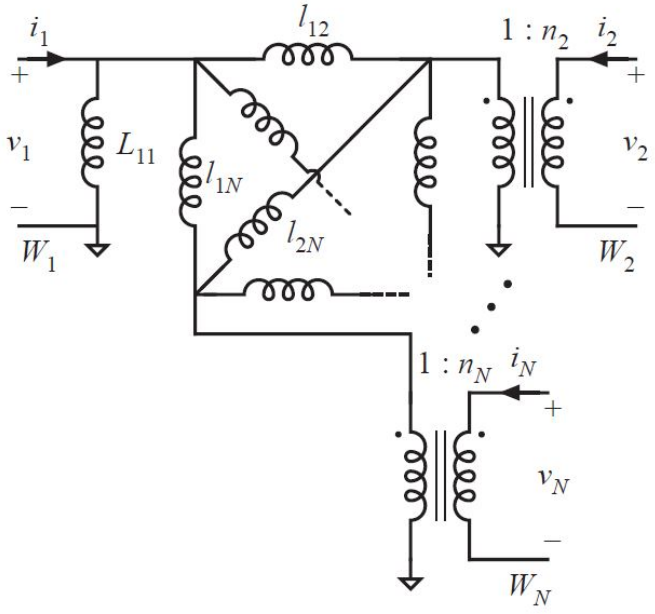


Figure 2.4. N-winding transformer extended cantilever model [5]

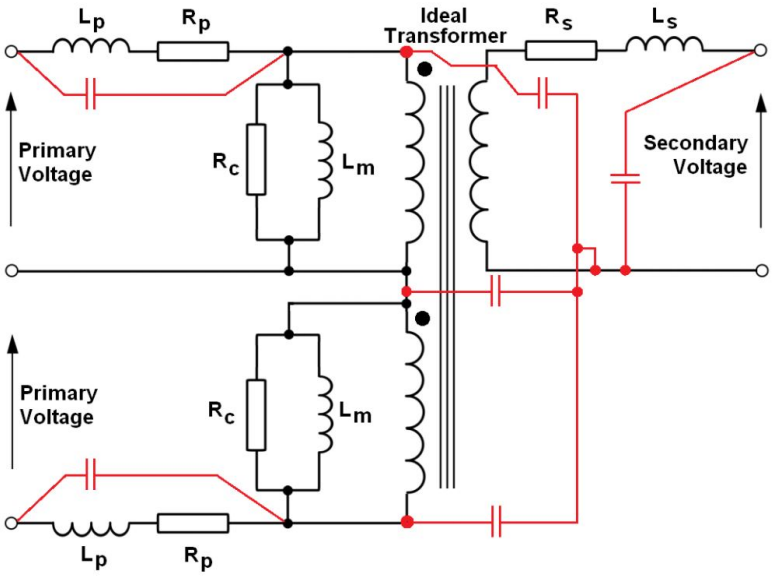


Figure 2.5. Two winding (center tapped) transformer high frequency model

However, a more understandable model for high frequencies is given in Figure 2.5. The model in Figure 2.5 provides a clue to why we may get low frequency oscillations in the transmitter circuit. This phenomenon occurs in conjunction with the reflections at the stub. The amount of reflections that are produced at the stub connection to the bus will be based on the impedance of the stub in parallel with the characteristic impedance of the transceiver [7]. In the meantime, we will let SPICE take care of the modeling (as opposed to us implementing it with discrete components ourselves) and will fall back to the modelings presented in this section later on when we discuss the transmitter circuits.

2.2. Receiver input filter and level shifter

The block diagram in Figure 2.1 shows an input filter at the receiver side just after the isolation transformer. This filter usually consists of a low pass filter (passive or active) which is responsible for filtering out high frequency noise. Therefore, the roll off frequency of this filter is typically designed to be around 1.5MHz. In this filter, as far as our design is concerned, a DC block (aka high pass) is also necessary. Therefore

we would have a band pass filter centered around 1MHz (required frequency) at the input. However, after a few problems observed on the manufactured PCB arising from the low pass filter (mostly capacitive) we decided to omit the low pass filter in our circuit. After all, most of the noise is filtered through the isolation transformer as well as the hysteresis effect in the receiver comparators which will be discussed more in detail in upcoming section. The high pass (DC block) is used to remove any DC component of the received signal. The level shifter will then add the required DC level suitable for comparator input. Figure 2.6 illustrates the input filter as well as the level shifter implemented for the PCB part of the project.

Figure 2.6. Receiver input filter and level shifter for PCB, LTSpice

As we can see in Figure 2.6, the input filter consists of a single capacitor and the level shifter shifts the DC value with a resistive divider to half of the supply voltage. This configuration yielded fairly successful results for the PCB part of the project. The transfer function of the filter can be written as in Equation 2.3.

$$Z_{fPCB} = \frac{R_1||R_2}{R_1||R_2 + \frac{1}{j\omega C_1}} = \frac{R_1^2R_2^2}{(R_1+R_2)^2(\frac{1}{C_1^2\omega^2} + \frac{R_1^2R_2^2}{(R_1+R_2)^2})} + j\frac{R_1R_2}{C_1(R_1+R_2)\omega(\frac{1}{C_1^2\omega^2} + \frac{R_1^2R_2^2}{(R_1+R_2)^2})} \tag{2.3}$$

Plugging in the values from Figure 2.6 we get the value for transfer function in Equation 2.4.

$$Z_{fPCB} = 0.71 + j0.45 \tag{2.4}$$

This configuration has been set up differently for the IC part of the project for good reasons which will be discussed later. We will call the attenuation of signal from the isolation transformer to the comparator input to be A_{fPCB} in Equation 2.5.

$$A_{fPCB} = ||(Z_{fPCB})|| = 0.84 \tag{2.5}$$

A similar design is utilized for the IC part of the project, Figure 2.7 shows the input filter with level shifter for the IC part of the project.

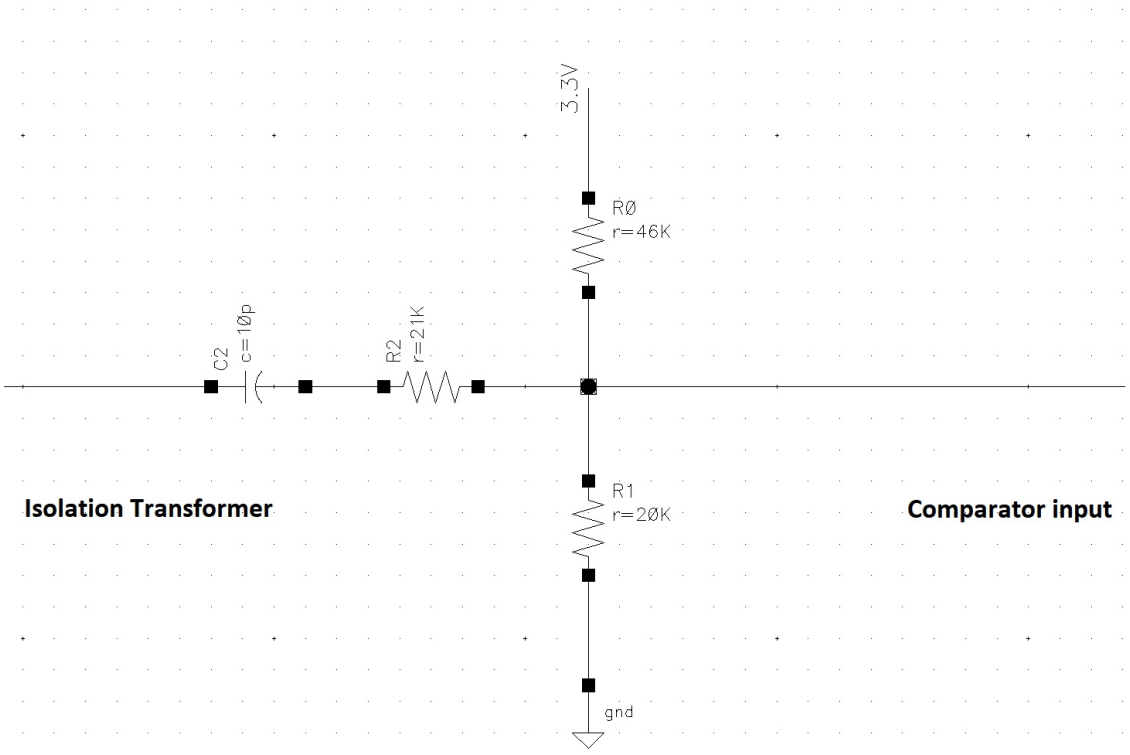


Figure 2.7. Receiver input filter and level shifter for IC, Cadence

Similar to the case in PCB, input filter consists of a capacitor DC block with an additional resistor $R_2 = 21$ kΩ. Transfer function is very similar to that of the PCB case with the difference of the attenuation factor. Referring to Figure 2.7 we have:

$$Z_{fIC} = \frac{R_0||R_1}{R_0||R_1 + R_2 + \frac{1}{j\omega C_2}} = \frac{R_0^2 R_1^2}{(R_0+R_1)^2(\frac{1}{C_2^2\omega^2} + (\frac{R_0R_1}{R0+R1} + R_2)^2)} + \frac{R_0R_1R_2}{(R_0+R_1)(\frac{1}{C_2^2\omega^2} + (\frac{R_0R_1}{R0+R1} + R_2)^2)} + j\frac{R_0R_1}{C_2(R_0+R_1)\omega(\frac{1}{C_2^2\omega^2} + (\frac{R_0R_1}{R_0+R_1} + R_2)^2)} \tag{2.6}$$

Plugging in the values in Figure 2.7 the following value for the transfer function of the input filter for IC design is found in Equation 2.7.

$$Z_{fIC} = 0.33 + j0.15 \tag{2.7}$$

Likewise, we will call the attenuation of signal from isolation transformer to the comparator input to be A_{flC} in Equation 2.8 for the IC part.

$$A_{fIC} = ||(Z_{fIC})|| = 0.36 \tag{2.8}$$

The reason we designed the attenuation to be much higher for the IC part will be evident in the receiver design part. The input to the comparator must not exceed 3.3 V since the differential input transistors used in umc130 technology are designed to endure maximum of 3.3 V. This limitation does not exist in PCB design since the comparators used are LM311 [13] chips which have an input swing up to 15 V. The DC level shifting of IC is designed to be at 1 V where the supply voltage is 3.3 V. This value is designed in such a way that it does not damage the differential input transistors. Finally, Figure 2.8 and Figure 2.9 show the frequency response of the input filters for PCB and IC respectively.

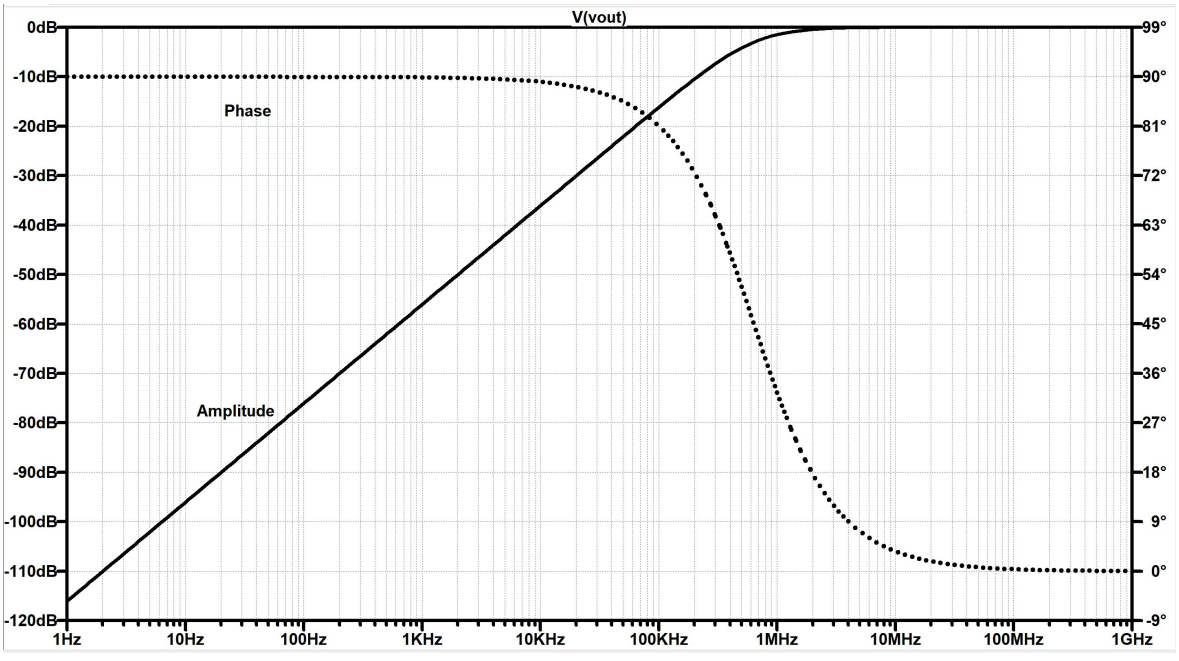


Figure 2.8. Receiver input filter frequency response, PCB

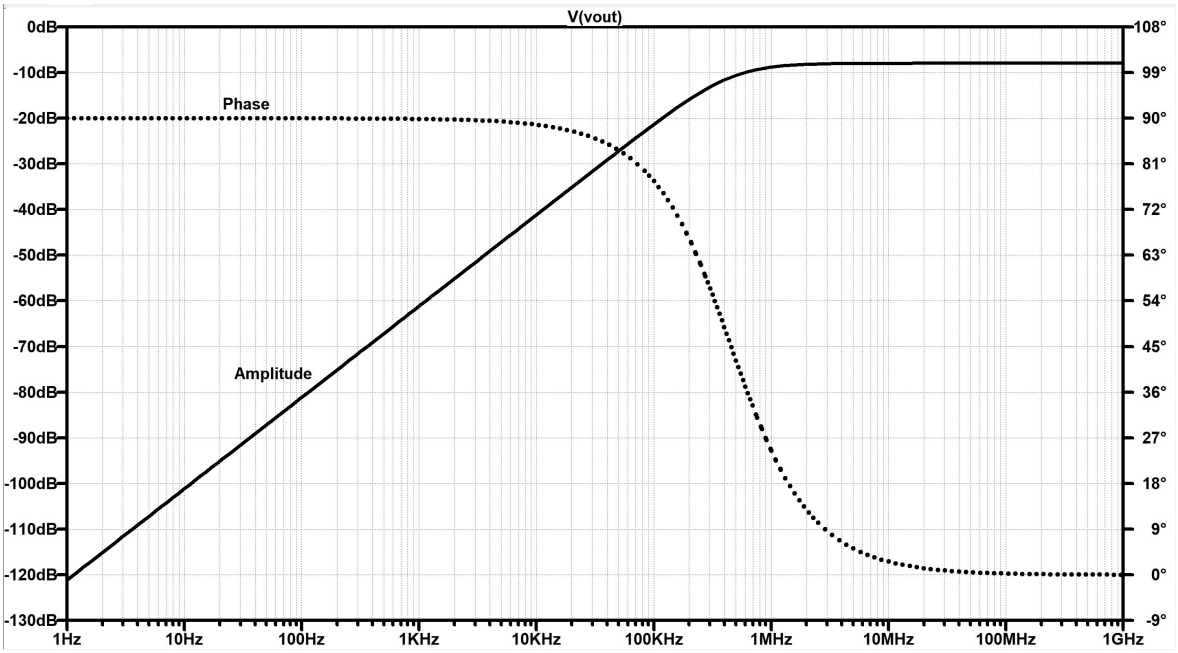


Figure 2.9. Receiver input filter frequency response, IC

2.3. Receiver Circuit

The requirement for the analog front end of a receiver circuit stated by 1553 standards are restricted to the terminal voltage. In other words, the receiver must be taking into account terminal threshold specifications while adjusting its comparator thresholds. From the terminal end of the transceiver to the receiving circuitry, there could be nonlinear attenuation that must be taken into account. This could arise from the isolation transformer, receiving input filter, and other circuit blocks which are important for the receiver operation, but with terminal signal attenuation. By now, it seems evident that we will be employing comparator circuits at the receiver. This however, will be different in the PCB than the IC part in details and technicality of the implementation but from the system point of view, they both will employ comparator circuits. As mentioned in Table 2.1 requirement HRS_008, when the terminal peak to peak voltage rises above 0.86 Vp-p (0.43 Vp) up to 14 V, the receiver must receive a bit signal, and ignore voltages below 0.2 Vp-p (0.1 Vp). It should also be mentioned that these threshold requirements are stated for transformer coupled stubs which is

our target design. These terminal threshold voltage requirements can be translated into comparator circuit requirements by keeping in mind that there will be attenuation from terminal end to the comparator inputs. A Schmitt-trigger (aka comparator with hysteresis) circuit is the subject of design for the receiver part. Figure 2.10 shows one end of the receiver designed with hysteresis enabled for the PCB.

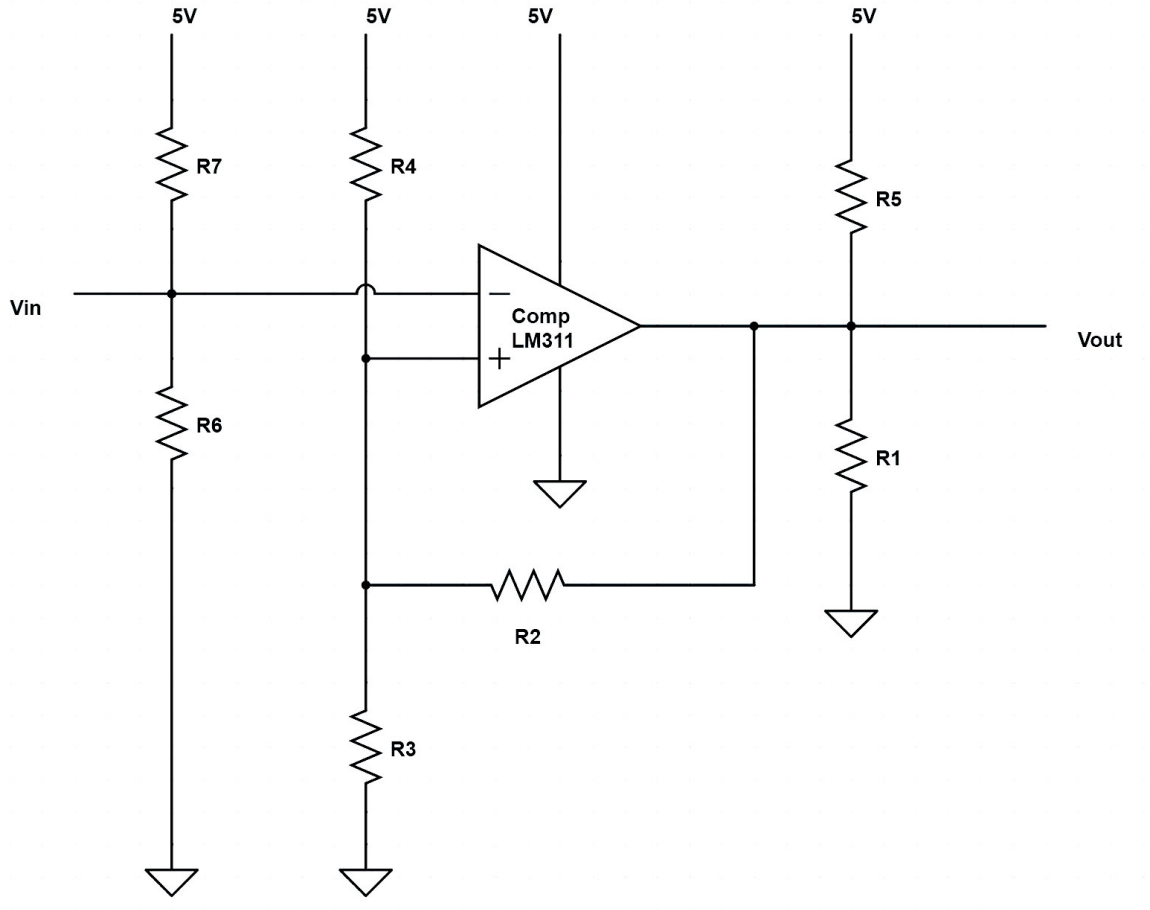


Figure 2.10. Receiver Comparator (with hysteresis), PCB

There will be two comparators with resistor networks shown in Figure 2.10 for RCV_OUT+ and RCV_OUT- outputs. Before getting into how this would affect the zero crossing delay in the receiver, let us first investigate the threshold levels for the comparator. R_6 and R_7 in Figure 2.10 will add a DC level to the input alternating signal connected to the comparator negative input (see Figures 2.7 and 2.6). This is necessary as we will see shortly that without this DC level shifting, R_4 and R_3 values

need to be quite different and resistor error values become a huge issue for the receiver. But for the time being, let us focus on the comparator side of the receiver, we will be investigating how this signal arrives at the V_{in} pin at later stages. In order to calculate the switching threshold levels of the circuit, we will consider the equivalent circuits at both ON and OFF states of the comparator. Figures 2.11 and 2.12 show the equivalent circuits respectively.

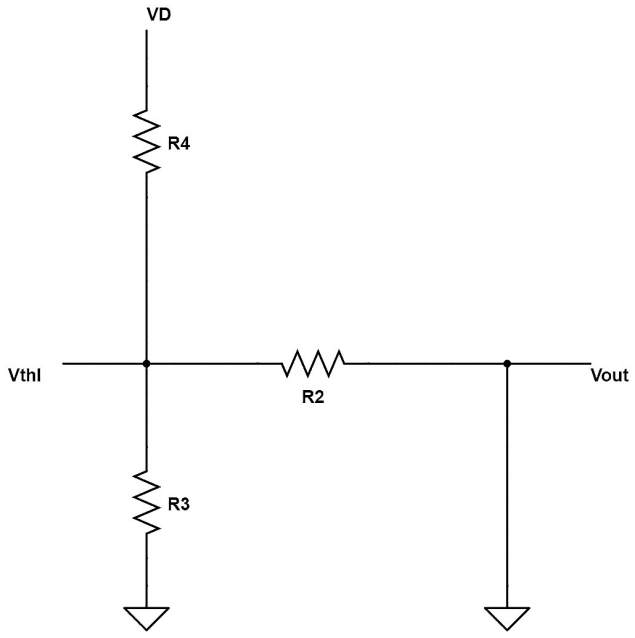


Figure 2.11. Comparator ON equivalent circuit, PCB

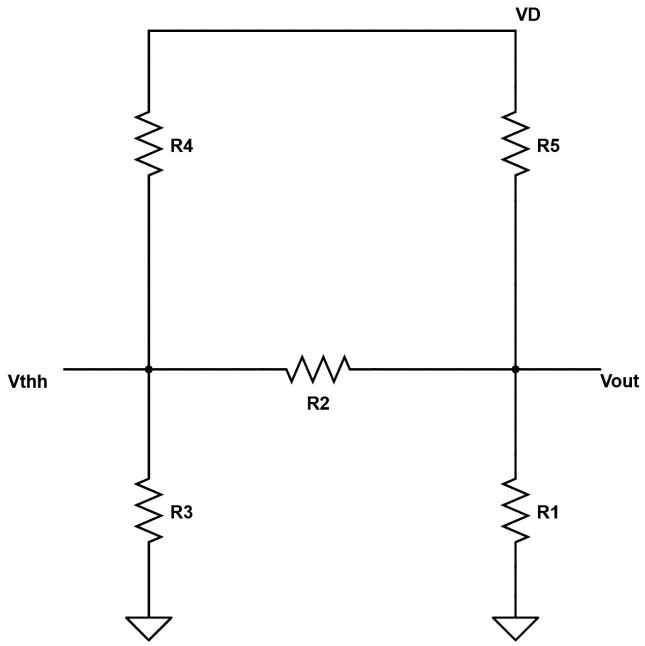


Figure 2.12. Comparator OFF equivalent circuit, PCB

V_{thl} and V_{thh} refer to the low and high threshold voltages respectively for hysteresis arising from the feedback resistor R_2. Conveniently, the design aims to target the 0.86 Vp-p terminal threshold criterion to match the high threshold value of the comparator, and 0.2 Vp-p terminal threshold criterion for the low threshold of the comparator. By design, we evidently understand that the voltages between 0.86 Vp-p and 0.2 Vp-p will be rejected by the comparator and this is what practically 1553 standard requires the receiver to abide to. On top of that, Schmitt-trigger rejects possible noise in the circuit (more on this on subsection 2.3.1). Simple circuit analysis yields the following derivations.

$$\frac{V_{thh} - V_D}{R_4} + \frac{V_{thh}}{R_3} + \frac{V_{thh} - V_{out}}{R_2} = 0 \tag{2.9}$$

$$\frac{V_{out} - V_D}{R_5} + \frac{V_{out} - V_{thh}}{R_2} + \frac{V_{out}}{R_1} = 0 \tag{2.10}$$

$$V_{thl} = \frac{\frac{R_2 R_3}{R_2+R_3}}{\frac{R_2 R_3}{R_2+R_3} + R_4} V_D \tag{2.11}$$

There are 9 unknowns in Equations 2.9, 2.10 and 2.11 namely: R_1, R_2, R_3, R_4, R_5, V_{thl}, V_{thh}, V_{out}, V_D. By design we know the values for some of those unknowns: $V_D = 5$ V, $V_{out} = 3.3$ V. Rest of the unknowns need to be determined. We already established values for R_6 and R_7 in section 2.2. Value of the feedback resistor R_2 must be chosen relatively large. A few trials indicate $R_2 = 240\text{k}\Omega$ is a suitable value. The pull-up resistor R_5 must be small for fast rise time, so R_5 is chosen as 500Ω. By finding the right values for V_{thh} and V_{thl} we would be down to three equations and three unknowns and a proper solution will be at hand. To connect the required terminal threshold value to the comparator threshold values we will be making use of the attenuation we deduced in Equation 2.5 and isolation transformer turns ratio in Equation 2.2. Equation 2.12 shows the total attenuation for the PCB:

$$A_{TPCB} = \frac{1}{n} A_{fPCB} = \frac{1}{2.42} 0.84 = 0.35 \tag{2.12}$$

Similarly the total attenuation for IC using Equations 2.8 and 2.2 is:

$$A_{TIC} = \frac{1}{n} A_{fIC} = \frac{1}{2.42} 0.36 = 0.15 \tag{2.13}$$

From this point, the following threshold values for the comparator input can theoretically be deduced for both IC and PCB designs. Equations 2.14 and 2.15 explain this approximation.

$$\begin{aligned} v_{thh,PCB} &= \frac{1}{2} A_{TPCB} V_{THH1553} = \frac{1}{2}(0.35)(0.86) = 0.150V \\ v_{thl,PCB} &= \frac{1}{2} A_{TPCB} V_{THL1553} = \frac{1}{2}(0.35)(0.2) = 0.035V \end{aligned} \tag{2.14}$$

$$\begin{aligned} v_{thh,IC} &= \frac{1}{2} A_{TIC} V_{THH1553} = \frac{1}{2}(0.15)(0.86) = 0.064V \\ v_{thl,IC} &= \frac{1}{2} A_{TIC} V_{THL1553} = \frac{1}{2}(0.15)(0.2) = 0.015V \end{aligned} \tag{2.15}$$

Note that the voltages in Equations 2.14 and 2.15 are the required threshold values without the DC level shifting. Division by two is required since the comparator reference voltage will be kept at around the halfway peak to peak voltage. Namely, each winding of the transformer at the receiving side will carry peak to peak voltage passed on from the terminal side.

Once we have a rough idea of what peak threshold values should be, we can finally go ahead and solve Equations 2.9, 2.10 and 2.11 to find a solution for R_1, R_3 and R_4. Since the signal is DC blocked by the input filter and a specific DC level is added by the level shifter, the following values hold for V_{thh} and V_{thl}:

$$\begin{aligned} V_{thh} &= \frac{R_6}{R_6+R_7}V_D + v_{thh,PCB} = \frac{5}{5+5}5 + 0.150 = 2.650V \\ V_{thl} &= \frac{R_6}{R_6+R_7}V_D + v_{thl,PCB} = \frac{5}{5+5}5 + 0.035 = 2.535V \end{aligned} \tag{2.16}$$

The solution for the PCB is summarized as follows:

$$\begin{gathered} \frac{2.65-5}{R_4} + \frac{2.65}{R_3} + \frac{2.65-3.3}{240} = 0 \\ \frac{3.3-5}{0.5} + \frac{3.3-2.535}{240} + \frac{3.3}{R_1} = 0 \\ 2.535 = \frac{\frac{240R_3}{240+R_3}}{\frac{240R_3}{240+R_3}+R_4}5 \\ R_1 \approx 1k\Omega, R_3 \approx 18.2k\Omega, R_4 \approx 16.5k\Omega \end{gathered} \tag{2.17}$$

The IC part is similar to that of PCB, the only difference would be that the comparator is designed to work with 3.3V supply, it therefore does not need the output leveling, since the output voltage swing will be between 0V and 3.3V by design. Figures 2.13 and 2.14 show the comparator design of the receiver end for PCB, its equivalent circuit when the comparator is OFF respectively. The equivalent circuit when the comparator is ON is identical to that of PCB ON case in Figure 2.11.

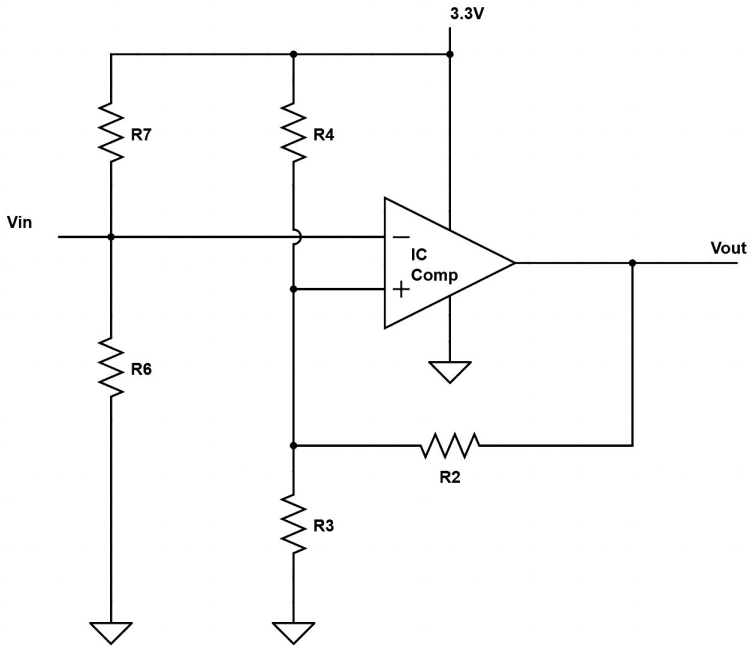


Figure 2.13. Receiver Comparator (with hysteresis), IC

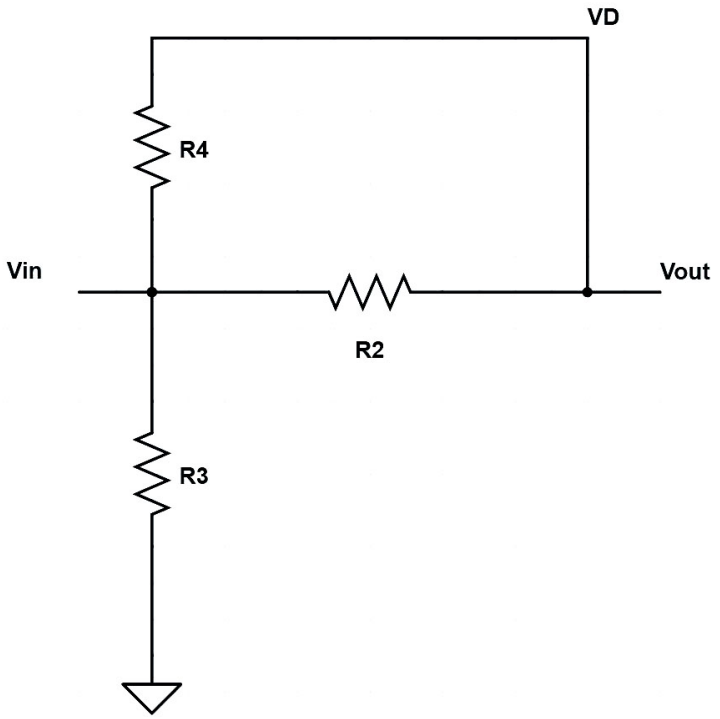


Figure 2.14. Comparator OFF equivalent circuit, IC

Equations 2.18 and 2.19 derive similarly for the IC receiver network:

$$V_{thh} = \frac{R_3}{R3 + \frac{R_2 R_4}{R_2 + R_4}} V_D \tag{2.18}$$

$$V_{thl} = \frac{\frac{R_2 R_3}{R_2 + R_3}}{\frac{R_2 R_3}{R_2 + R_3} + R_4} V_D \tag{2.19}$$

Using Equation 2.15 and referring to the Figures 2.7 and 2.13 we have:

$$\begin{aligned} V_{thh} &= \frac{R_6}{R_6 + R_7} V_D + v_{thh,IC} = \frac{20}{20 + 46} 3.3 + 0.064 = 1.064V \\ V_{thl} &= \frac{R_6}{R_6 + R_7} V_D + v_{thl,IC} = \frac{20}{20 + 46} 3.3 + 0.015 = 1.015V \end{aligned} \tag{2.20}$$

By choosing R_2=200kΩ and V_D=3.3 V, the solution for the IC network is acquired as follows:

$$\begin{aligned} 1.064 &= \frac{R_3}{R3 + \frac{200 R_4}{200 + R_4}} 3.3 \\ 1.015 &= \frac{\frac{200 R_3}{200 + R_3}}{\frac{200 R_3}{200 + R_3} + R_4} 3.3 \\ R_3 &\approx 4.4k\Omega, R_4 \approx 9.6k\Omega \end{aligned} \tag{2.21}$$

The actual attenuation caused by the input filter in the PCB and IC are different than what we calculated in Equations 2.5 and 2.8. This discrepancy occurs because the signal arriving to the comparator input is not fully sinusoidal as depicted in Figure 3.5, Chapter 3. As a matter of fact the arriving signal in the terminal is a square wave as opposed to sinusoidal. Equations 2.5 and 2.8 make use of the absolute value of the transfer function input filter. Since this slight discrepancy is seen, for the sake of being accurate in the terminal minimum voltage specifications of 1554, 0.86 Vp-p is applied at the terminal and attenuation is observed experimentally. Also, it was in the PCB boards better interest to produce smaller zero crossing delays after first prototype was manufactured. V_{thh} and V_{thl} values were chosen just a few tens of millivolts below V_{thh}

and resistor values were calculated [1] . Figures 2.15 shows how input voltage to the comparator changes by inducing different voltages on the terminal found from SPICE simulation. Figure 2.16 depicts how different terminal voltages affect the attenuation.

[1] Choosing threshold high and low to be the exact same value produces no solution in the equations for R_3 and R_4, however, assigning $R_3 = R_4$ in the simulation circuit, still produces alternating reference voltage around 10mV peak to peak. i.e. the gap between threshold high and low can be zero in the presence of the R_2 feedback resistor which creates very small hysteresis window.

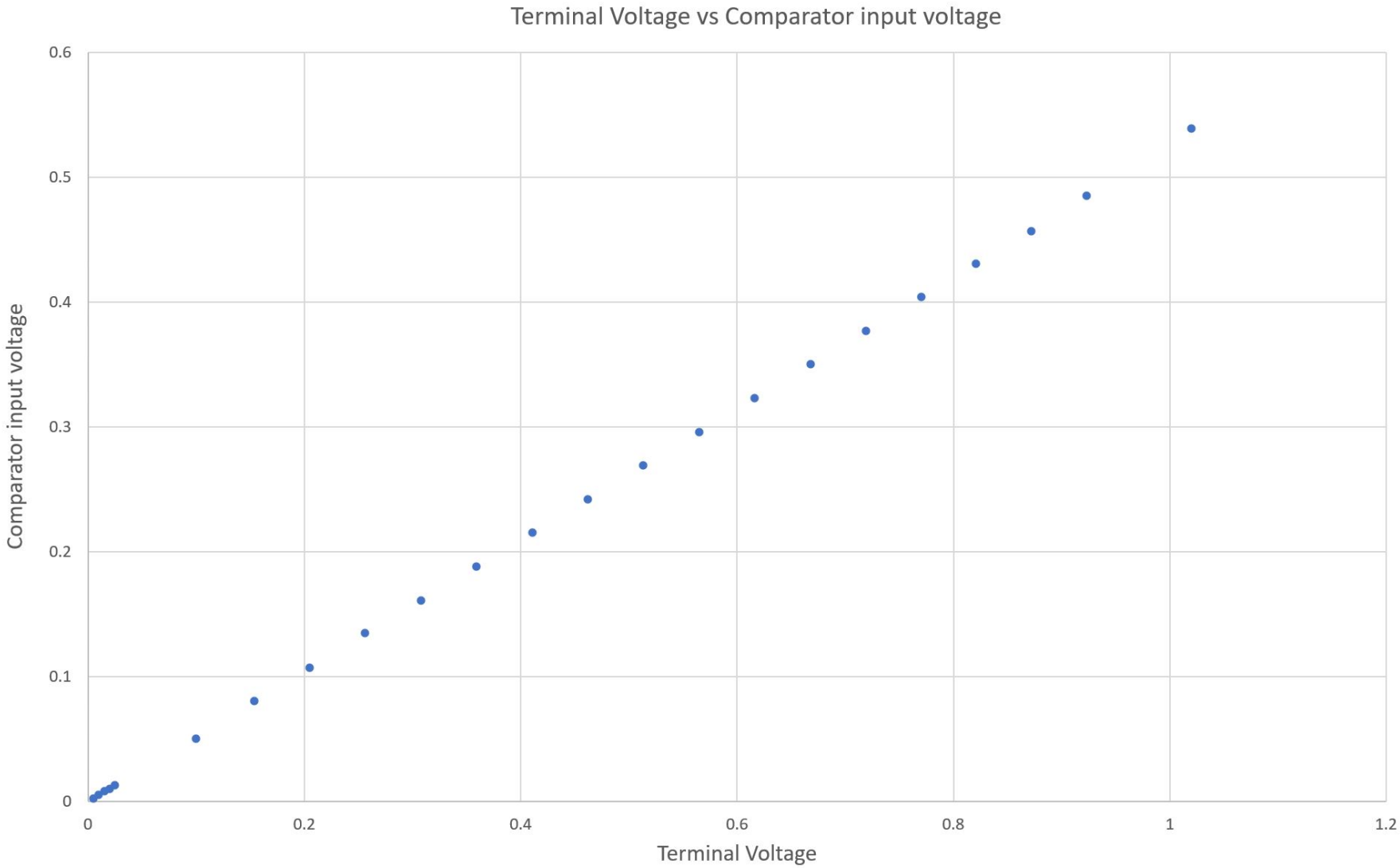


Figure 2.15. Terminal Voltage vs Comparator input voltage

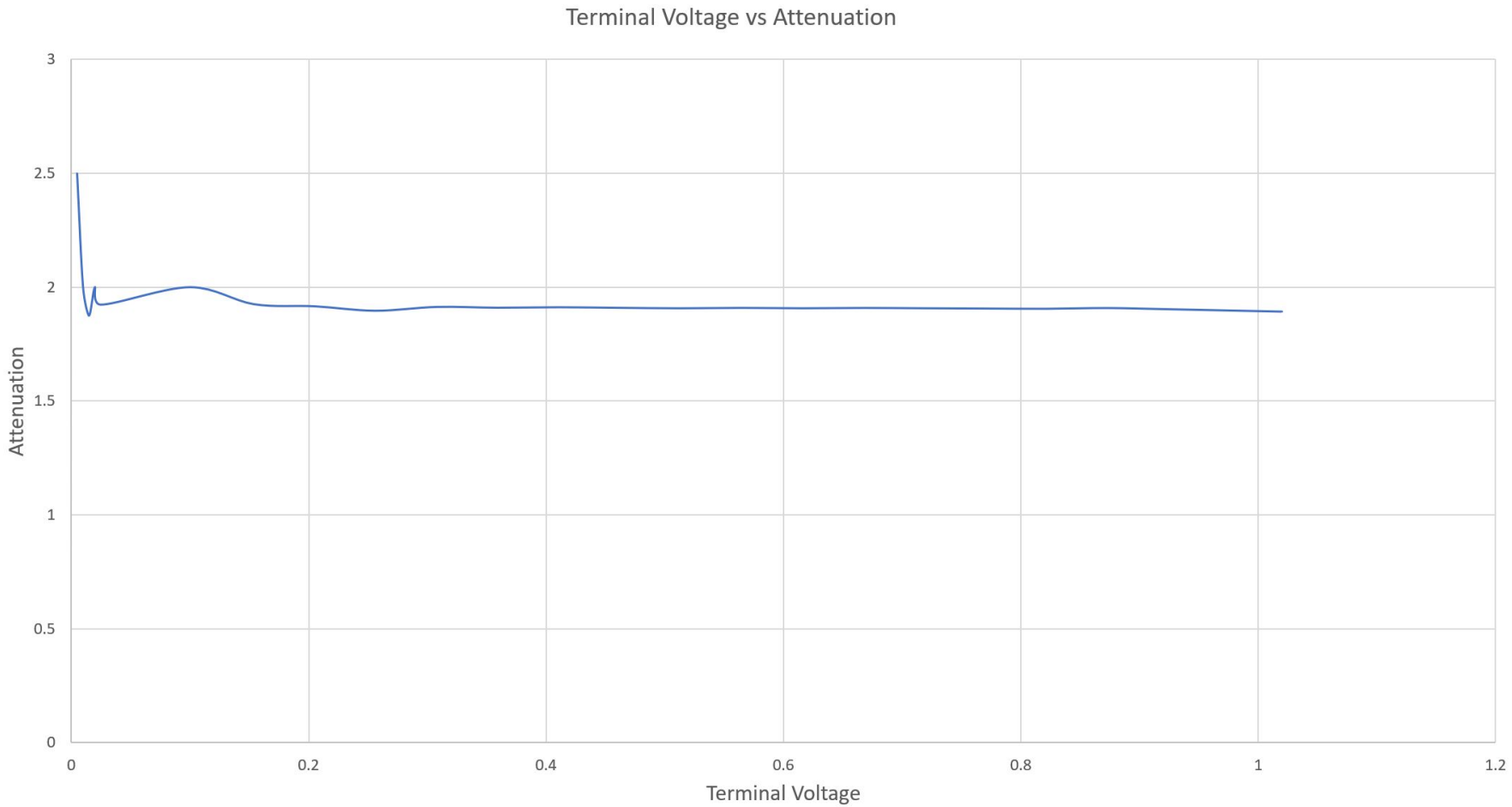


Figure 2.16. Terminal Voltage vs Attenuation

Although the terminal voltage vs attenuation relation seems linear in Figure 2.15, we can see in Figure 2.16 that at lower terminal voltages the attenuation is not stable. However, for our target which is 0.86 Vp-p, the attenuation seems to be constant at around $0.52 = \frac{1}{1.9}$. This value does not match with the value found at Equation 2.12 understandably since the nature of signal arriving to the comparator input (as will be seen in experiment and results section) is far from pure sinusoidal.

Moving on from the external resistor network design, we will now be looking at the comparator CMOS circuit design for the IC part of the project. The comparator used in PCB circuit is LM311 IC. Figure 2.17 is the schematic of the comparator designed in cadence using umc130nm process technology.

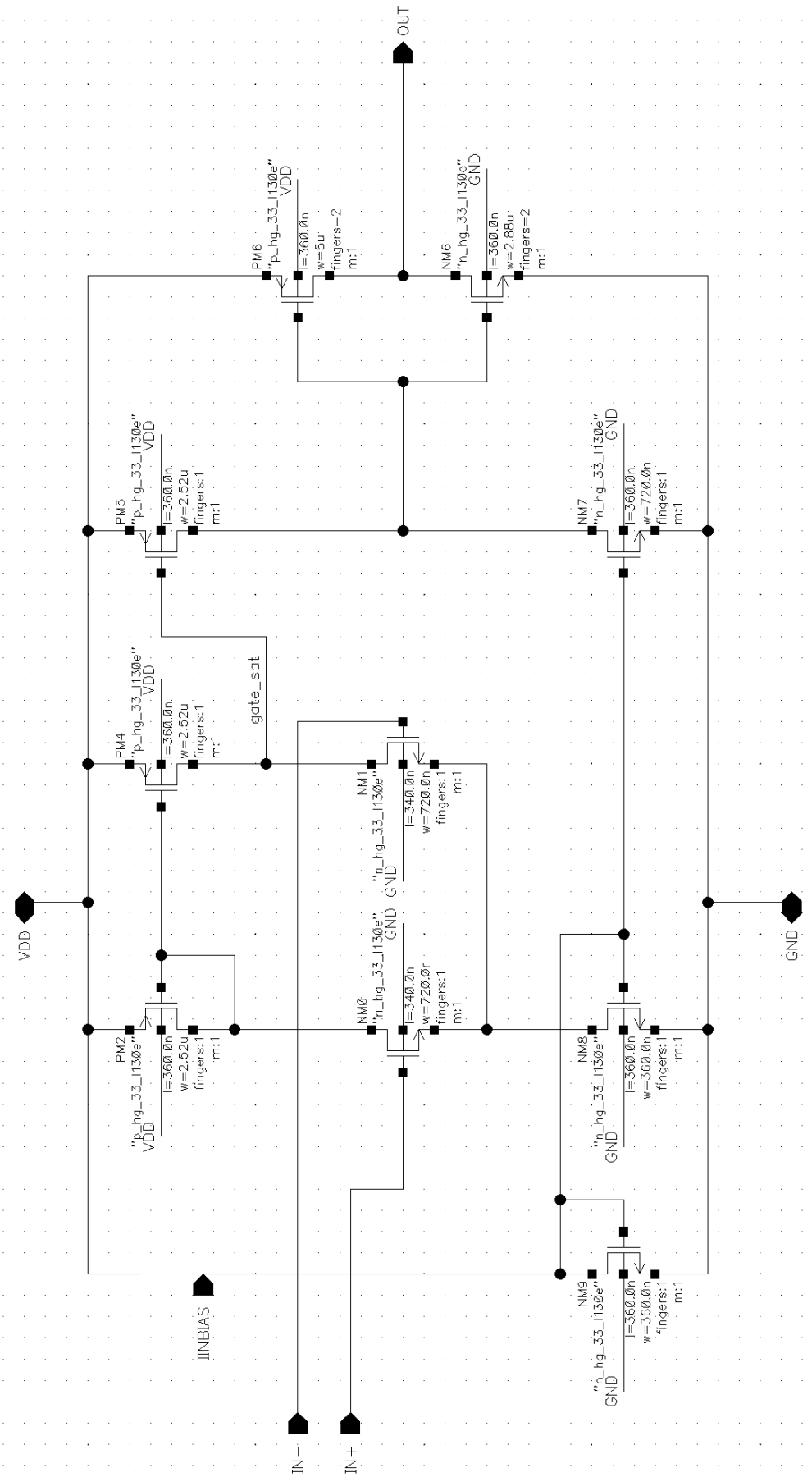


Figure 2.17. Comparator CMOS schematic used for the receiver of IC. Using umc130nm process.

The following analysis has been done to determine the transistor sizing given the few design requirements we had at hand [14]. Signal resolution of about 15mV is enough at this stage. Output rise and fall times shall not pass 100ns and shorter times are better for the receiver performance.

$$V_{DD} = 3.3V, res = 15mV, LoadCapacitance \approx 1pF \tag{2.22}$$

$$Gain > \frac{3.3}{0.015} = 220 \tag{2.23}$$

$$SR = \frac{3.3V}{100ns} = 33V/\mu s \tag{2.24}$$

$$I_{DN6} = LoadCapacitance \times SR = 10^{-12} \times \frac{3.3}{100 \times 10^{-9}} = 33\mu A \tag{2.25}$$

$$OverDrive = V_{DN6,sat} = 0.25V \tag{2.26}$$

$$(\frac{W}{L})_{N6} = \frac{2I_{DN6}}{K_N(V_{OV}^2)} \tag{2.27}$$

$$(\frac{W}{L})_{P6} = \frac{2I_{DP6}}{K_P(V_{OV}^2)} \tag{2.28}$$

From Equations 2.22 to 2.28 the sizing of the transistors are determined. Basically what we have here is a differential pair input amplifier with fast switching capabilities. Current mirror sizing is adjusted as such to have put transistors in SAT operation region. IBIAS input has been configured to an ideal current source of magnitude 28μA.

2.3.1. Receiver zero crossing delay effect

As explained earlier, fixed thresholds assigned to both receiver comparators introduce zero crossing delays at the received complementary digital signal. Figure 2.18 illustrates this effect and the following points are made.

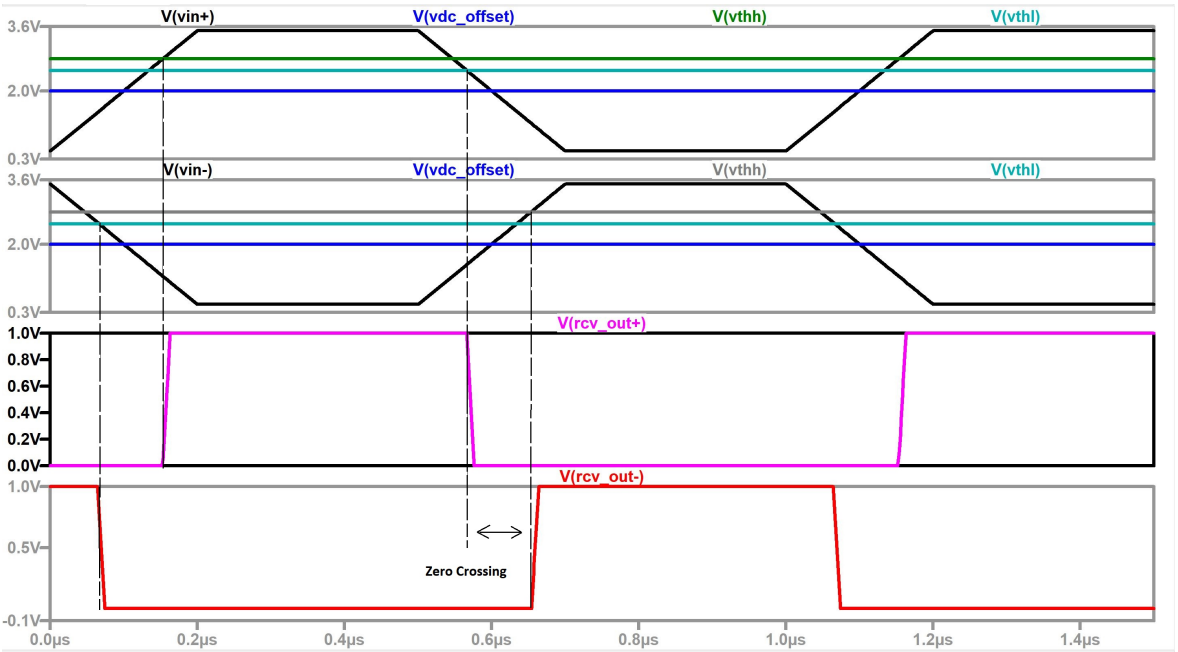


Figure 2.18. Receiver zero crossing delay illustrated. Voltage levels along with rise and fall times are exaggerated to highlight the effect

- Threshold high and low could be associated with 1553 terminal threshold requirements which serves the purpose well.
- The larger the gap between the threshold high and low voltages is, the greater the zero crossing delay effect becomes which is an unwanted result. However the noise rejection of the receiver increases in that case (input signal altering in the region, does not trigger the output switch of the comparator).
- We can observe that tightening the space between threshold high and threshold low voltage values would reduce the zero crossing delay but, considerably smaller reduction in zero crossing delay compared to the case where we get them both closer to the DC offset (mid voltage) value introduced by the input level shifter.

However, design requirement of 0.43 Vp on the terminal is required and zero crossing delay is inevitable (i.e. by getting threshold high and threshold low voltages close to DC offset, switching may occur at very low values of the terminal voltage).

- The faster the $V_{in}+$ and $V_{in}-$ rise and fall times are, the smaller the zero crossing delay becomes.
- By introducing threshold high and low values (Schmitt-trigger) we can eliminate the need for input filter for noise reduction.
- Capacitor C_1 in Figure 2.6 and C_2 in Figure 2.7 determine how fast the input voltage from the terminal settles down to 0V DC (has its DC value removed) to be fed to comparator inputs at the receiver. Therefore, smaller values for these capacitors will allow faster settling time and smaller zero crossing delays at the first bits received. Although this effect was not observed in the simulations LTSpice (PCB) and Cadence (IC), PCB measurements suffer from a large zero crossing delay for the very first bit received due to the possible unwanted capacitive effects on the board. By introducing a large DC blocking capacitance we can observe the first bit zero crossing delay effect as depicted in Figure 2.19 in SPICE simulation.
- Zero crossing delay time value can be estimated by using the small signal threshold values calculated in Equations 2.15 and 2.14. $ZC = \frac{(v_{thh}+v_{thl})}{SR}$ where SR is the slew rate of the signal receiving to the comparator inputs namely V_{in} in Figures 2.13 and 2.10.

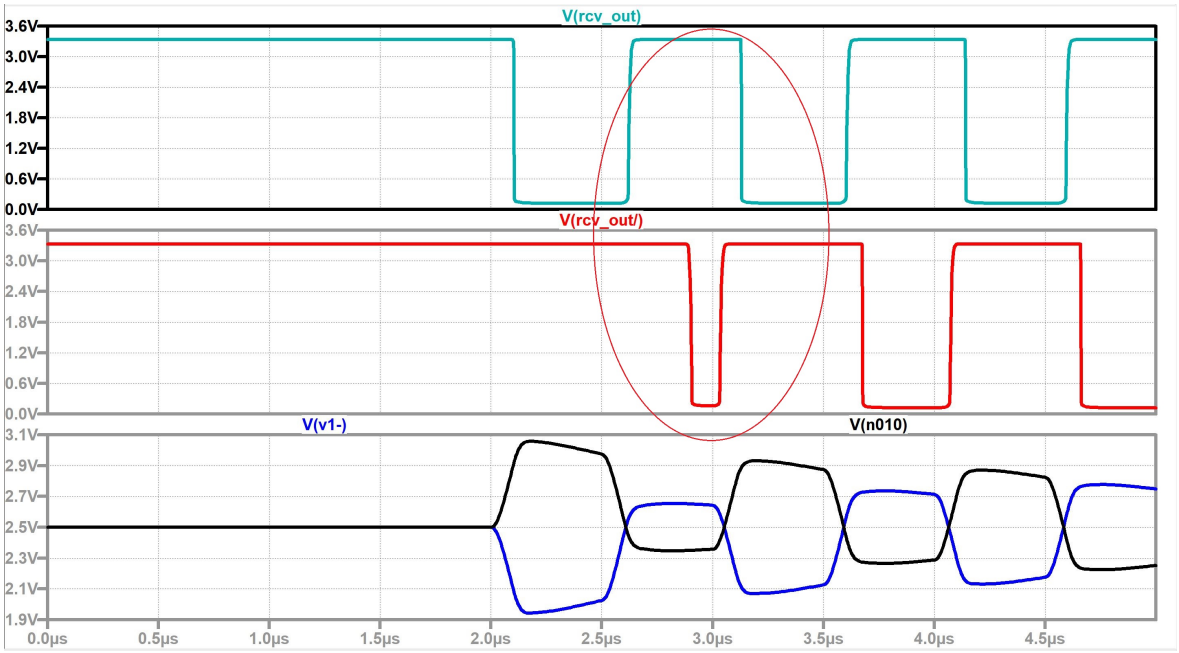


Figure 2.19. Receiver zero crossing delay for the first bit received in SPICE. To observe the effect, value of input DC capacitance is increased to values close to 550pF

2.4. Transmitter Circuits

As stated in Table 2.1, there are quite a few terminal signal transmission requirements that need to be met as far as 1553 standards are concerned. Some of these requirements are the backbone in the success for the IP devices communicating properly in the aircraft. In order to build the transmitter part of the circuit, it is useful to investigate how high speed data links operate as pointed out earlier. The transmitter must generate an accurate voltage swing on the channel while also maintaining proper output impedance in order to attenuate any channel-induced reflections. Either current- or voltage-mode drivers, shown in Figure 2.20 and Figure 2.21, are suitable output stages [6].

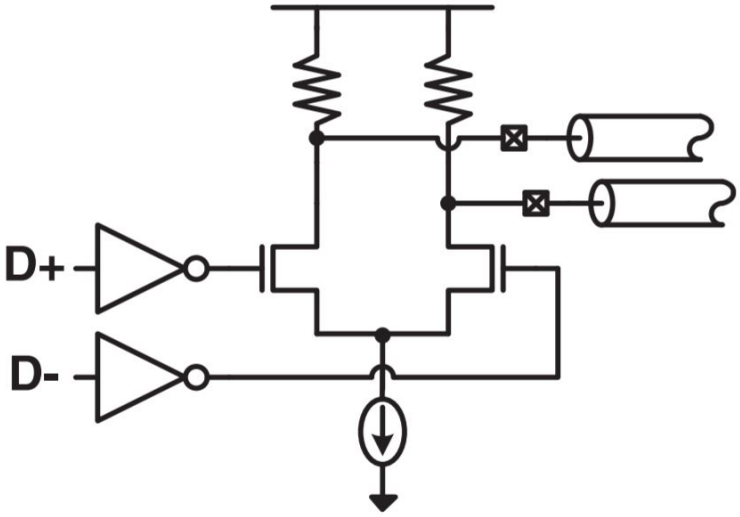


Figure 2.20. current-mode driver [6]

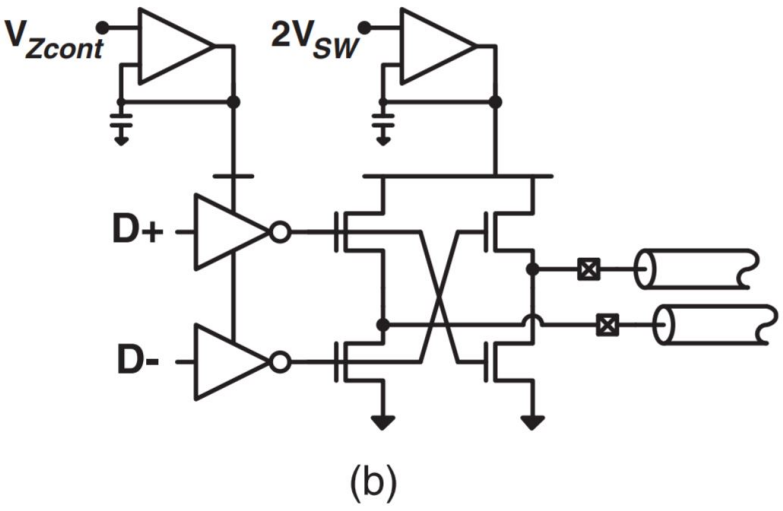


Figure 2.21. voltage-mode driver [6]

Although the driver in Figure 2.20 is designed for electrical links with voltage swings up to ± 500mV, it gives us some idea on how we should tackle the transmission circuit design. First of all, the required voltage on the terminal loaded with 70Ω load is around 22 Vp-p. This makes the current required to be delivered to be around $\frac{22}{70} = 314mA$. Translated to the primary side of the isolation transformer makes $n \times$

$314mA = 2.42 \times 314 = 760mA$. Noting that this current on the primary side is peak to peak current required, we also know that we have two winding in primary side as well and if we were to make proper use of this, we would be driving one winding in positive half cycle of the transmission, and other winding for the negative half cycle. This way at each half cycle the current through each winding would be $\frac{760mA}{2} = 380mA$ as opposed to $760mA$. However, practically we would have a peak to peak current of 760mA but 180 degrees out of phase. Therefore, by making use of the complementary transmission signal input, it seems if we were to control current flow through the windings by having input signal control one of them, and complementary input the other, in a full transmission cycle (one period) we would be driving one winding in one half, and the other winding in the other half of the cycle. By adjusting the topology presented in Figure 2.20 which is similar to LVDS systems (Low Voltage Differential Signaling), we came up with the configuration in Figure 2.22. Controlling the current flow through the winding is done by means of MOSFET switches. As we will be seeing in subsequent sections, these switches must be capable of high currents, around 380 mA, and have relatively large gate capacitance and large threshold value. More on this will be discussed when investigating designs for PCB and IC separately (switching too fast causes overshoots and instability, too slow causes breaking point in transmitted signal).

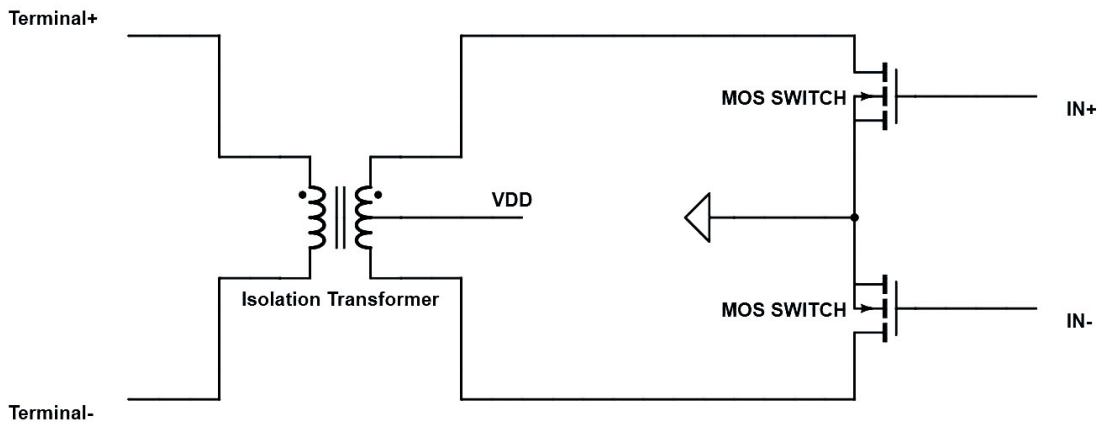


Figure 2.22. Transmitter circuit topology

Now let us investigate how this circuit operates in functional level. When IN+ is ON (and IN- OFF) the voltages appearing on the nodes are depicted in Figure 2.23 and the complementary case in Figure 2.24.

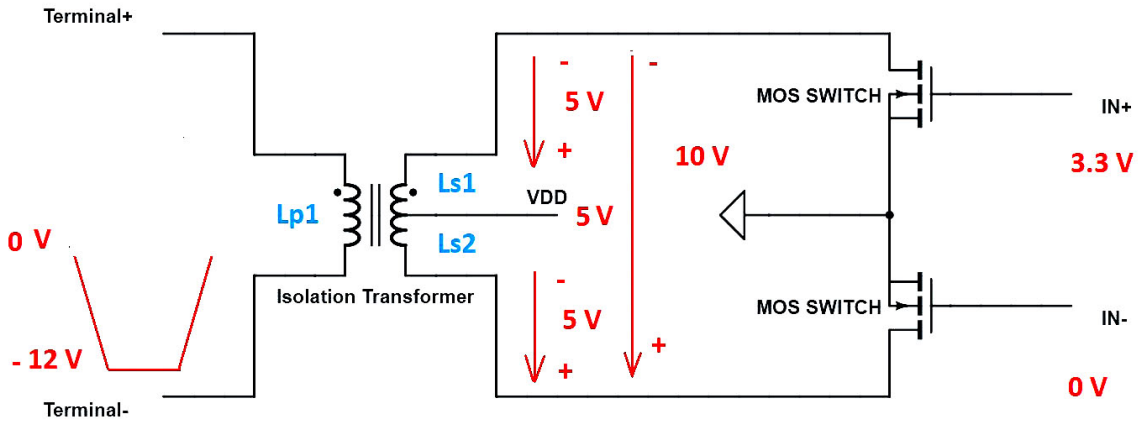


Figure 2.23. Transmitter circuit voltages, IN+ ON

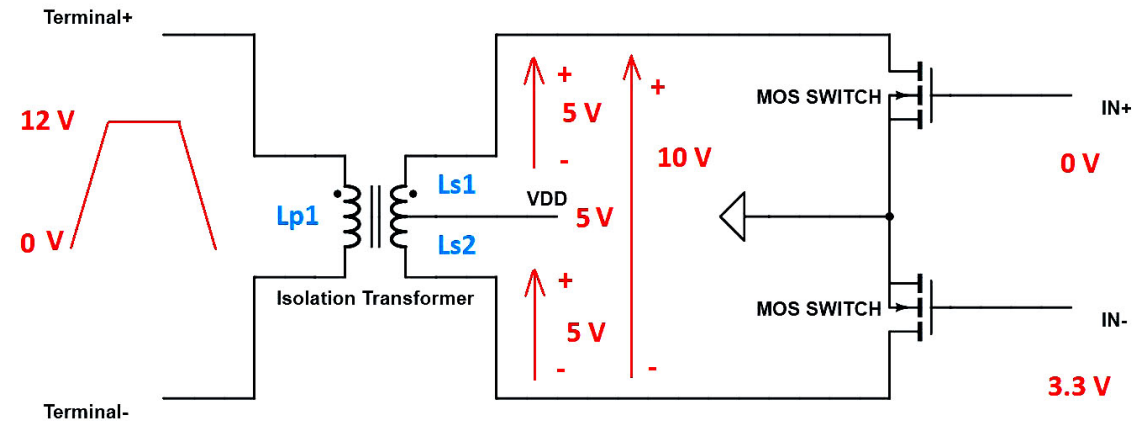


Figure 2.24. Transmitter circuit voltages, IN- ON

Demonstrative values in Figures 2.23 and 2.24 have been chosen to fit the actual design parameters. V_{DD} = 5 V, Input-high = 3.3 V, Input-low = 3.3 V, n = 2.42. Switch is ON when input is 3.3 V (driven from a TTL output). Transformer driving

voltage is 5V. Value of the turns ratio of the transformer from primary to the secondary is calculated in Equation 2.2.

Since the center is tapped to 5V supply, when IN+ is high the switch opens and there is a direct path to the ground (ideally). This forces 5V across Ls1, which in turn is directly coupled to Ls2 with ratio 1 ($\frac{2.11mH}{2.11mH}$) and having passed current through it, induces 5V across Ls2 with same polarity (same direction of turns with mutual core) and as a result there appears a 10V voltage from negative end of Ls1 to the positive end of Ls2. This effect is similar to a seesaw centered at the driving voltage. The 12V voltage at each cycle of the terminal side is calculated simply by multiplying the voltage over the driving winding by the turns ratio: $V_{half-cycle} = 2.42 \times 5 = 12.1$. This would make a full cycle of $12 \times 2 = 24V_{p-p}$ on the terminal side at each transmission. It is safe to say that the transmission peak to peak can be effectively calculated as $V_{transmission\_p-p} = (V_{DD} \times 2) \times n$ under this setup.

As mentioned before, a sudden and abrupt switching would be detrimental to the operation of the circuit. The reason would be the fact that during one half cycle driving, while one winding is conducting, there would be energy stored in that winding even after the switch is closed. Now, if the other half cycle switch opens right after it, it would force a current in the reverse direction. Although current across an inductor does not change abruptly, this would evidently cause the previous charges contributing to the current which have energy from previous transmission, to clash with the new charges contributing to the new current in the reversed polarity of the abruptly induced voltage. This charge accumulation manifests itself as unwanted overshoots on the primary windings of the transformer and therefore on transmitted signal (although lesser on transmitted signal than on primary side). At some cases, it also disrupts the whole operation of the transmission by manifesting itself as low frequency oscillations on the primary side (i.e. a few milliseconds later operation settles to seesaw model described above, this settling has been seen to oscillate with an envelope of around 1kHz).

A solution to the overshoot problem above, and generally more healthy transmission, is to drive the switches in a non overlapping manner. Figure 2.25 shows an example of overlapping and non-overlapping signals. If the delay gap between the input signals becomes large, this time the shape of the transmitted signal looses its smoothness and practical rise and fall times pass the allowed limits. Figure 2.26 shows an example of such ill-formed transmitted signal.

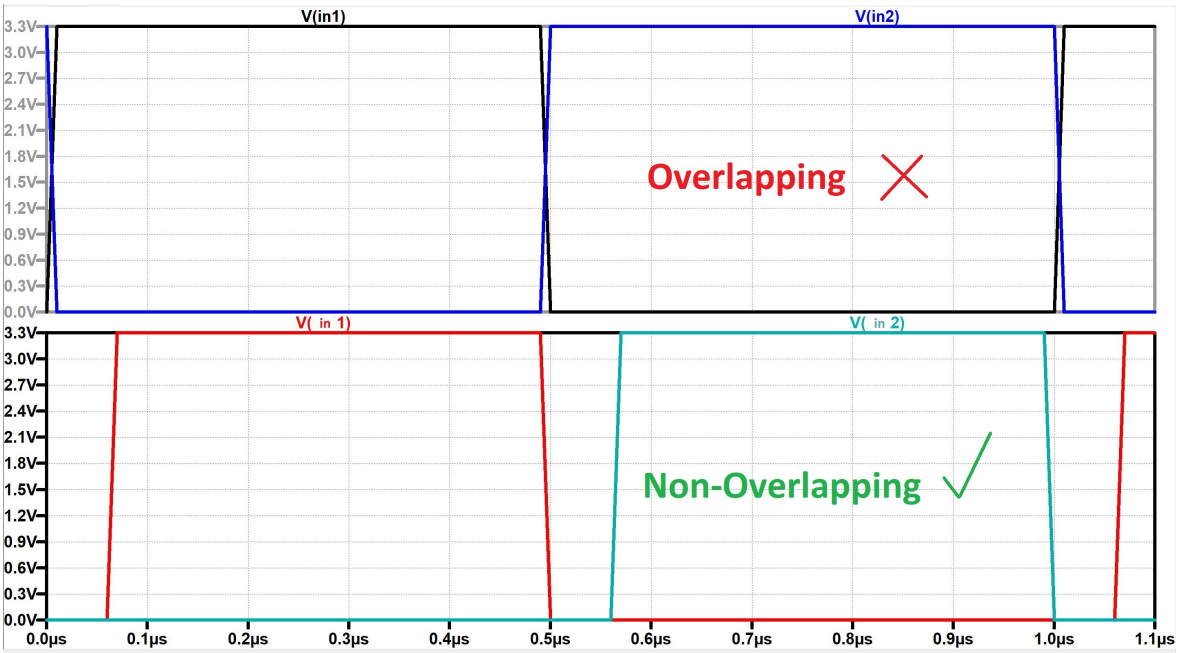


Figure 2.25. Example of overlapping and non-overlapping driving signals. Non-overlapping is desired

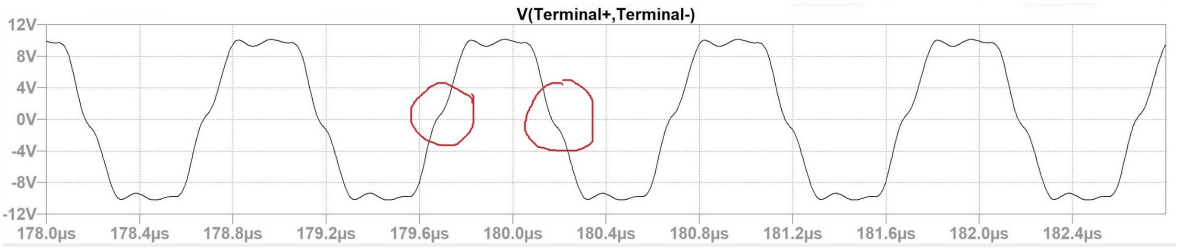


Figure 2.26. ill-formed transmission signal due to large delay between non-overlapping signals

A point to add to the non-overlapping gate driving signals in Figure 2.25 is that the slope at which this gate is being driven also plays an important role for the transmission signal shape, as well as overshoots and current consumption. Basically the signal rise and fall times have been set to 10ns. Usually this slope needs to be larger, but then again not too large. This is often referred to as "Slope Control" in the transmitter driving circuitry. Slope control, non-overlapping signal generation, and delay between non-overlapping signals will be discussed more in detail in IC part.

To estimate and understand the operation of the transmitter mathematically, lets model the driving gate NMOS with ideal switch and estimate the circuit model for the transformer. Figure 2.27 shows the circuit model we will be investigating, and Figure 2.28 is used to model a step input of 5V at time equal to zero with zero initial conditions [15].

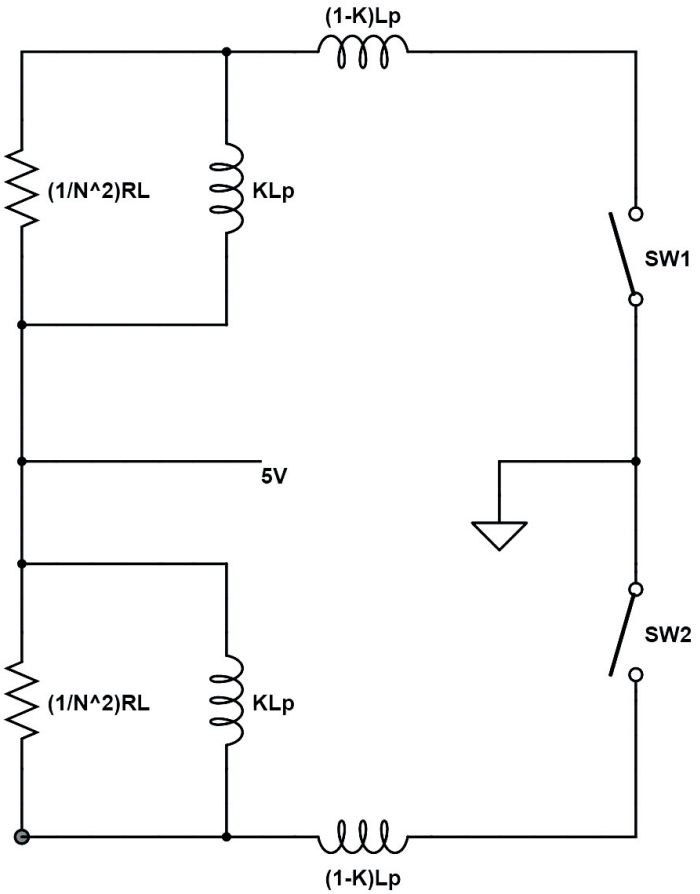


Figure 2.27. Transformer model with load referred to primary side and leakage present

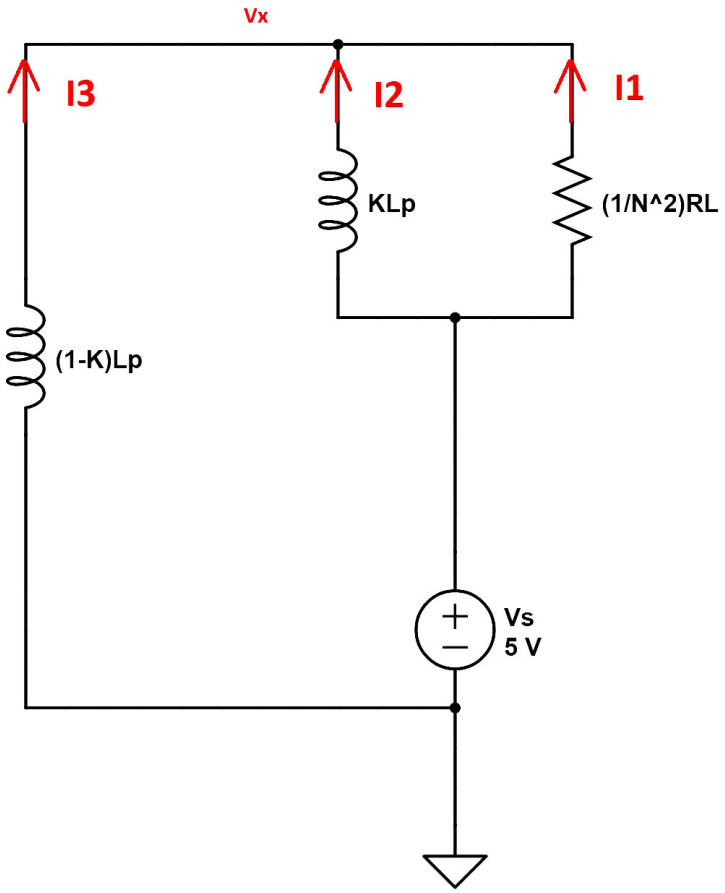


Figure 2.28. Transformer model with step input transient model

Simple circuit analysis yield the following differential equations in Equation 2.29 and Equation 2.30.

$$i_1 + i_2 + \frac{L_2}{\frac{1}{N^2}R_L}\frac{di_2}{dt} + \frac{V_s}{\frac{1}{N^2}R_L} = 0 \tag{2.29}$$

$$-L_1\frac{di_1}{dt} + L_2\frac{di_2}{dt} + V_s = 0 \tag{2.30}$$

Where we have $L_1 = KL_p$ and $L_2 = (1-K)L_p$ where K is the coupling factor and $L_p = 2.11mH$ is the primary winding inductance discussed previously. Using the Mathematica, parametric solutions for the differential equations are depicted in Figure

2.29. $L_1 = 0.9999526 \times 2.11^{-3} H$, $L_2 = (1 - 0.9999526) \times 2.11^{-3} H$, $N = 2.42$, $R_L = 70\Omega$ and $V_s = 5V$ are plugged in for the solution and the outputs in Figure 2.30 for the three currents are drawn.

```
In[81]:= pfun = DSolve[{I1[t] + I2[t] + (L2/(1/N^2 RL)) I2'[t] + Vs/(1/N^2 RL) == 0, 5 + L2 I2'[t] == L1 I1'[t], I1[0] == 0, I2[0] == 0}, {I1[t], I2[t]}, t]

Out[81]= {{I1[t] → (5 N^2 L2^2 - 5 e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L2^2 + 5 t L1 RL + 5 t L2 RL - N^2 L1 L2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1 L2 Vs - N^2 L2^2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L2^2 Vs)/(L1 + L2)^2 RL,
  I2[t] → (5 N^2 L1 L2 - 5 e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1 L2 - 5 t L1 RL - 5 t L2 RL - N^2 L1^2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1^2 Vs - N^2 L1 L2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1 L2 Vs)/(L1 + L2)^2 RL}}

In[86]:= Evaluate[pfun[L1, L2, N, RL, Vs][t], {{L1, 0.9999526×2.11×10^-3}, {L2, (1 - 0.9999526)×2.11×10^-3}, {N, 2.42}, {RL, 70}, {Vs, 5}}, {t}]

Out[86]= Sequence[{{I1[t] → (5 N^2 L2^2 - 5 e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L2^2 + 5 t L1 RL + 5 t L2 RL - N^2 L1 L2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1 L2 Vs - N^2 L2^2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L2^2 Vs)/(L1 + L2)^2 RL,
  I2[t] → (5 N^2 L1 L2 - 5 e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1 L2 - 5 t L1 RL - 5 t L2 RL - N^2 L1^2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1^2 Vs - N^2 L1 L2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1 L2 Vs)/(L1 + L2)^2 RL}}[L1, L2, N, RL, Vs][t],
 {{L1, 0.0021099}, {L2, 1.00014×10^-7}, {N, 2.42}, {RL, 70}, {Vs, 5}}, {t}]

In[89]:= Sequence[
 {{I1[t] → (5 N^2 L2^2 - 5 e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L2^2 + 5 t L1 RL + 5 t L2 RL - N^2 L1 L2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1 L2 Vs - N^2 L2^2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L2^2 Vs)/(L1 + L2)^2 RL,
  I2[t] → (5 N^2 L1 L2 - 5 e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1 L2 - 5 t L1 RL - 5 t L2 RL - N^2 L1^2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1^2 Vs - N^2 L1 L2 Vs + e^(t (-L1-L2) RL/(N^2 L1 L2)) N^2 L1 L2 Vs)/(L1 + L2)^2 RL}}[L1, L2, N, RL, Vs][t],
 {{L1, 0.0021098999859999997`}, {L2, 1.0001400000006489`*^-7}, {N, 2.42`}, {RL, 70}, {Vs, 5}}, {t}]
I3[t] = -(I1[t] + I2[t])
```

Figure 2.29. Mathematica solutiosn for differential equations governing the transmitter

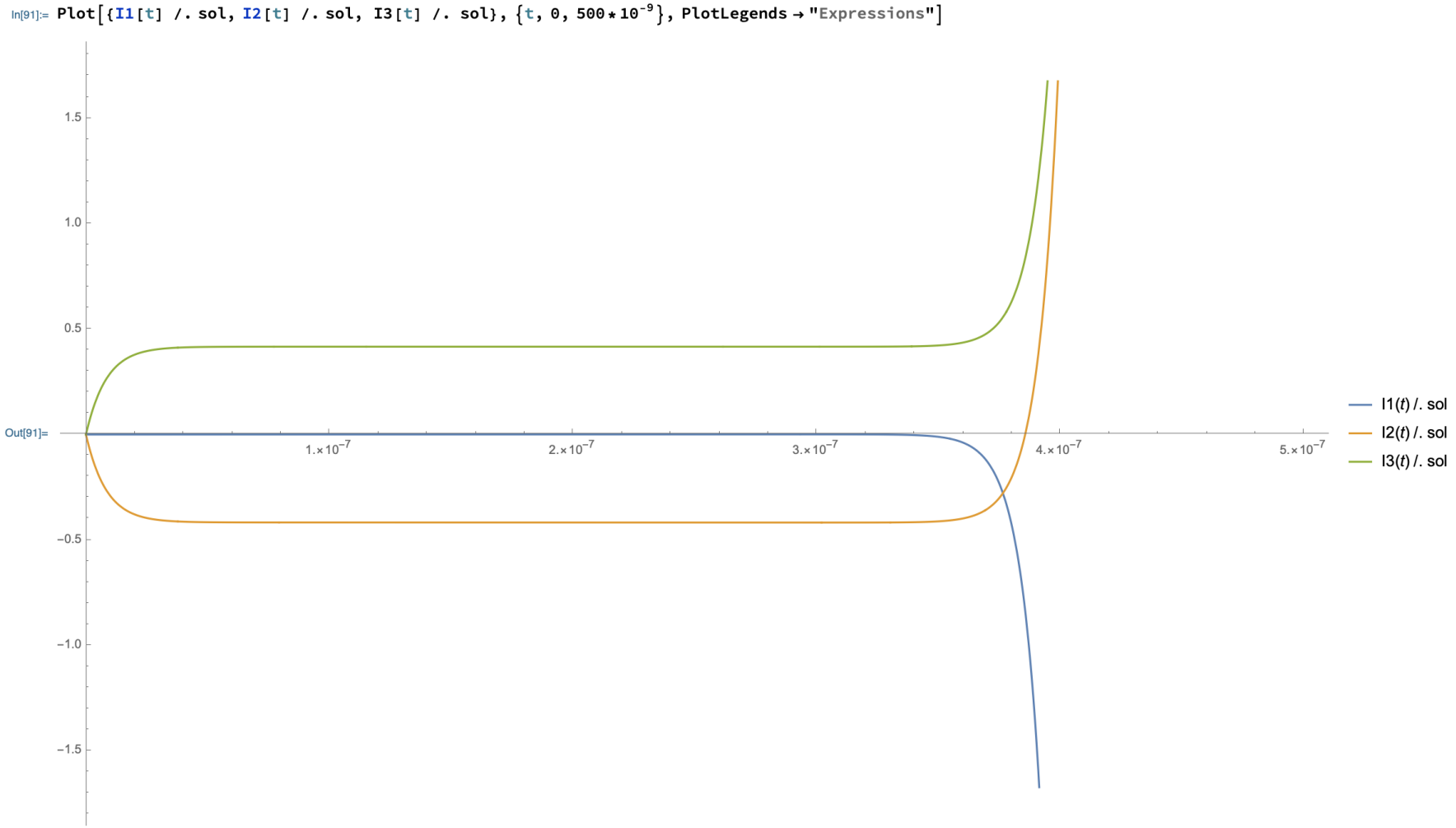


Figure 2.30. Mathematica solutions for differential equations, numerical values for currents

$I3$ in Figure 2.30 is essentially the current flowing through the resistive load which is about 415 mA when it settles and it agrees with the simulation and experimental results too. As we can see, keeping the switch ON for more than about 380 ns shorts the circuit theoretically but we also should keep in mind that we have used an ideal switch. A more accurate model would be to use the large signal model of the transistor with ideal current source (for both saturation and linear regions at specific times), but without further complicating the analysis, we have what we need which is a rough estimate for the rise time. Rise time here shows to be around 40 ns. We expect it to be between 100 ns and 200 ns as it will be evident in the simulations and experiment part. But then again, the reason for this is the fact that we used ideal switches. From the parametric results in Equation 2.29 we conclude a few important notes regarding the rise time. Apparently as the coupling factor K decreases in value from its initial 0.9999526 value, the rise time at the terminal increases and at some low values of K, peak to peak current (also voltage) decreases too. This goes to say that the transformers designed for MIL-STD-1553 need to have a high coupling factor. A decrease in the inductance of the transformer winding reflects a decrease in the rise time of the terminal voltage understandably, however, by decreasing the winding inductance we essentially have to further improve the coupling factor, otherwise rise time significantly increases. Finally, last but not the least, the turns ratio increase causes a slight increase in the rise time but it also significantly increases the peak to peak terminal current as well as voltage. Figures 2.31 and 2.32 show the spoken effects graphically. Data collected from the solutions of Figure 2.29 by sweeping one variable, and keeping the rest constant.

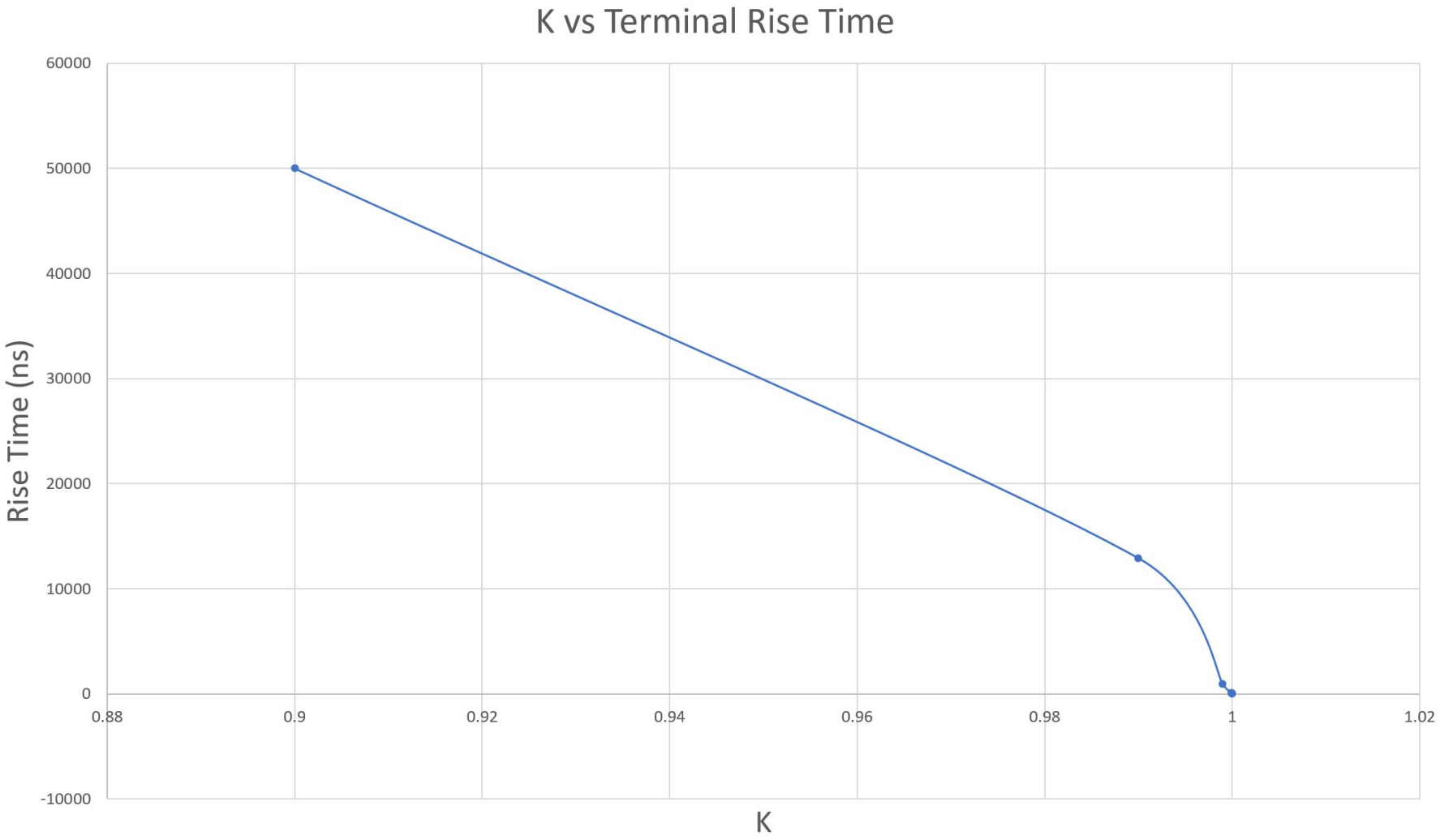


Figure 2.31. K vs Terminal rise time

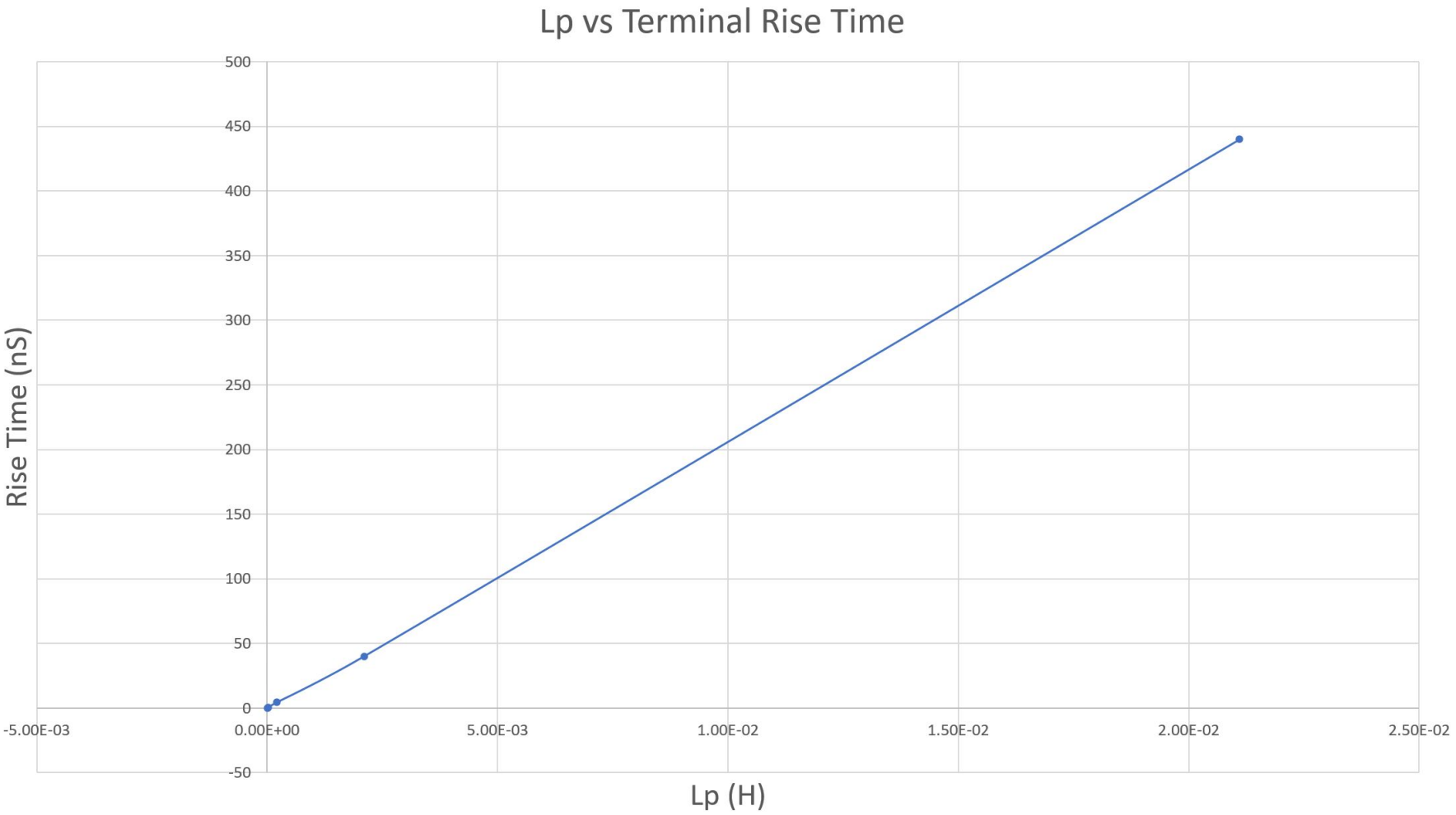


Figure 2.32. Lp vs terminal rise time

2.4.1. Transmitter circuit design for PCB with discrete elements

The circuit designed for PCB involves the switch configuration shown in Figure 2.22 and a gate driver chip. Switch NMOS transistors are a pair of Si733ADP [16] power MOSFETS with 30V V_{ds} rating with a threshold voltage of 2.9V. Gate driver chip used is FAN322TMX [17]. Two 3Ω resistors are added to the driving side to limit the current (They were originally put for experimental purpose, however they introduce small oscillations as a side effect). Figure 2.33 shows the current (version 1) PCB boards transmitter circuit.

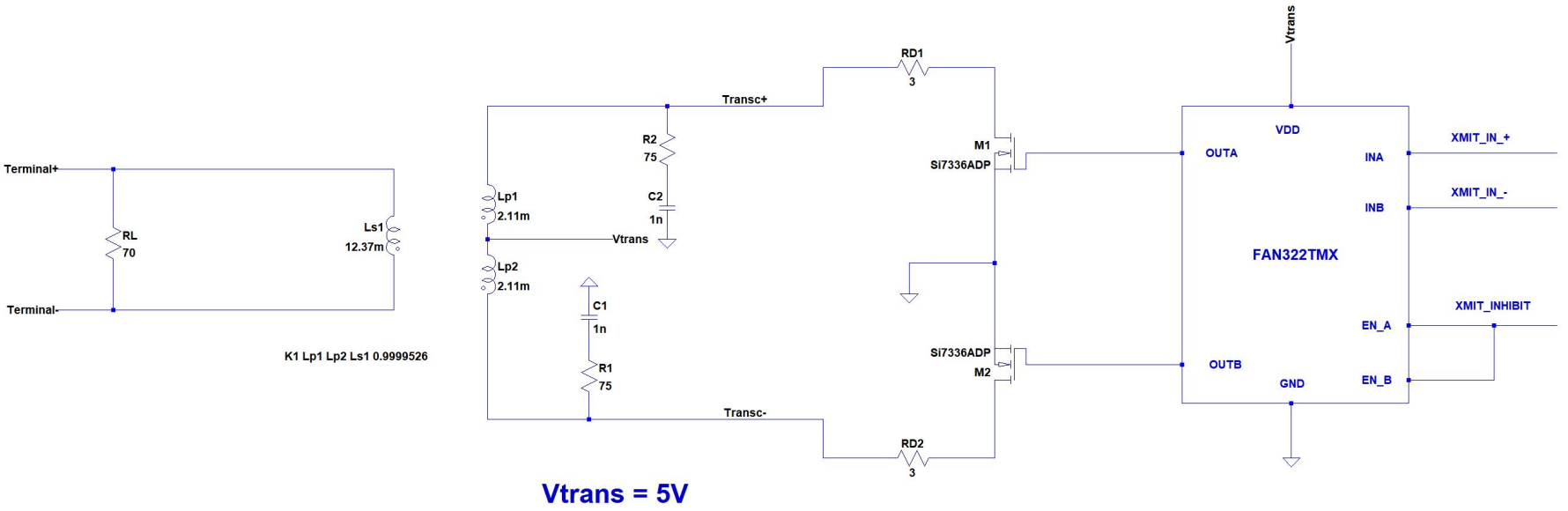


Figure 2.33. Transmitter circuit, PCB, in LTSpice

In Figure 2.33, R_1, R_2, C_1, and C_2 are responsible for reducing the overshoots in the transmitter side. The larger the capacitance values, the more suppression on the possible overshoots. FAN322TMX integrated circuit drives the gates of power mosfets. It is present on the PCB schematics and board, however not in the SPICE simulation. We therefore simulated with ideal large rise and fall times at the transmission to get as close as we could to the real situation.

2.4.2. Transmitter circuit design for IC with UMC130 technology in Cadence

The transmitter circuit in IC needs quite a few considerations. UMC130nm technology library is equipped with 1.2 V and 3.3 V transistors. More on this will be discussed in the experiment and results section when layout is presented too but for now it suffices to state that driving switches must be able to endure 380 mA current with large gate capacitance for slope control. The switches given in Figure 2.34 consist of 228 parallel connected, 100 μm in width and 10μm in gate length 3.3 V transistors. This is done to reduce the drain current per transistor to below 2mA ($\frac{380mA}{228} = 1.67mA$).

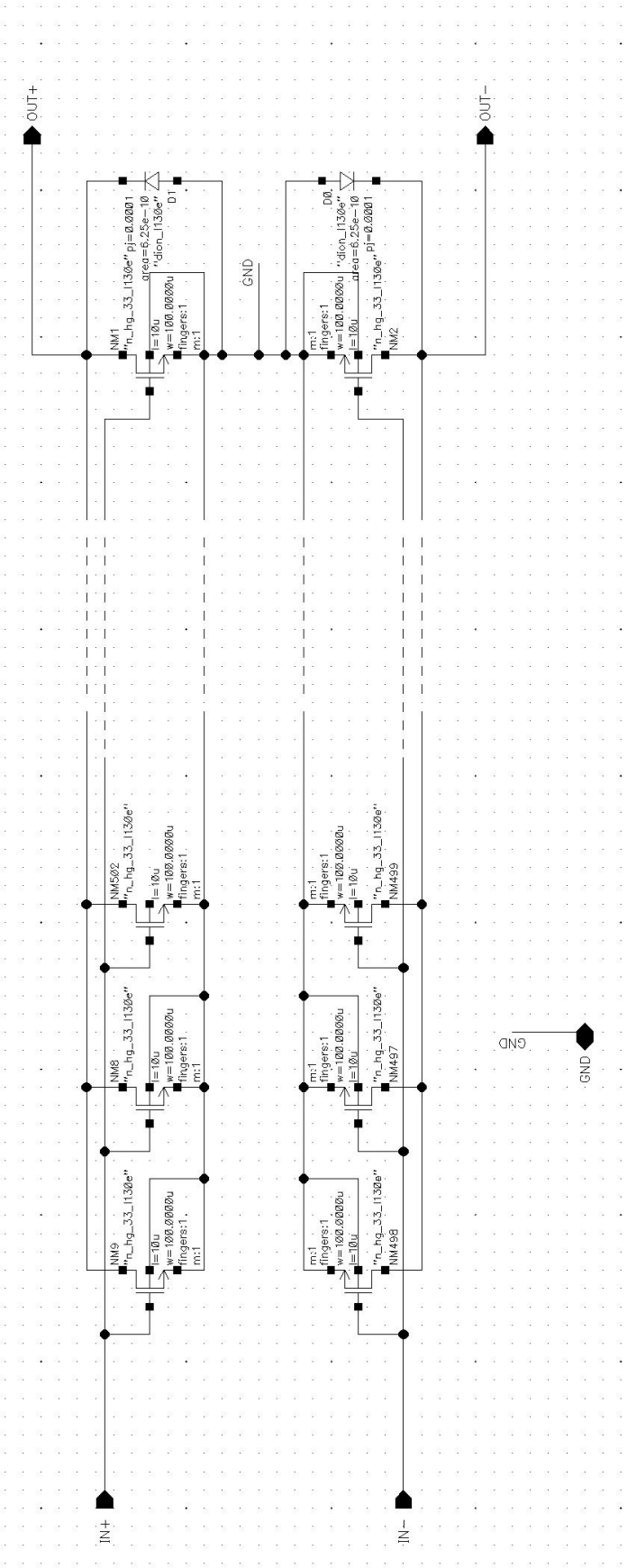


Figure 2.34. Transformer Line Driver MOS circuitry, UMC130nm Cadence

Large gate length for each transistor is set for two main reasons. First off, as we saw in Figures 2.23 and 2.24 while one transistor is conducting through the winding and their drain, drain to source voltage drops to $V_{DS,ON} \approx 500mV$. At the same time, the drain to source voltage of the non-conducting NMOS switch is around $V_{DS,OFF} = 2 \times V_{DD}$. In fact simulation results show $V_{DS,OFF} \approx 9.6V$. This voltage on drain and source could cause problem for the 3.3 V transistor chosen when fabricated. Therefore, 30 times the minimum gate length ($\approx 10\mu m$) has been chosen to prevent any potential problems that could arise in the fabricated IC. The proper way of calculating how large this gate length should have been would be to have gone through process specific documentation and estimate the capacitance of the POLY layer per transistor and their interconnection. For now, this 10μm gate length is chosen experimentally (recall too large of a capacitance would mean larger slope and ill-formed transmitted signal, or otherwise large power consumption at each gate charging cycle). Figure 2.35 shows the current through the 3.3V transistor we used in IC when the gate source voltage is zero (transistor OFF) and drain to source voltage is 10V.

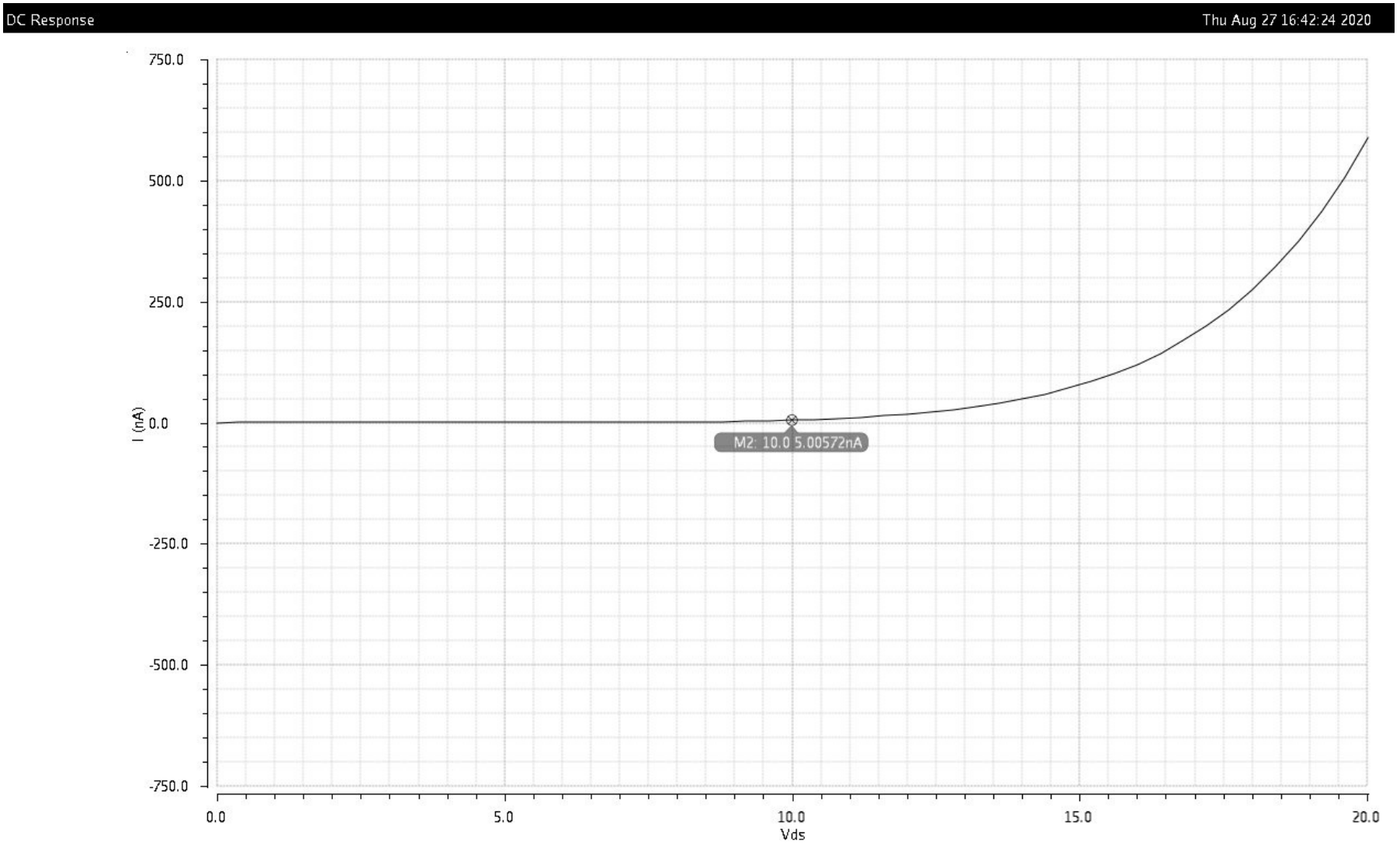


Figure 2.35. I_D vs V_{DS} when V_{GS}=0V, of NMOS transistor used in UMC130nm process. W=2μm, L=360nm

When $V_{GS} = 100mV, I_D \approx 77nA$ which is still a small current. Although it is not entirely feasible to assume just by looking at Figure 2.35 that when one of the NMOS switches is off, the 9.6V over drain to source would not break down through drain to source since we need specific process documentation to comment on that, it would be reasonable to assume little to no current is a good indication that the spoken problem may not occur. This conclusion is enforced in the I_D vs V_{DS} curve in Figure 2.36 when we change the width and length values to match that of what we use in driver circuit in Figure 2.34.

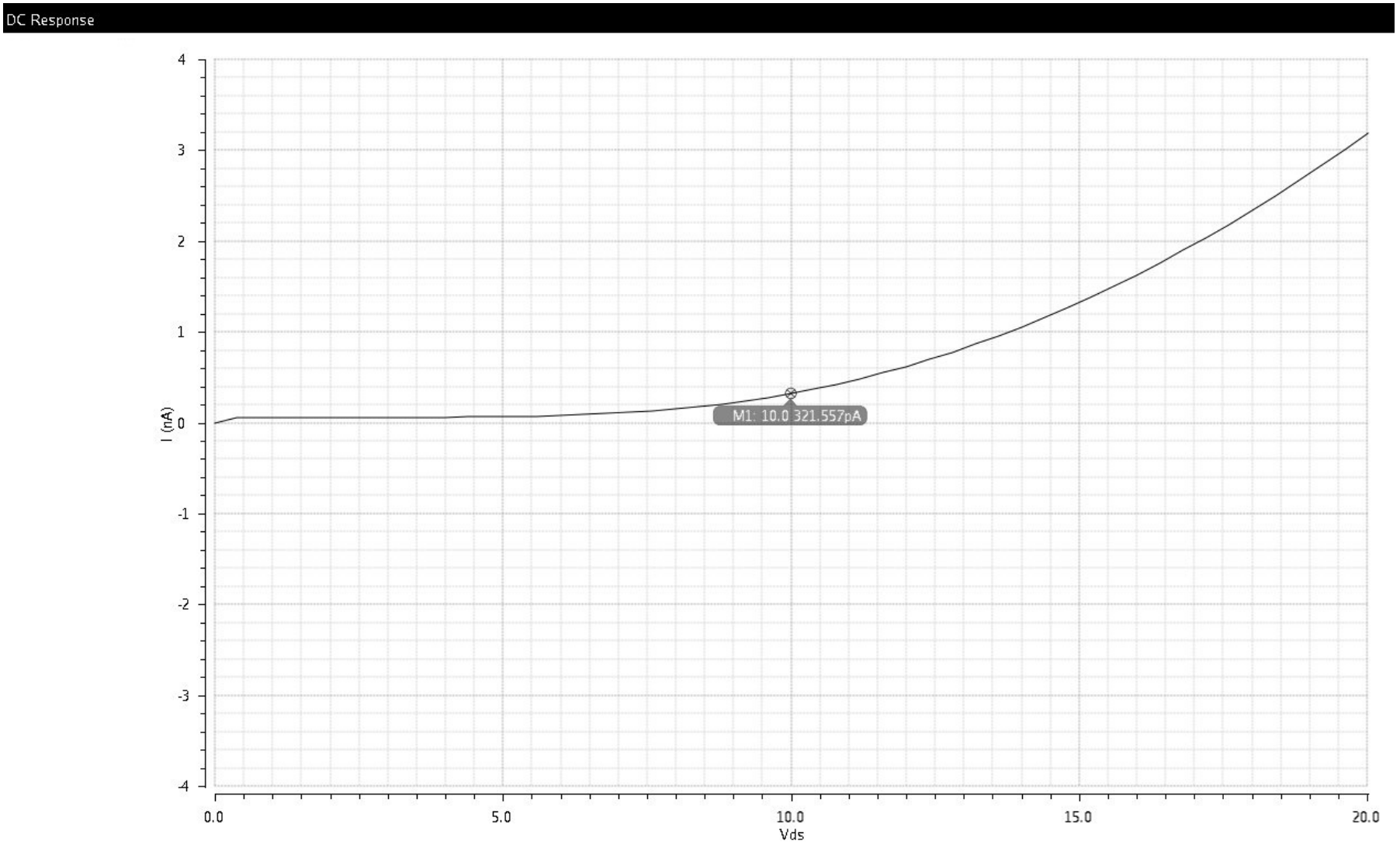


Figure 2.36. I_D vs V_{DS} when V_{GS}=0V, of NMOS transistor used in UMC130nm process. W=100μm, L=10μm

Figure 2.37 shows the setup simulation to obtain the curve in Figure 2.36 presented for the sake of completeness.

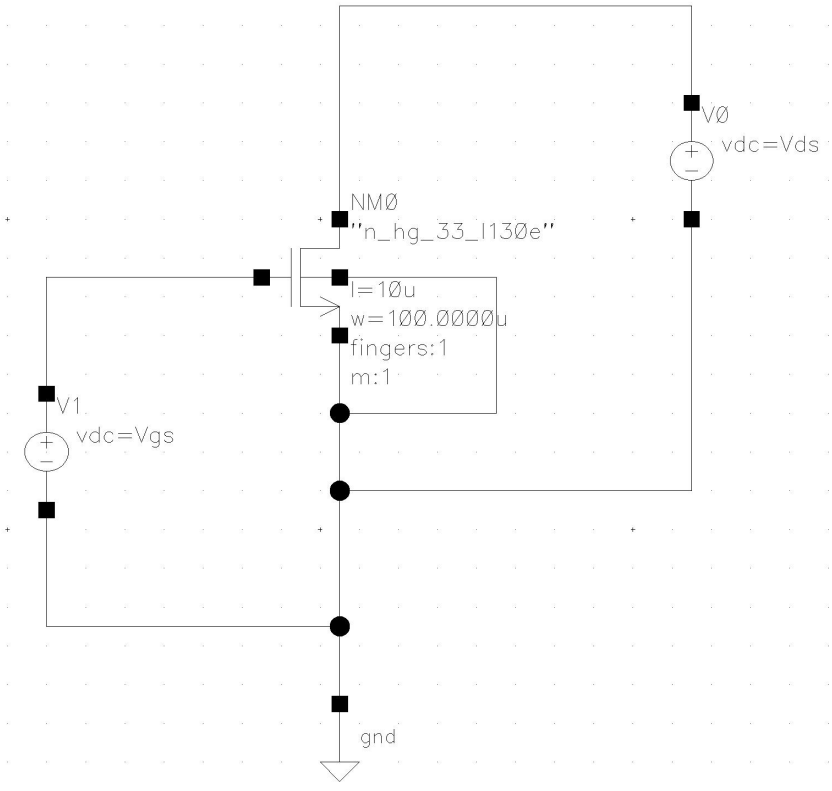


Figure 2.37. I_D vs V_{DS} when V_{GS}=0V, circuit setup of NMOS transistor used in UMC130nm process. W=100μm, L=10μm

As we can see from Figure 2.36 the current is around 320 pA confirming our assumption that by increasing the gate length, we further drop this current. However larger gate length, as pointed out before, introduces absurd power consumption issues..

The transmitter is required to have a transmission inhibit signal where transmission is enabled through that control signal. A simple NAND gate is in Figure 2.38 is presented to serve that purpose.

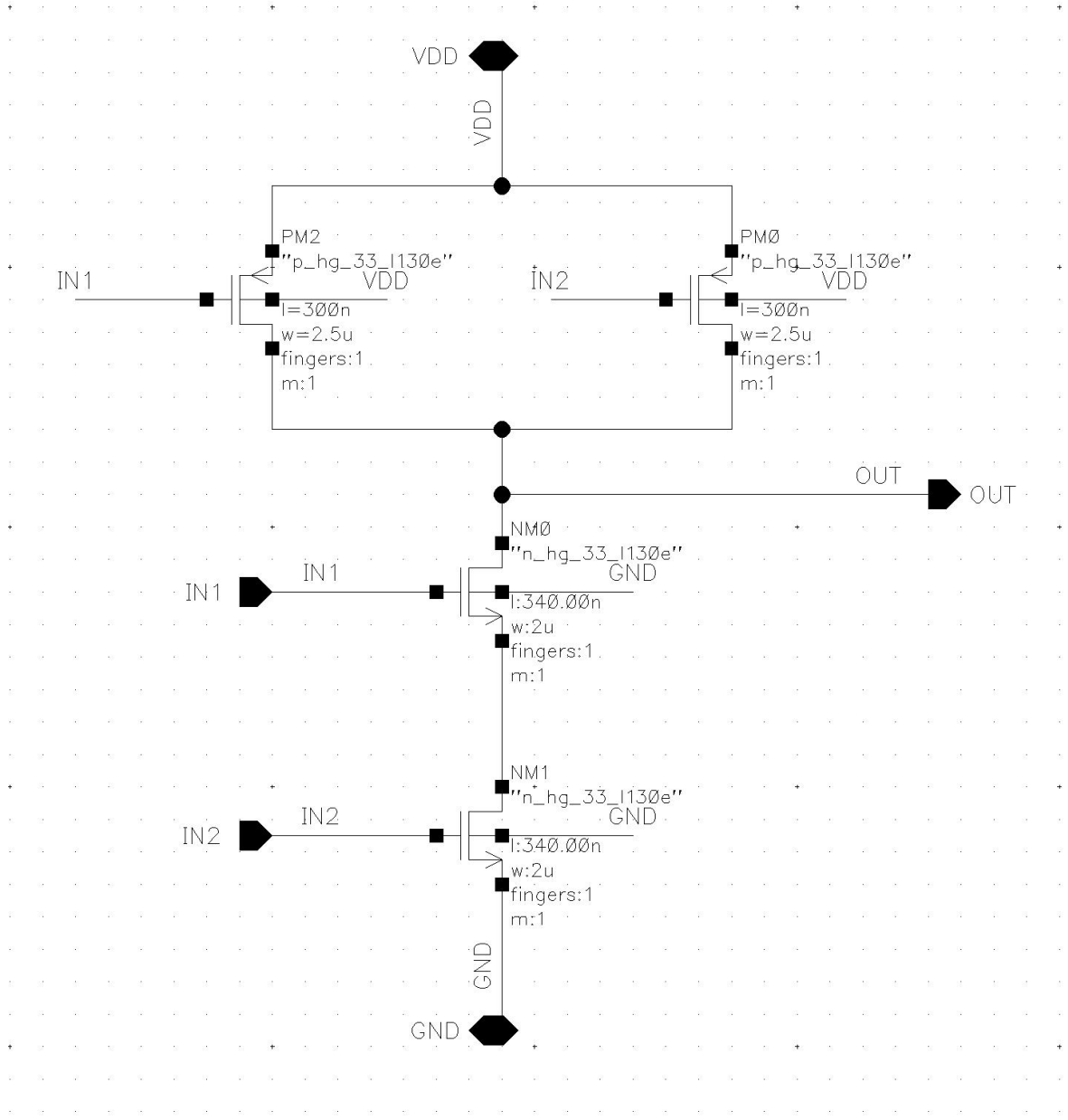


Figure 2.38. Transmission INHIBIT NAND gate, UMC130nm, Cadence

Equations from 2.31 to 2.34 show simple calculations for sizing to match rise and fall times of the output NAND gate.

$$I_{DP} = I_{DN} \tag{2.31}$$

$$K_p \frac{W_p}{L_{min}} = 2.5 K_p \frac{W_n}{L_{min}} \times \frac{1}{2} \tag{2.32}$$

$$W_n = 2\mu m \tag{2.33}$$

$$W_p = 2.5\mu m \tag{2.34}$$

Finally, maybe one of the most important components of the transmitter circuit, is the circuitry for generation of the non-overlapping signal from the overlapping TTL input for the transmission [18]. As depicted in Figure 2.25, the gate to the driving NMOS switches are ought to be driven in a non-overlapping fashion for the reasons mentioned (mainly overshoot prevention). Figure 2.39 is the schematic of such a predriver required to drive the switch gates in a non-overlapping way. BUFF and INV circuits are buffer and inverter circuits respectively whose schematics are presented in Figures 2.40 and 2.41. The delay of the proposed buffer are nearly independent of power supply voltage [19]. INV circuit acts a gate driving component for the switches. To design gate drive circuits, the study of the device (MOSFET) circuit models and the turn-on and turn-off characteristics of the MOSFET are required [20] [21].

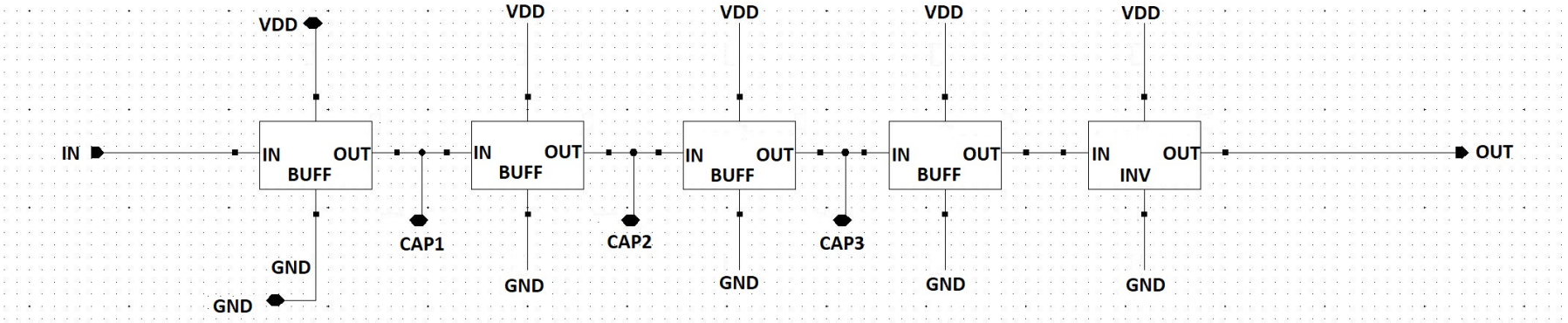


Figure 2.39. PREDRIVER schematic (non-overlapping generator), UMC130nm, Cadence

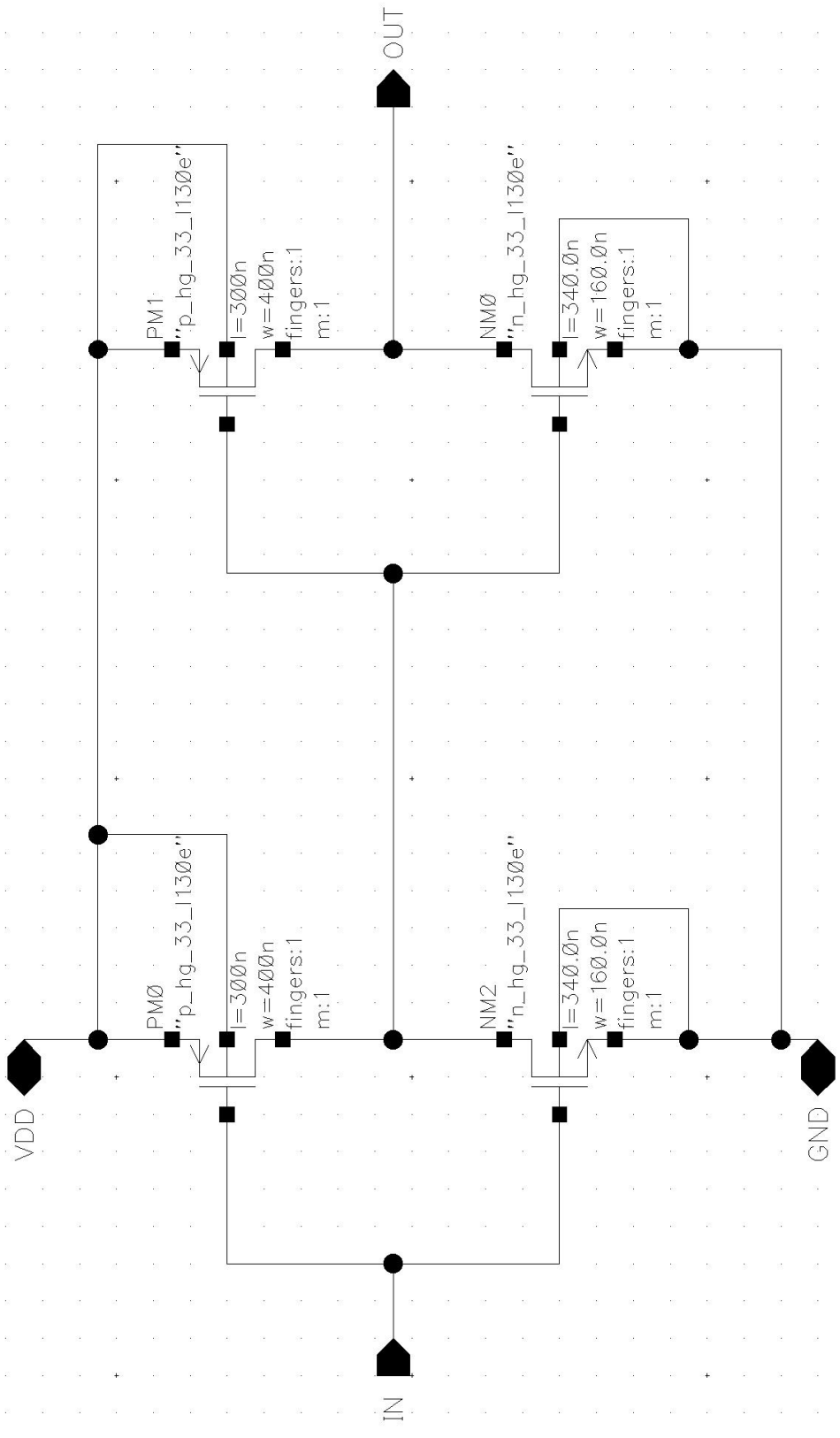


Figure 2.40. Buffer circuit, UMC130nm, Cadence

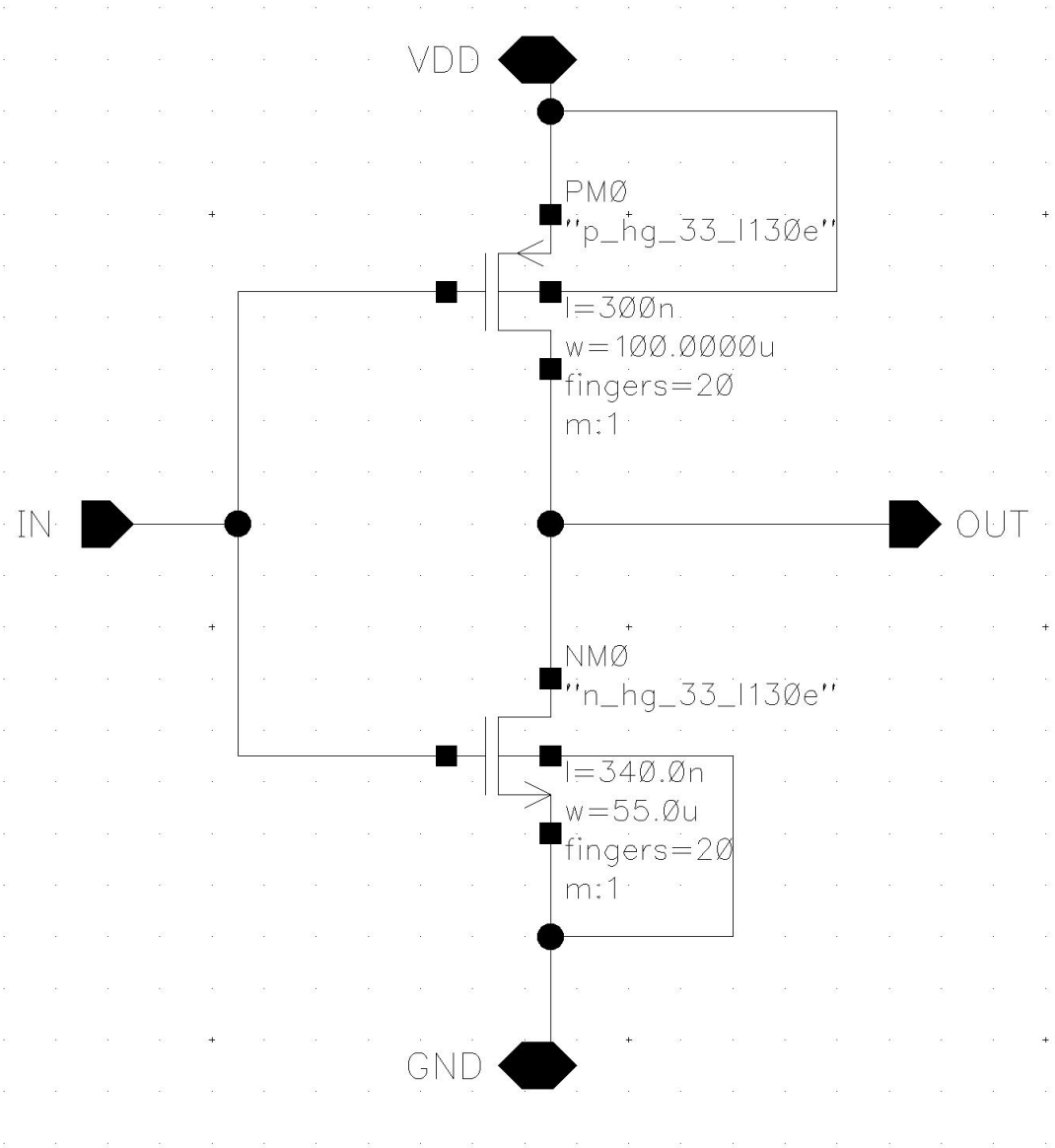


Figure 2.41. Inverter circuit, UMC130nm, Cadence (this component is important in a sense that the driving of large gate capacitance of the transformer driving switches is solely on them)

INV component will be driving the large gate capacitance of the transformer driving switches; therefore, it has to be large. BUFF and NAND gate sizing is kept to the minimum for power consumption reduction.

The capacitor pins in Figure 2.39 (CAP1, CAP2 and CAP3) are responsible for delay control. If the capacitances are too small, the non-overlapping effect disappears. If they are too large, the transmission signal disfigures. This capacitor value must not exceed values of 50pF. We found experimentally in post layout simulations that 2-7 pF generates best results. Analytical calculation of this requires the knowledge of approximate gate POLY capacitance and transient solution to the current flowing through each winding of the transformer.

Figure 2.42 shows the complete transmitter block to be used in the IC.

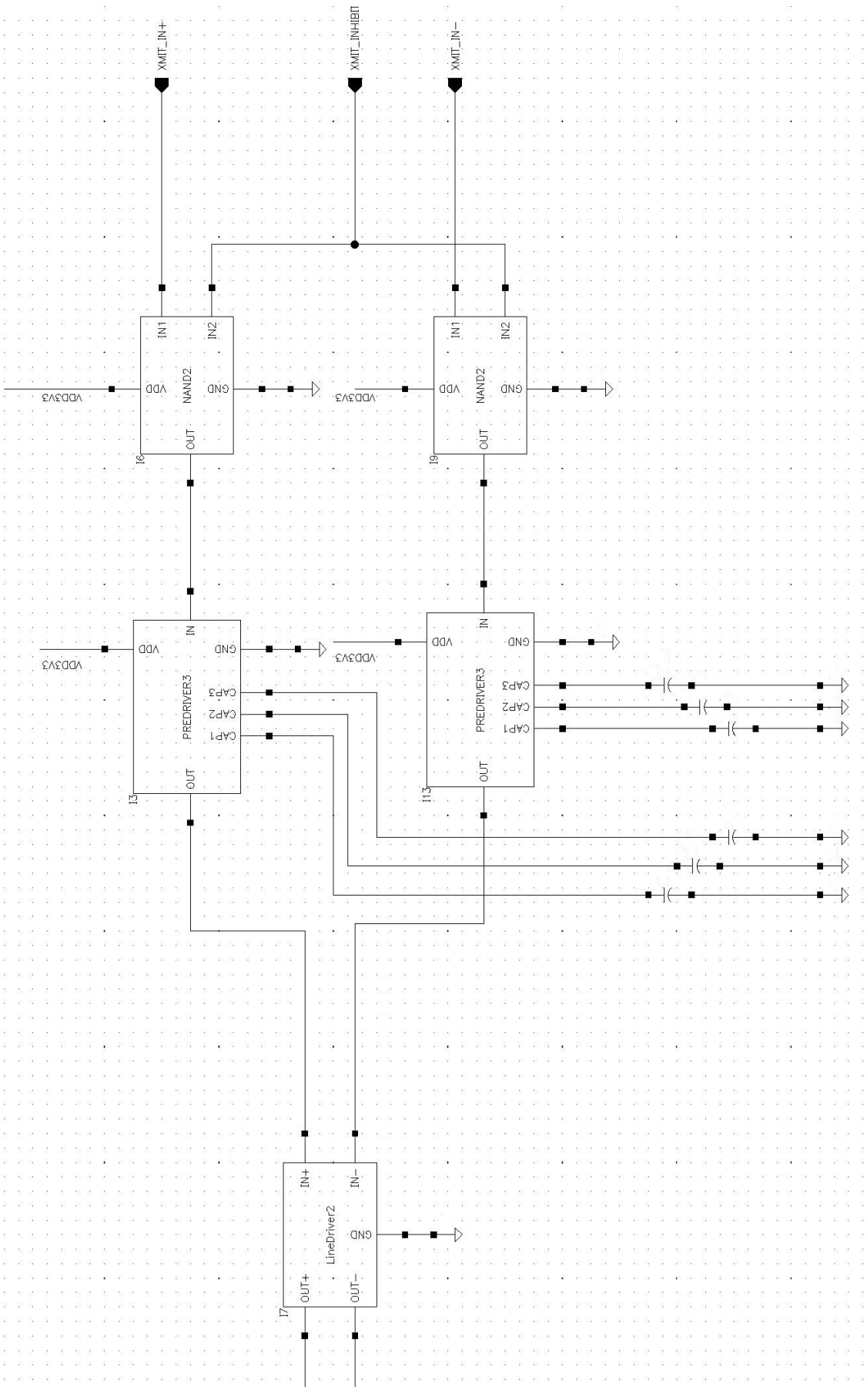


Figure 2.42. Transmitter circuit schematic, UMC130nm, Cadence

3. SIMULATION, EXPERIMENTS, AND RESULTS

3.1. Simulation Results

In this section, simulation schematics and test setup with results for PCB (SPICE) and IC (Cadence schematics, UMC130nm) will be presented. And then the actual experimental results will be compared.

3.1.1. PCB, SPICE schematic simulations

LTSpice is used to simulate the PCB part of the project. In this part the spice parameters of one component, namely the TTL input driver FAN3227TMX, were not available. Therefore, it is not present in the SPICE simulation but however we account for its absence by adjusting the ideal input sources.

Figure 3.1 shows the entire transceiver is a single schematic. Figure 3.2 shows the transient results for transmission testing. As discussed before, the resistor network for the receiver part of the project has been recalculated for the experimental threshold levels on the actual PCB using Equations 2.9, 2.10 and 2.11.

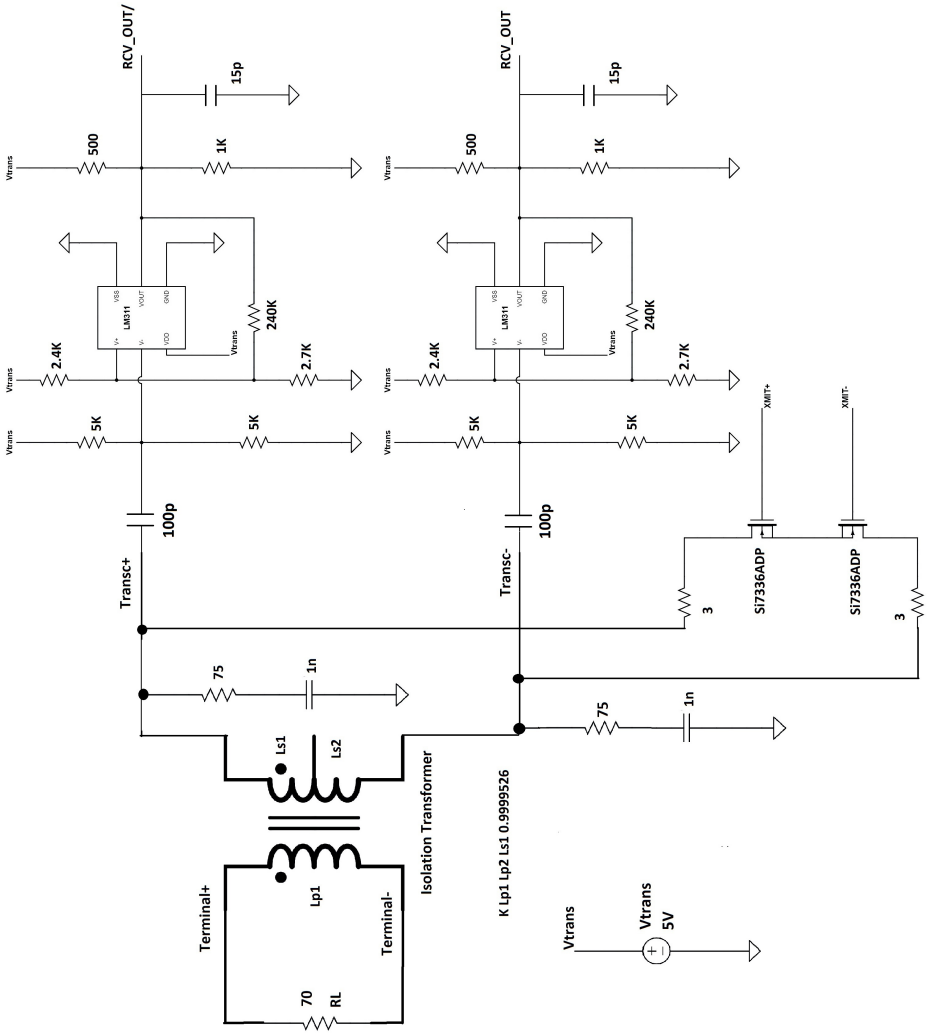


Figure 3.1. Transceiver circuit schematic LTSpice, PCB

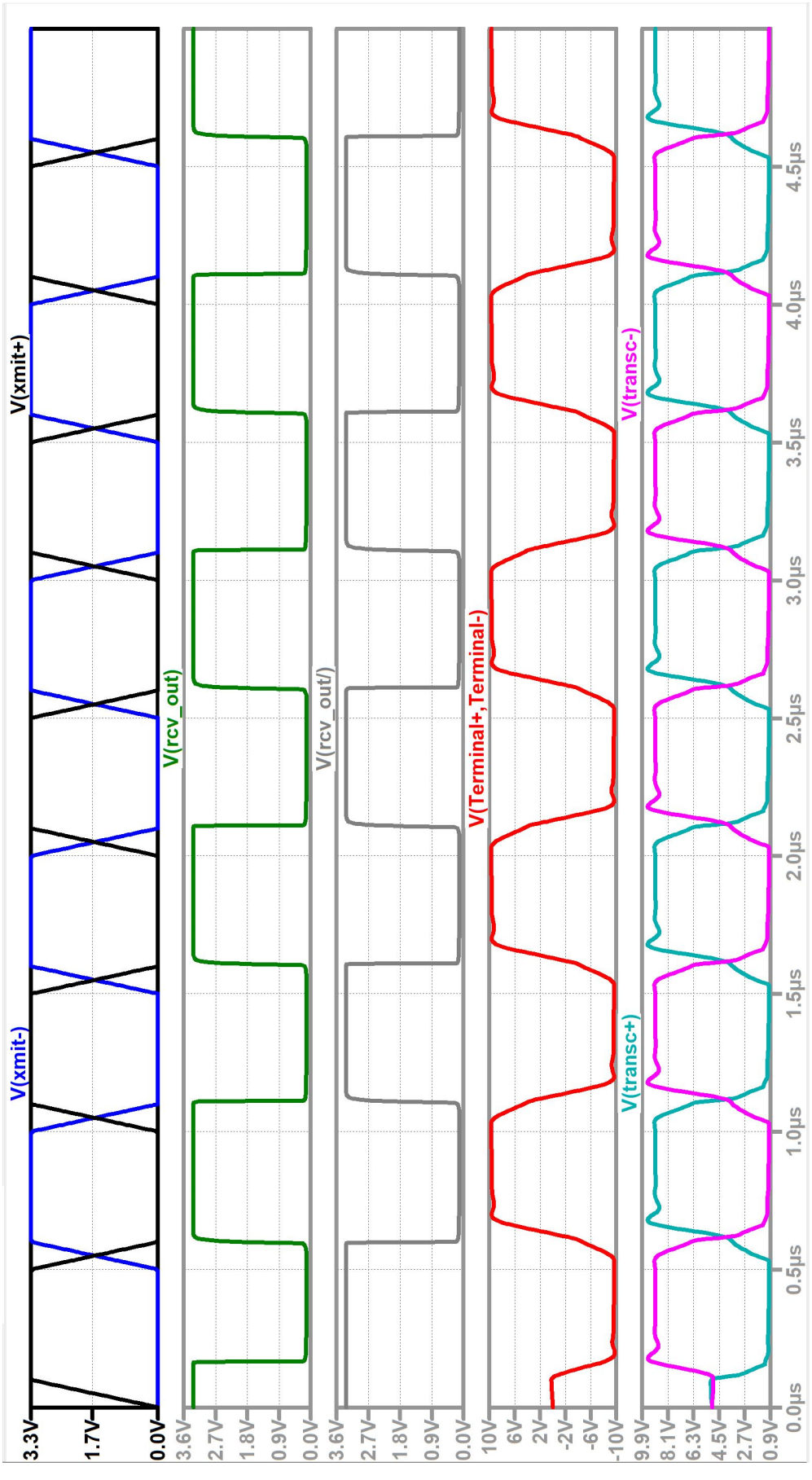


Figure 3.2. Transceiver circuit results (Voltages Transmitting), LTSpice, PCB

The transmitted signal is received at the receiver in a parallel fashion as seen in Figure 3.2 (RCV_OUT and RCV_OUT/) as expected. Zero crossing delay in this case is minimal since the voltages arriving at the negative input of the comparators are relatively large. Peak to peak transmission voltage is around 19.2 V. This is due to the 1V drop over the 3Ω Resistor placed at the transmission side. Transmission rise time is 169ns and fall time is 165ns. Figure 3.3 shows the waveforms of the comparator and received signal while transmitting.

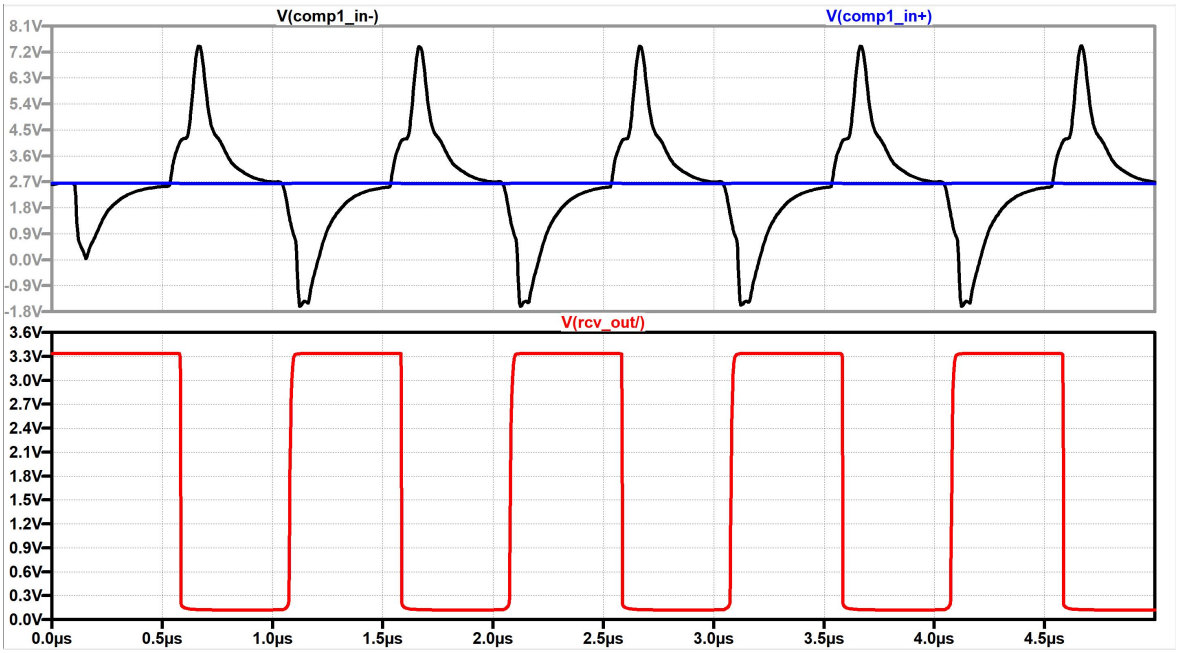


Figure 3.3. Transceiver circuit results (Looped backed voltages while transmitting), LTSpice, PCB

COMP1_IN+ signal is the reference signal to the comparator which is fixed at 2.5V. The received signal here is due to the parallel connection of the receiver part of the circuit to the transmitter part of the circuit.

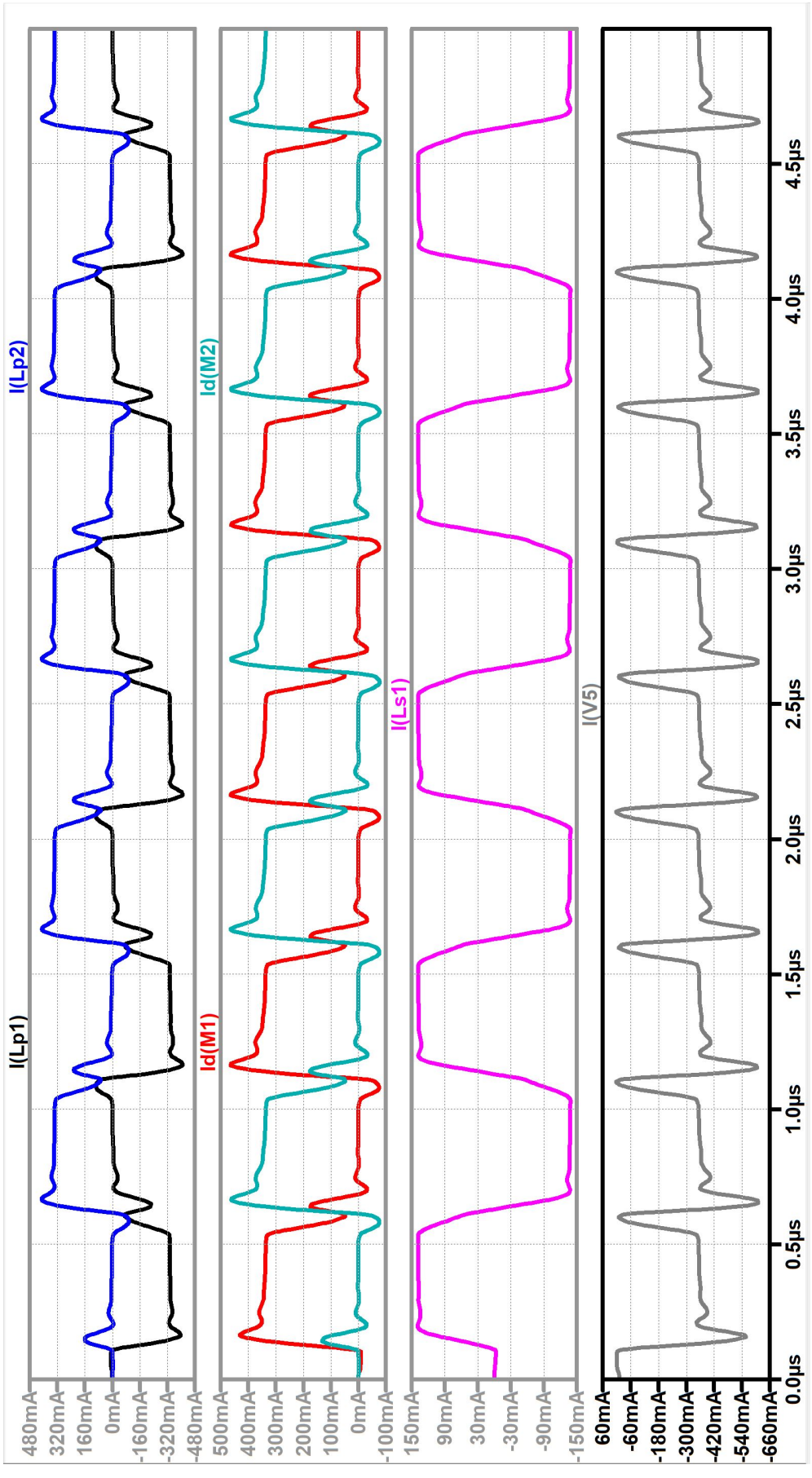


Figure 3.4. Transceiver circuit results (Transmission currents), LTSpice, PCB

Figure 3.4 shows the currents through the components while transmitting. The wobbling currents in Figure 3.4 as well as overshoots in pins Transc+ and Transc- seen in Figure 3.2 are due to the overlapping nature of the input transmission signals. The overshoot in transmitted signal is around 65mV. I(V5) in Figure 3.4 is the current through the 5V supply voltage. The rms current through the source is around 362 mA. The current consumption for the receiver in operation (although the waveforms are not present) is around 15 mA.

To test the receiver, we apply the input to the terminals and disable the transmission signals. Figure 3.5 shows a typical receiver in action with adequate voltage levels on the terminal. The zero crossing delay measured here in this typical configuration where terminal voltage is around 5 Vp-p, is around 38ns. The maximum zero crossing delay occurs when the minimal terminal voltage is present on the terminal. That is what we have designed it to be 0.86 Vp-p as required by 1553 standards. By inducing 0.86 Vp-p on the terminal we can observe this effect in Figure 3.6. We measure this maximum zero crossing delay to be around 286ns which is within the acceptable range of 1553 standards. We can also observe the reference voltages of the comparators switching between the determined values we calculated before.

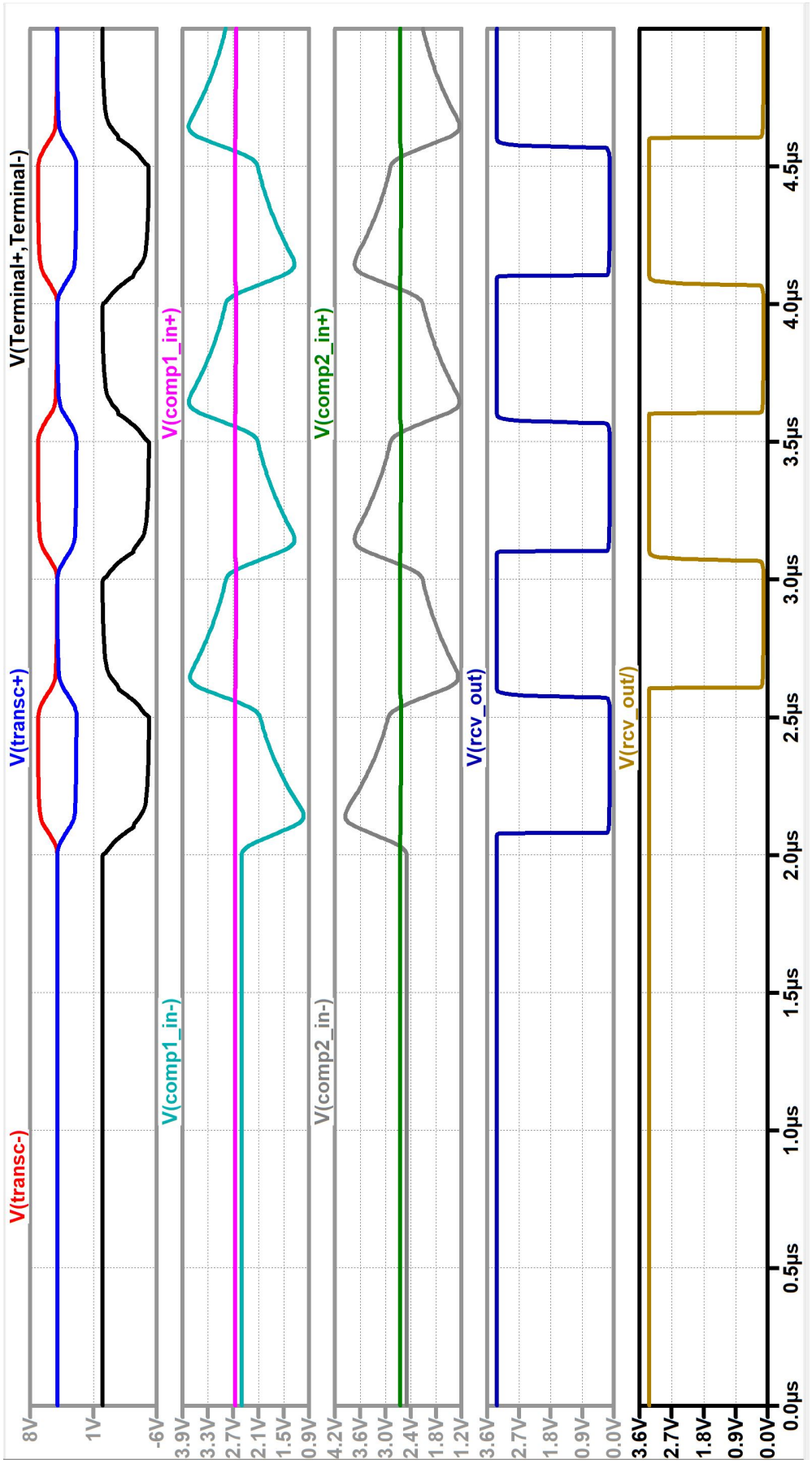


Figure 3.5. Transceiver circuit results (Receiver voltages), LTSpice, PCB

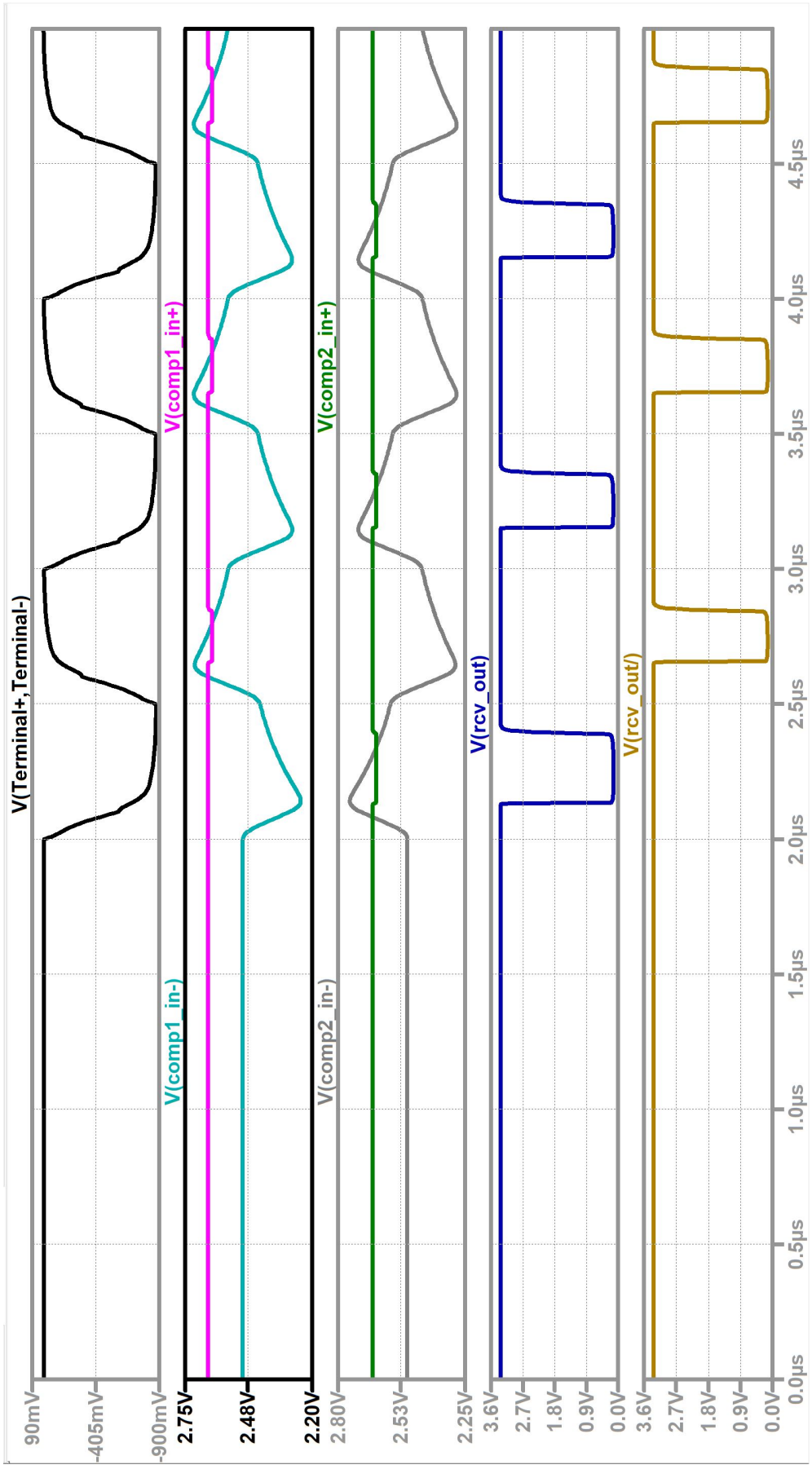


Figure 3.6. Transceiver circuit results (Receiver voltages, 0.86V threshold check and max zero crossing delay), LTSpice, PCB

3.1.2. IC, Cadence schematic UMC130nm simulation

In this section the schematic simulations for the IC part of the project will be presented. All simulations were performed in Cadence ADE. The whole transceiver schematic connections is shown in Figure 3.7 and its for demonstration purpose. The transceiver block under test is presented in Figure 3.8 and its test bench schematic is presented in Figure 3.9.

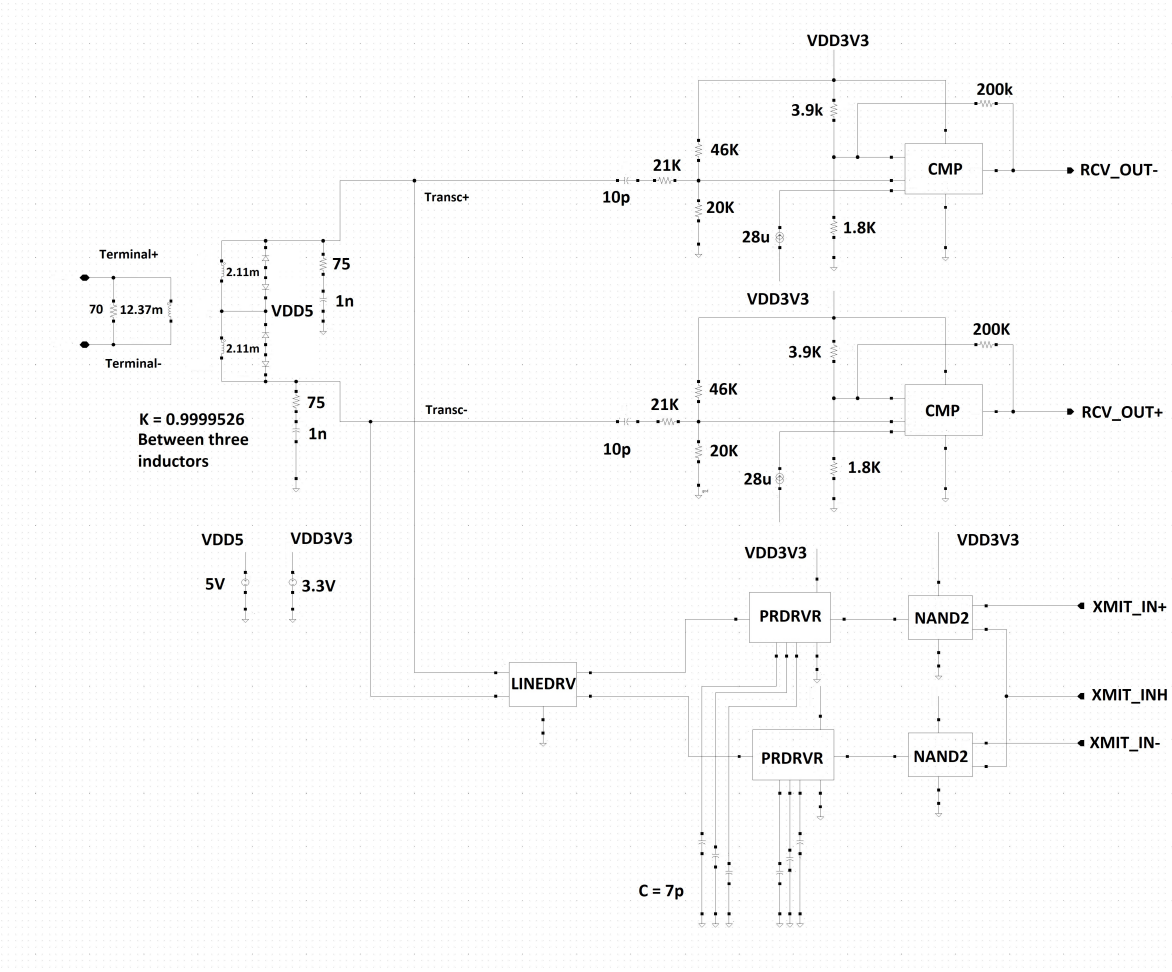


Figure 3.7. Transceiver schematic, Cadence UMC130nm, IC

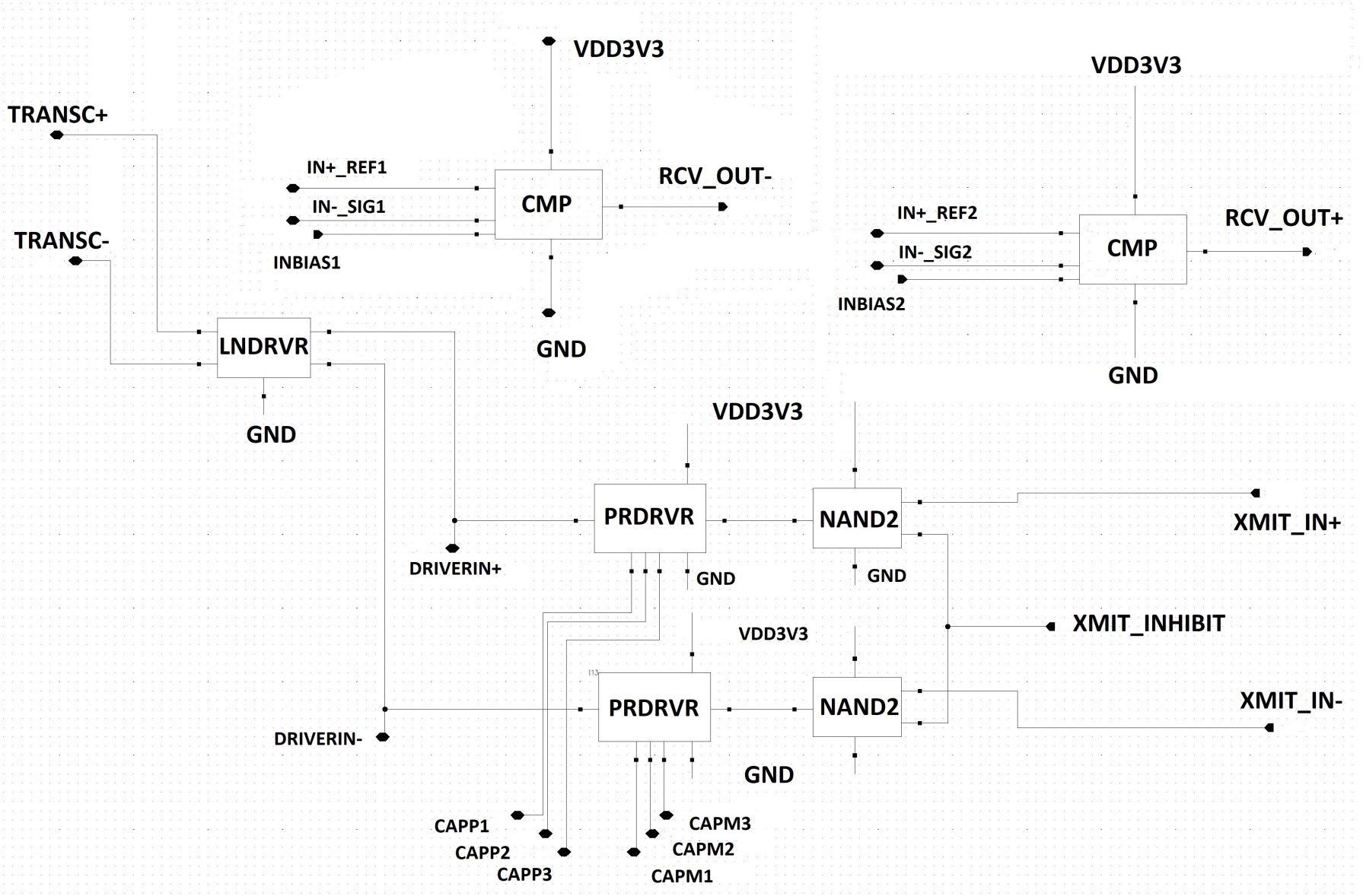


Figure 3.8. Transceiver schematic block, Cadence UMC130nm, IC

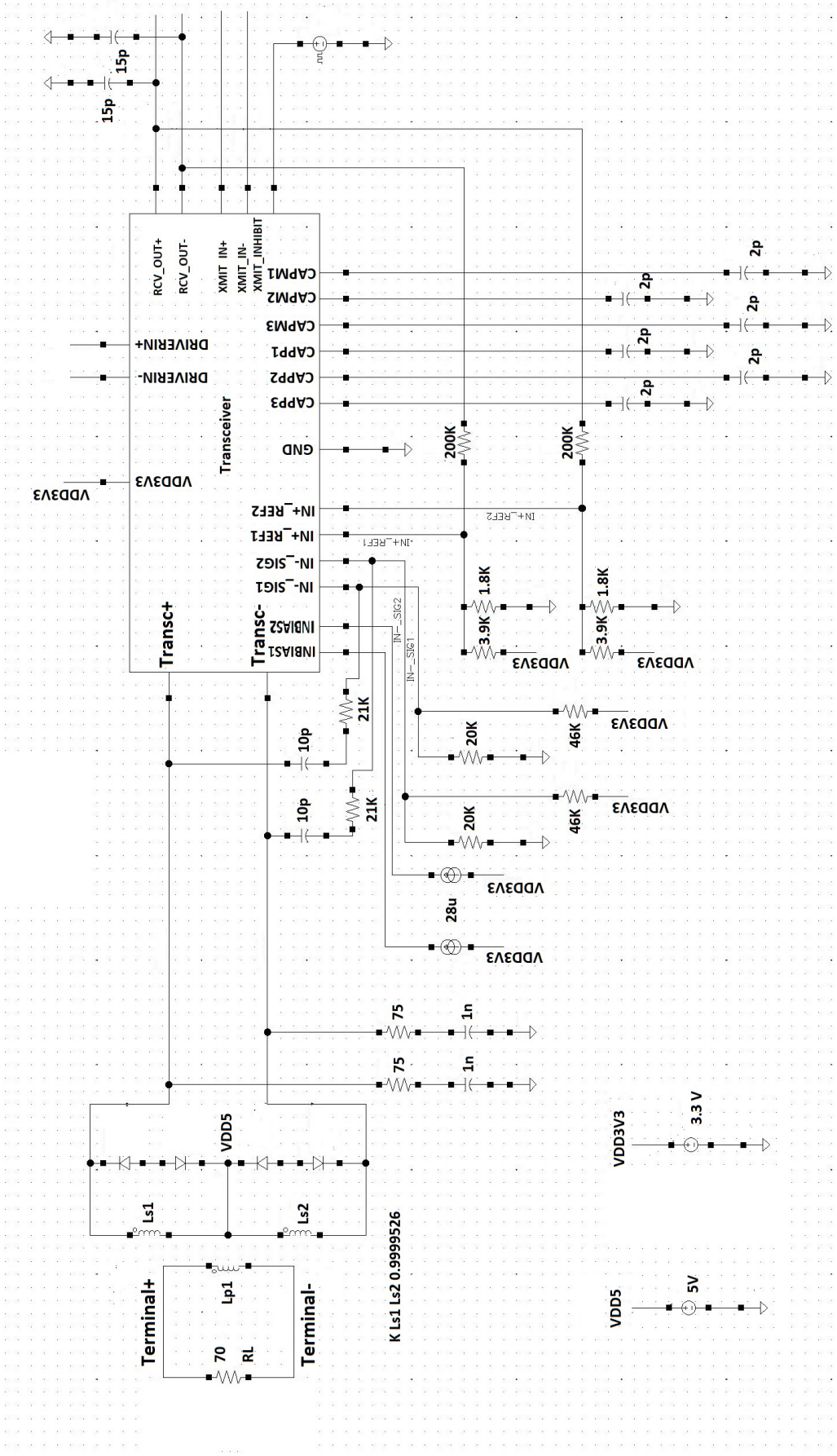


Figure 3.9. Transceiver circuit test bench schematic, Cadence UMC130nm, IC

The value of the delay capacitances are different for schematic and experimental (extracted layout) and shall not be confused on the schematic. Delay capacitors for predriver circuit in Figure 3.9 are 7pF for schematic simulation and 2pF for experimental (extracted layout) simulations. The reason for this is that parasitic capacitances are introduced in the extracted layout; therefore, the delay capacitances need to be reduced to compensate. Secondly, the input to the transmitter is setup ideally in the most undesirable configuration possible. Fast switching is assumed (10ns rise and fall times) and signals overlap. Reduction in slope and non-overlapping generation is what we are aiming PREDRIVER circuit to take care of in Figure 2.39.

Figures 3.10, 3.11, 3.12 and 3.13 are the schematic simulations of the transceiver. In Figure 3.10 the transmission is tested. Peak to peak transmission is measured to be around 21.8 Vp-p for 70Ω terminal load. Rise time 137ns and fall time for transmission 136ns. The rms current consumption through 3.3V voltage source is 9.2 mA and through 5V voltage source is 288 mA by taking the rms values of V0 and V1 in Figures 3.11 and 3.12.

What is important to note here is the the way we drive the gates of the switches in Figure 3.10. Although the DRIVERIN+ and DRIVERIN- signals seem to overlap at about third way of the full swing (1V), Without the PREDRIVER circuit block, this overlap occurs at halfway. This would cause overshoots depicted in Figure 3.14, where we have removed the delay capacitances in Figure 3.9 and effectively the non overlapping generation process. Also note that the lack of complete non overlapping (0V as opposed to third the voltage swing) is compensated by the slope control of the circuit via large capcitances in the gate of the driving switches. Recall we touched on this subject in the theory and design section by stating that the overshoots at the edges of the primary transformer winding is heavily dependent on the slope at which the switching gates are driven plus the nature of non overlapping voltages at the gate. Since we already have slope control, there leaves no need for PREDRIVER to separate inputs farther than it is needed. Figure 3.15 on the other hand shows what happens when we increase the value of the capacitances to 15pF for large non-overlapping effect

and how ill-formed transmission signals are formed. Furthermore, when overshoots are present in the absense of the PREDRIVER circuit, while transmitting, signals IN-_SIG1 and IN-_SIG2 which are connected to the differential pair at the receiving comparator rise to values above 4V as shown in Figure 3.14 and would damage the differential NMOS transistors.

Figure 3.12 shows the receiver at its maximum zero crossing delay when the terminal voltage is at 0.86 Vp-p which is around 282 ns. Figure 3.13 is where the terminal voltage is at its maximum 14 Vp-p and zero crossing delay at the receiver is around 10 ns.

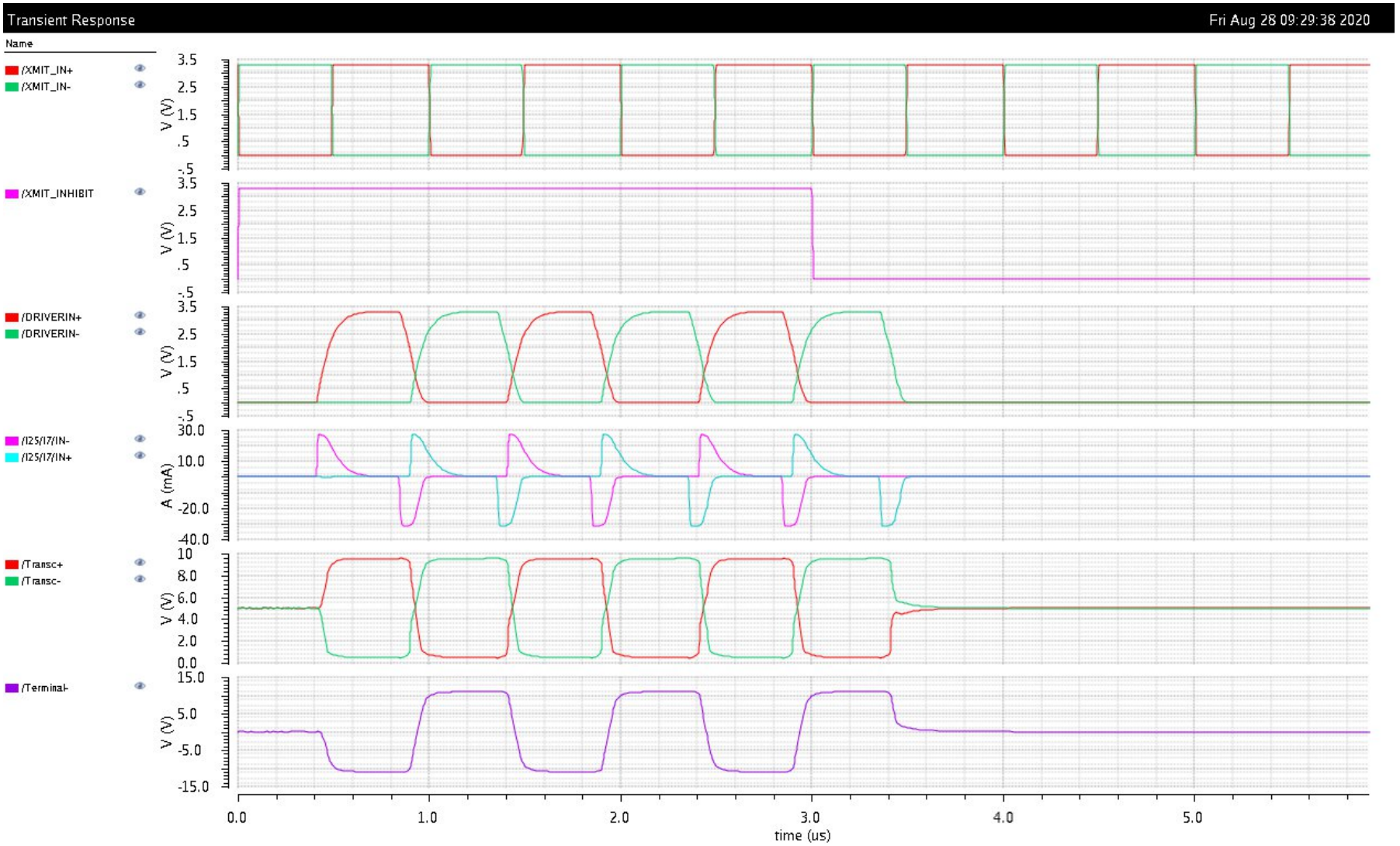


Figure 3.10. Transceiver circuit schematic transmission results 1, Cadence UMC130nm, IC

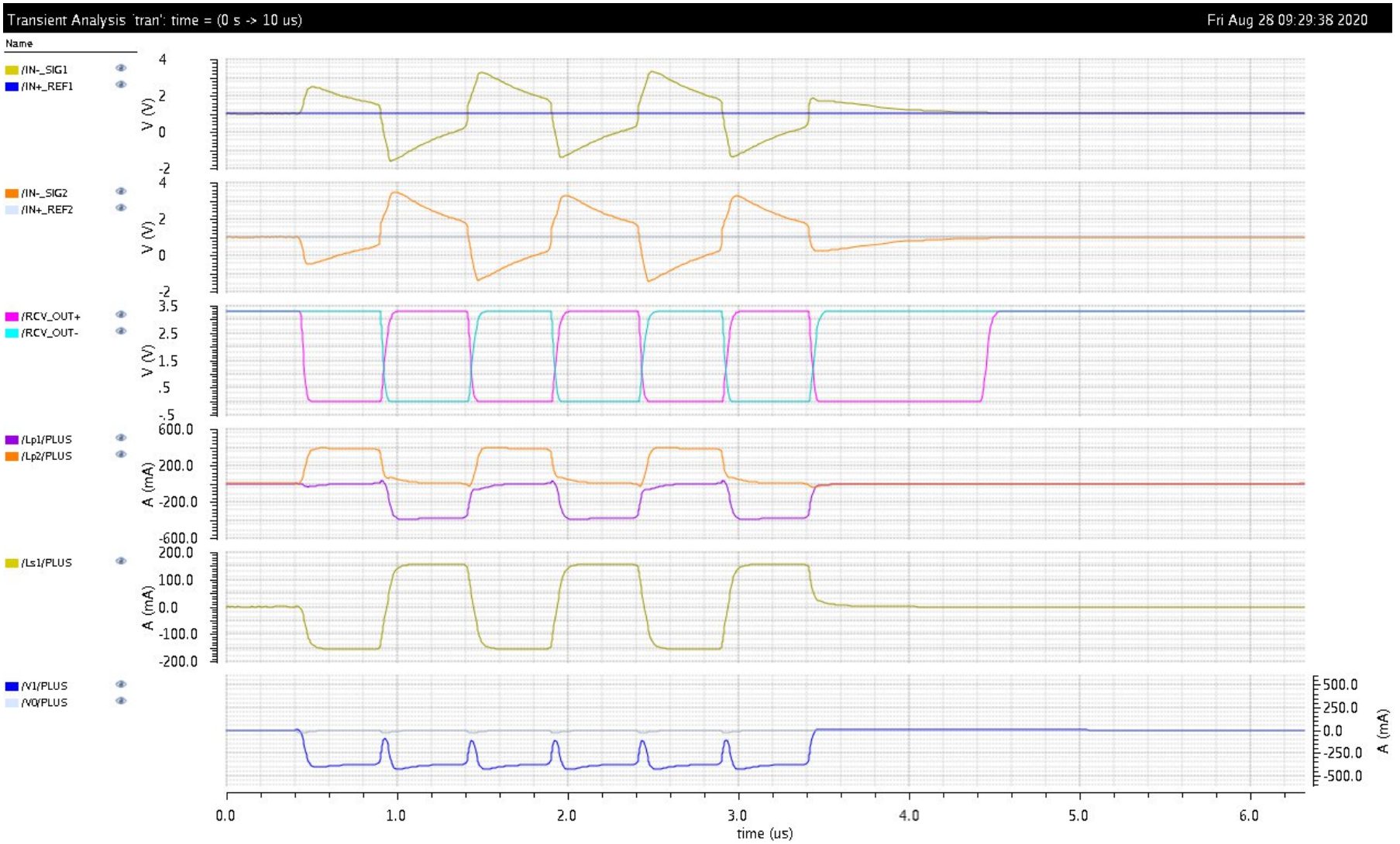


Figure 3.11. Transceiver circuit schematic transmission results 2, Cadence UMC130nm, IC

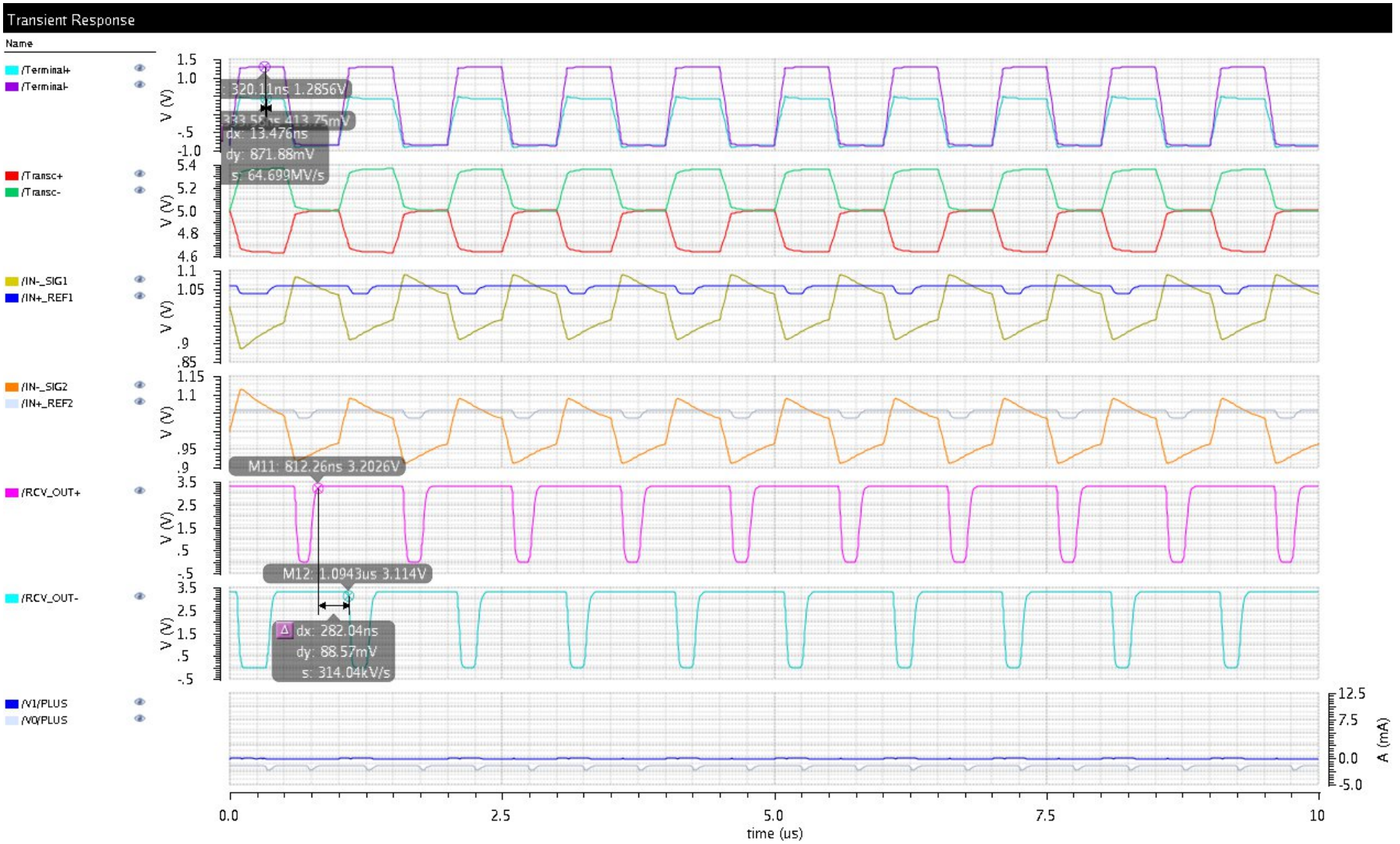


Figure 3.12. Transceiver circuit schematic receiving results 1, Cadence UMC130nm, IC

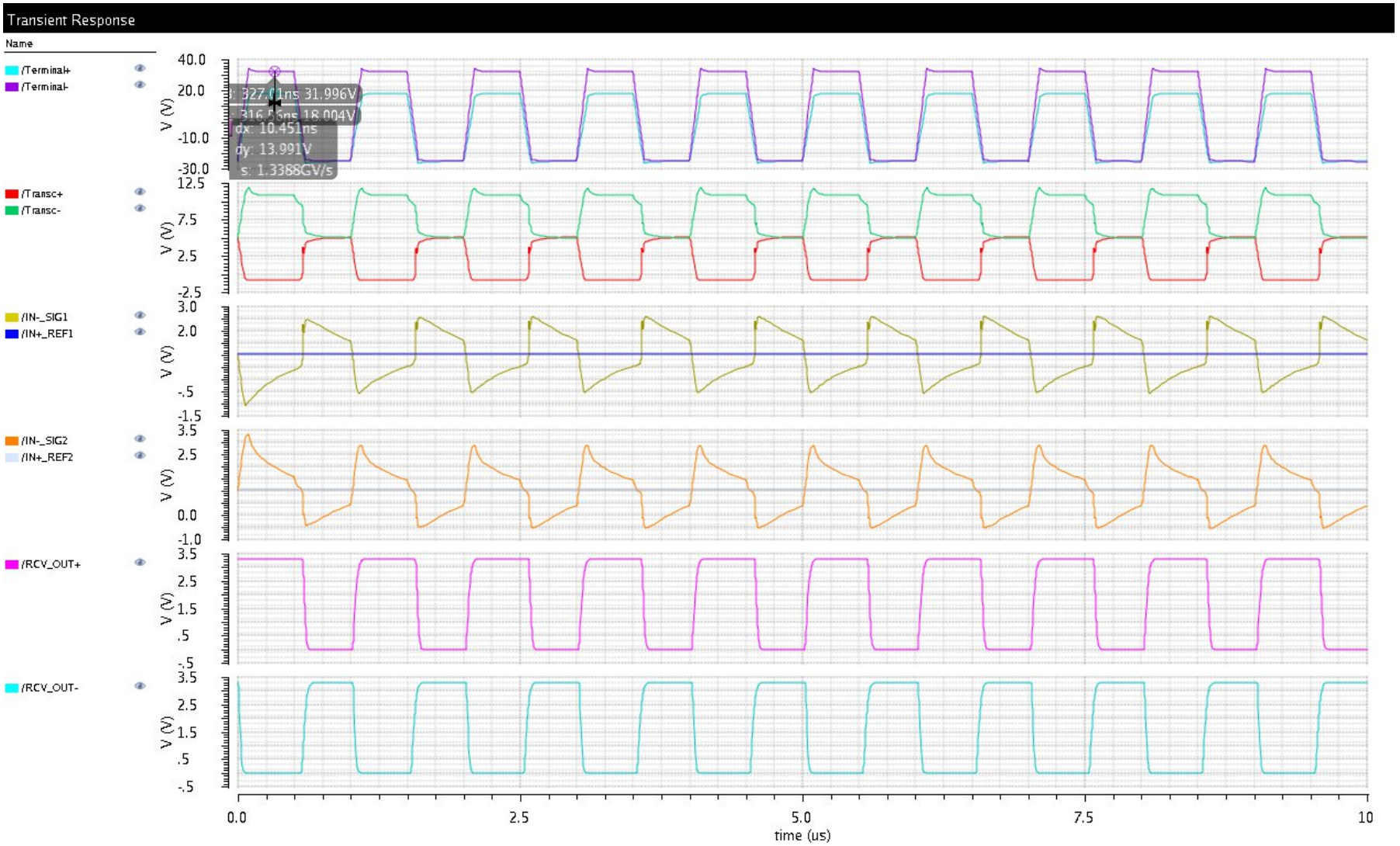


Figure 3.13. Transceiver circuit schematic receiving results 2, Cadence UMC130nm, IC

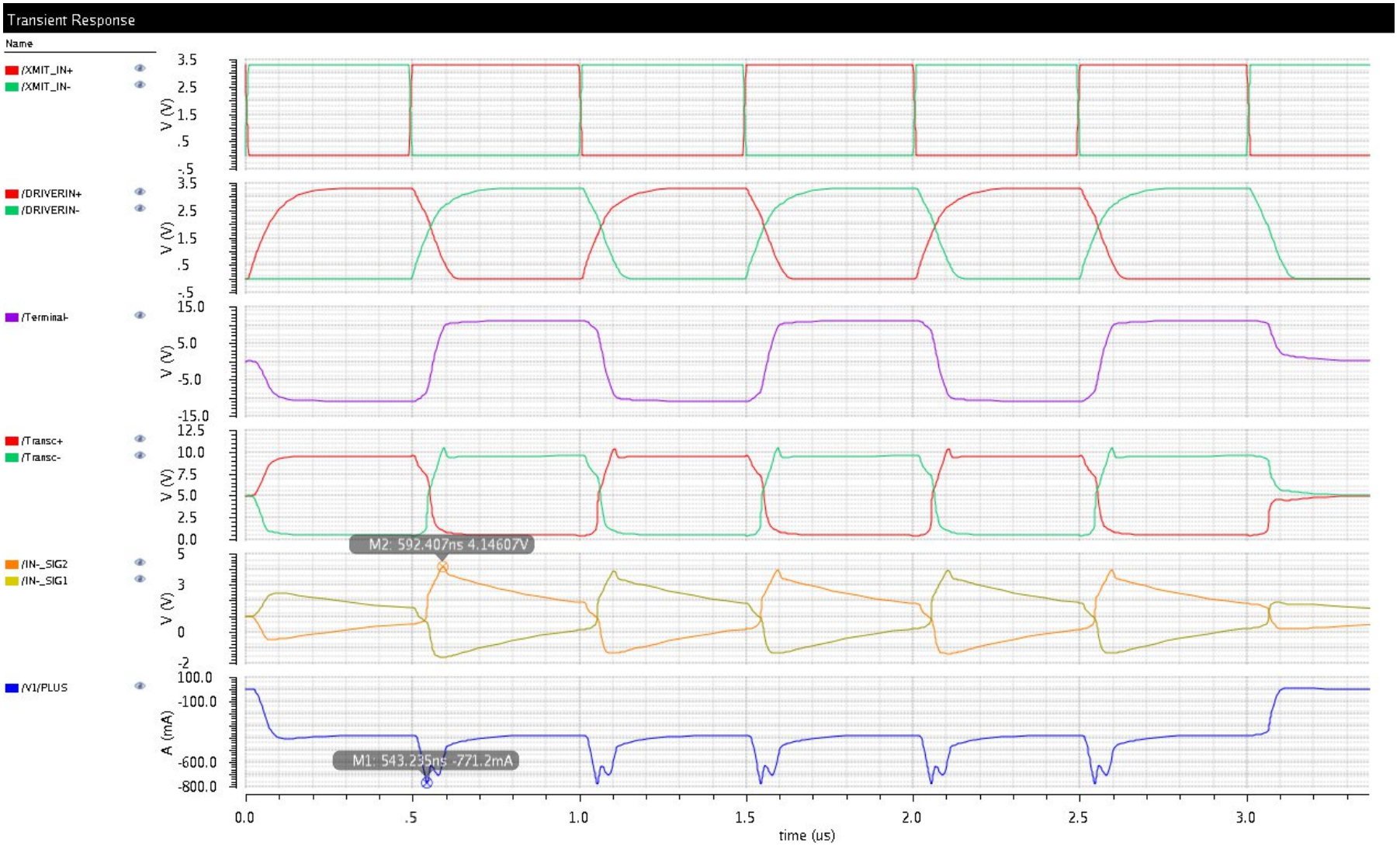


Figure 3.14. Transceiver circuit schematic transmission results (Overshoots present), Cadence UMC130nm, IC

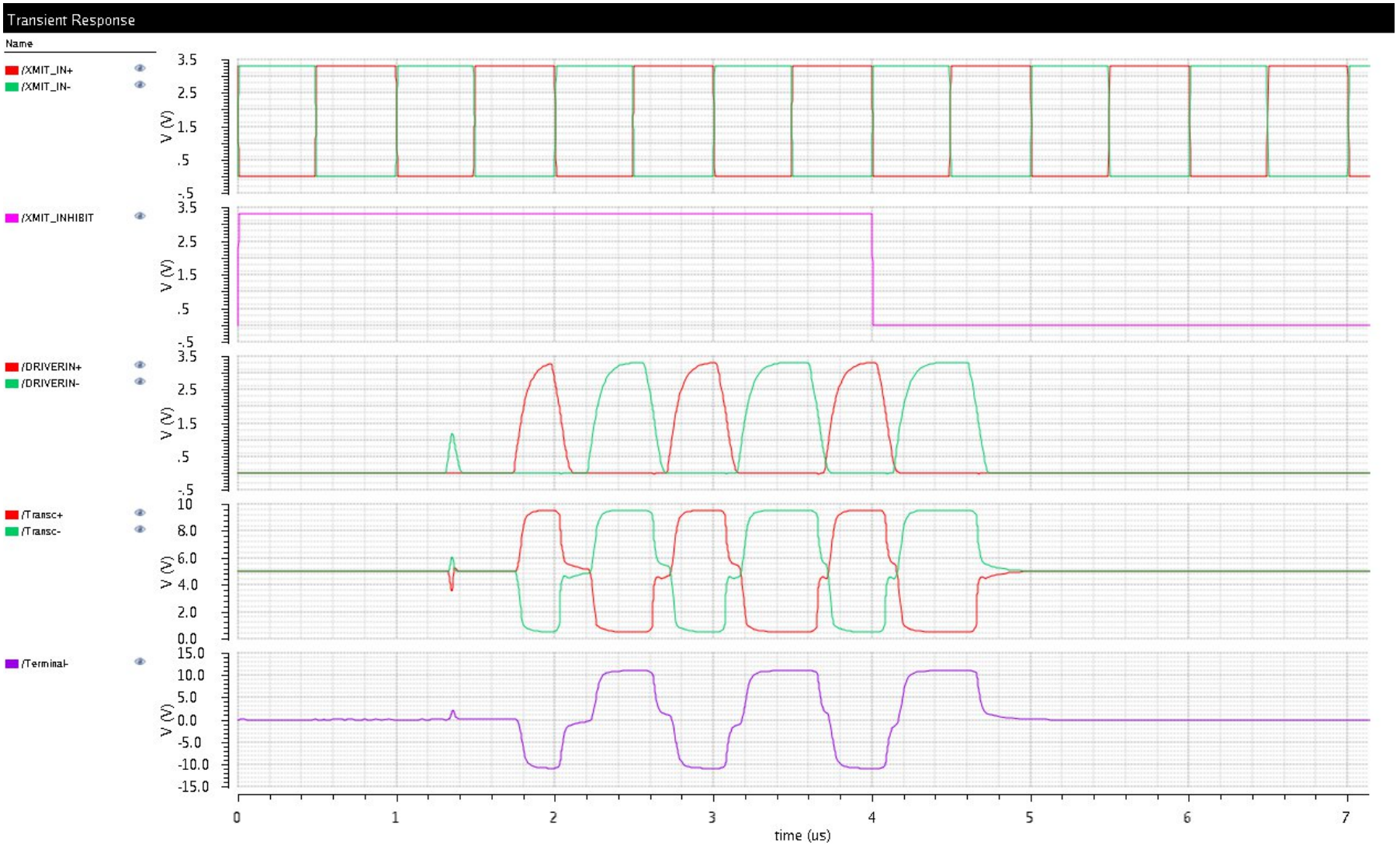


Figure 3.15. Transceiver circuit schematic transmission results (ill-formed transmission wave by enlarging the non-overlapping effect), Cadence UMC130nm, IC

3.2. Experimental Results

In this section the actual PCB board results and extracted layout simulation results are presented. For the PCB project, the setup images and oscilloscope results are shown. For the IC, layout images with post layout simulations are shown.

3.2.1. PCB, board simulations

First prototype of the PCB board is in Figure 3.16. Altium schematic and layouts are shown in Figures 3.17 and 3.18. Figure 3.19 is the functional diagram of the PCB board. Layout and schematics presented here have been designed to be physically configurable. LT1210 (current feedback amplifier) and SN74AHCT1G08 (Logical AND gate) components are configured to be out of the circuit. Current feedback amplifier (CFA) was originally simulated to show another solution for switch gate driving, but due to the larger current, required proper transmission signal was produced on the transmitter only with high current consumption. Besides the gate drive voltages were chosen to be between 1.65 V and 3.2 V as opposed to 0 V and 3.3 V. It was assumed that since the threshold voltage of NMOS SI7336ADP was 2.9 V, it would cause no problems. However, even at the low voltage of 1.65 V, current was measured on the drain of the NMOS and CFA was removed from the circuit. Logical AND gate in the other hand was removed since the gate driver FAN3227TMX showed better performance. Also the collector output of the LM311 comparator is later on connected to the ground which necessary for low output of the LM311 comparator.

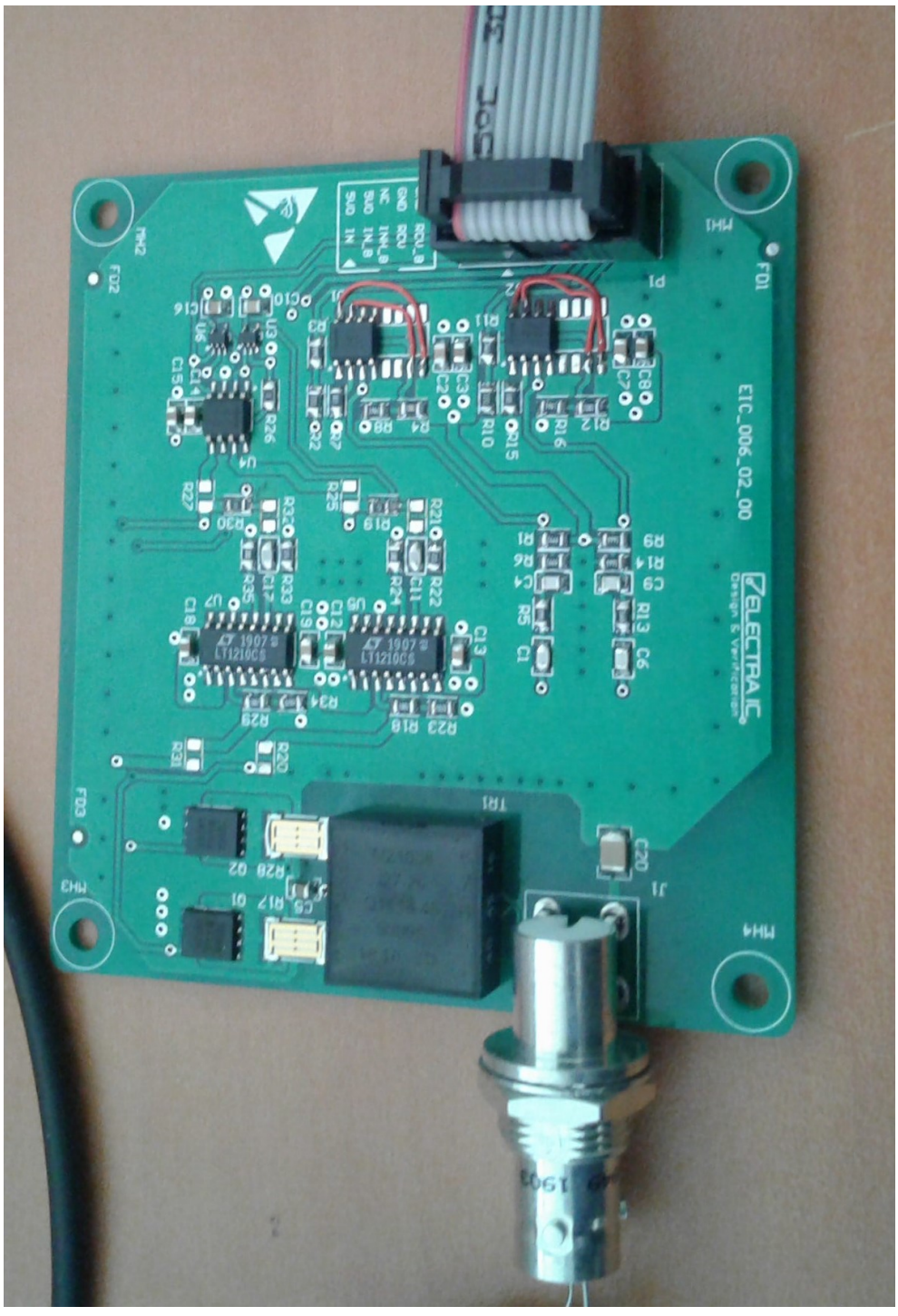


Figure 3.16. Transceiver PCB circuit board

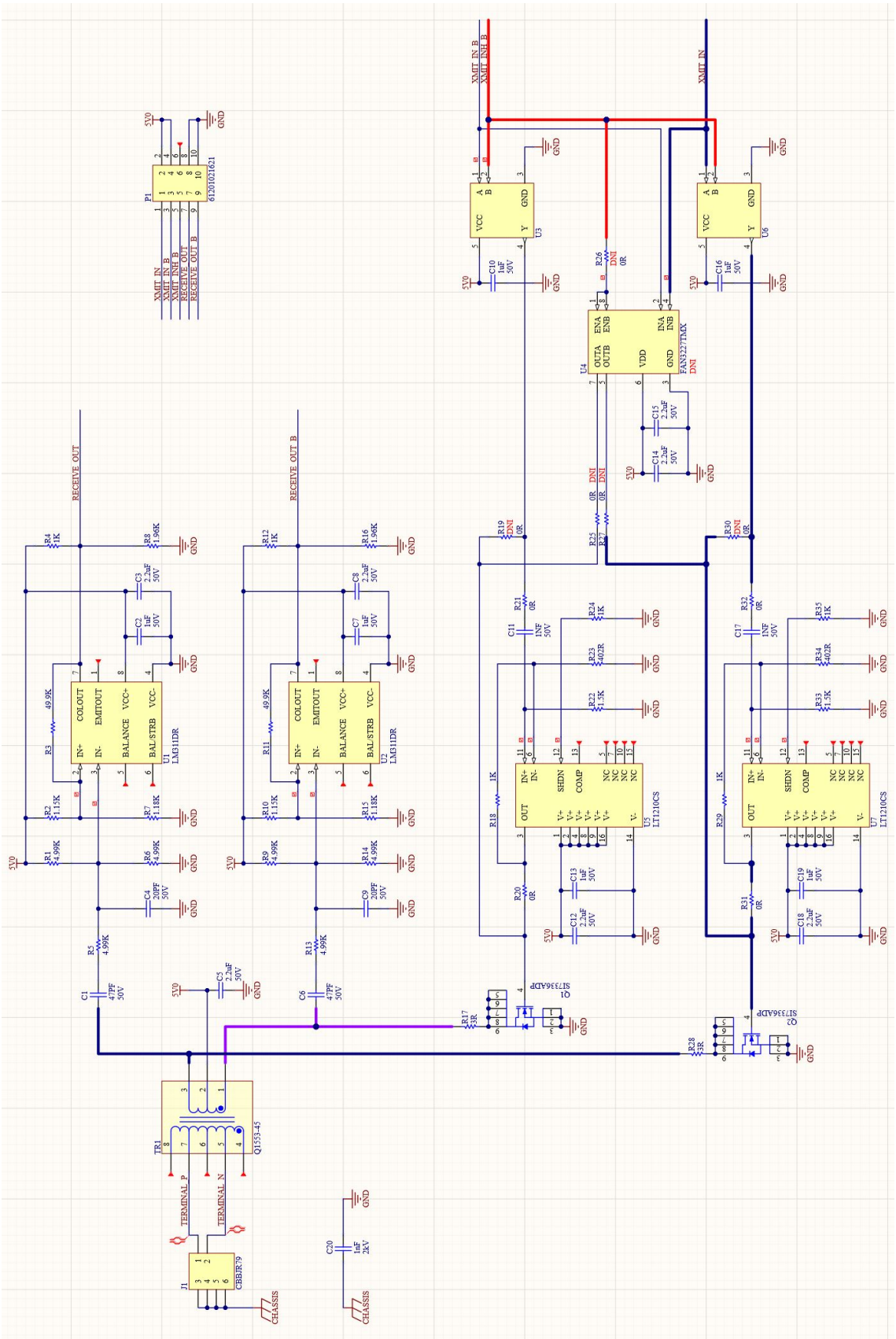


Figure 3.17. Transceiver PCB Altium circuit schematic

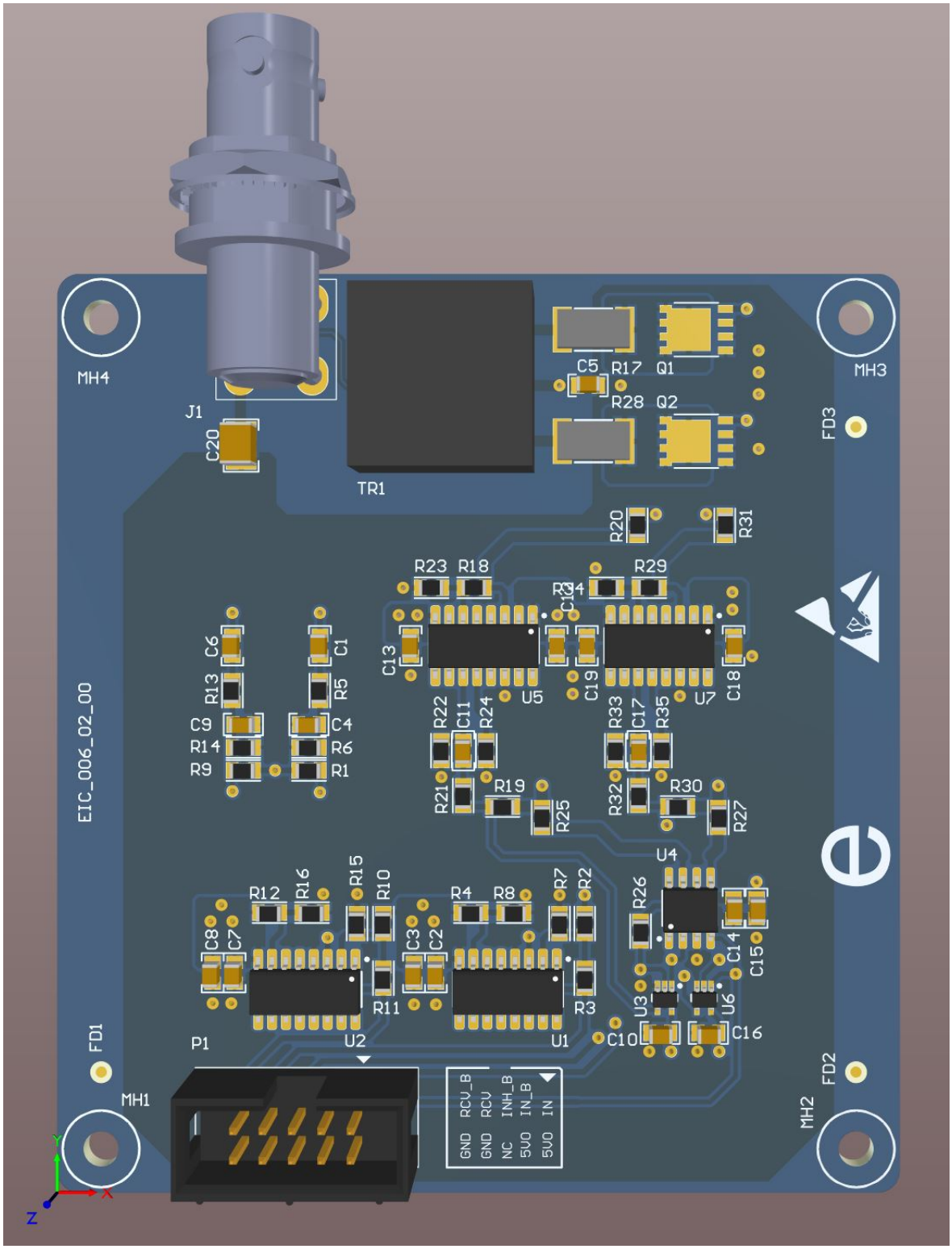


Figure 3.18. Transceiver PCB Altium layout

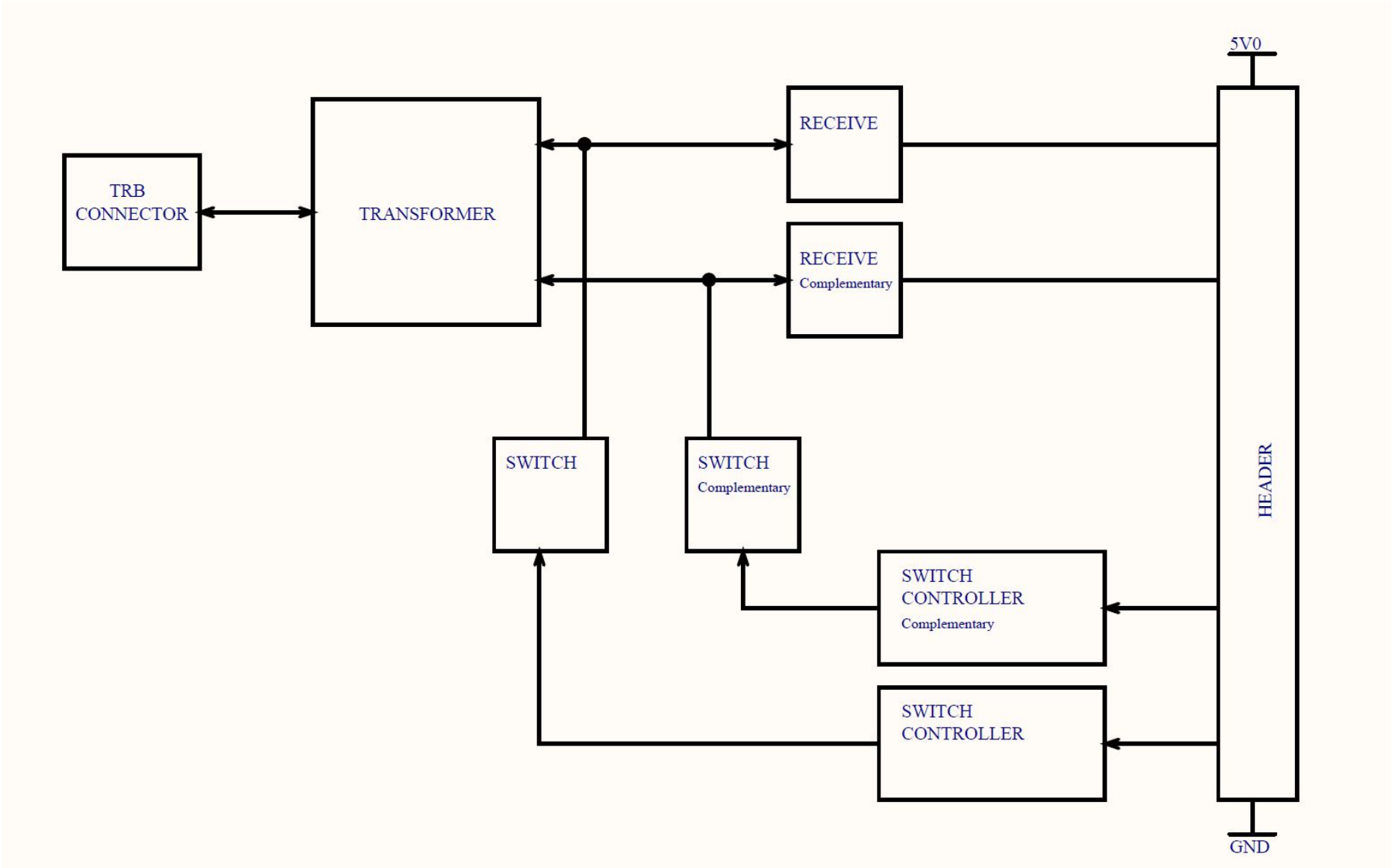


Figure 3.19. Transceiver PCB Altium layout

Using the PCB in Figure 3.16, the setup in Figure 3.20 is made. The PCB is transformer coupled to the stub, and the transmission signal on the stub, having driven from a TTL input is shown in Figure 3.21. Line impedance in which the stub connection is made 72Ω.

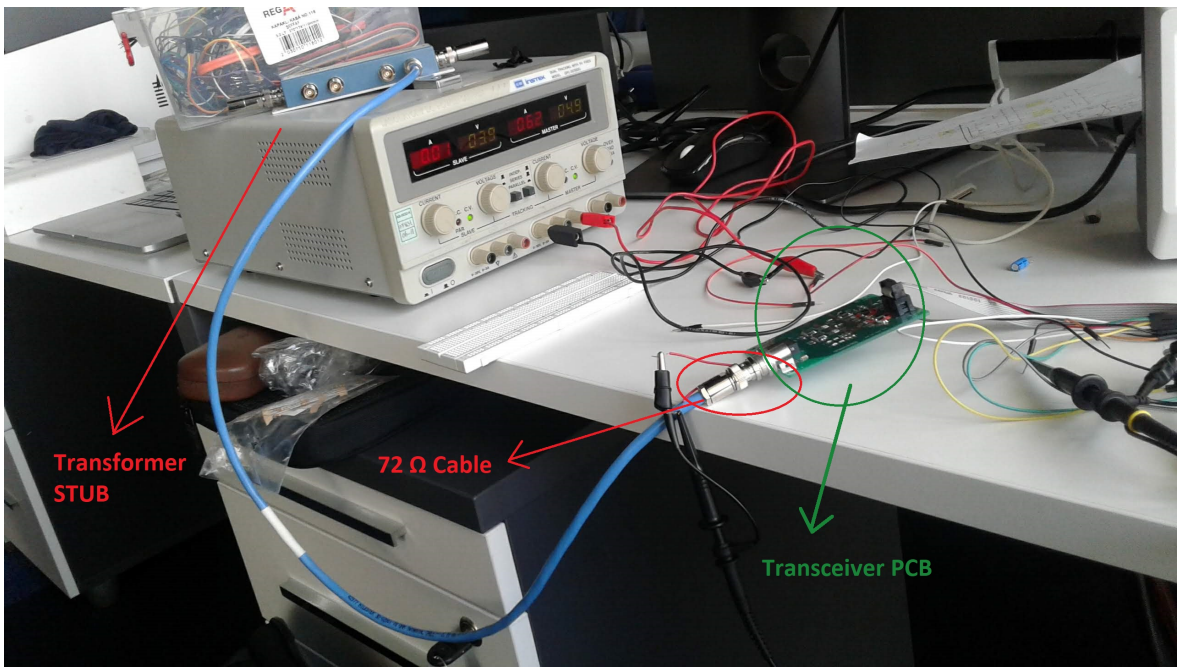


Figure 3.20. Transceiver PCB test setup 1

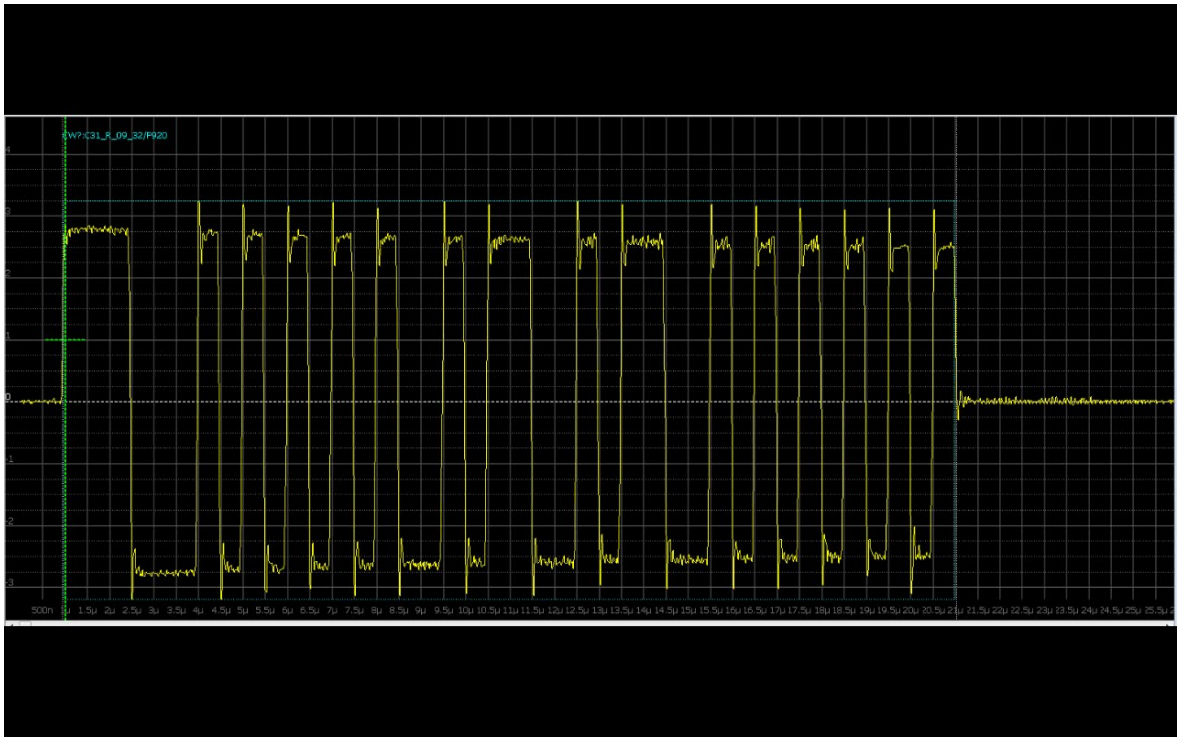


Figure 3.21. Transceiver PCB transmission signal on the stub

Overshoot is measured to be around 500mV, rise and fall times around 70ns and peak to peak voltage approximately 5V. Figure 3.22 shows the transmitted signal on the terminals of the transceiver under same setup. Peak to peak voltage is measured to be 20V with an overshoot/undershoot of about 1.2V. The gates of the switches are driven as depicted in Figure 3.23.

Figure 3.22. Transceiver PCB transmission signal on the terminal, with 72Ω cable load

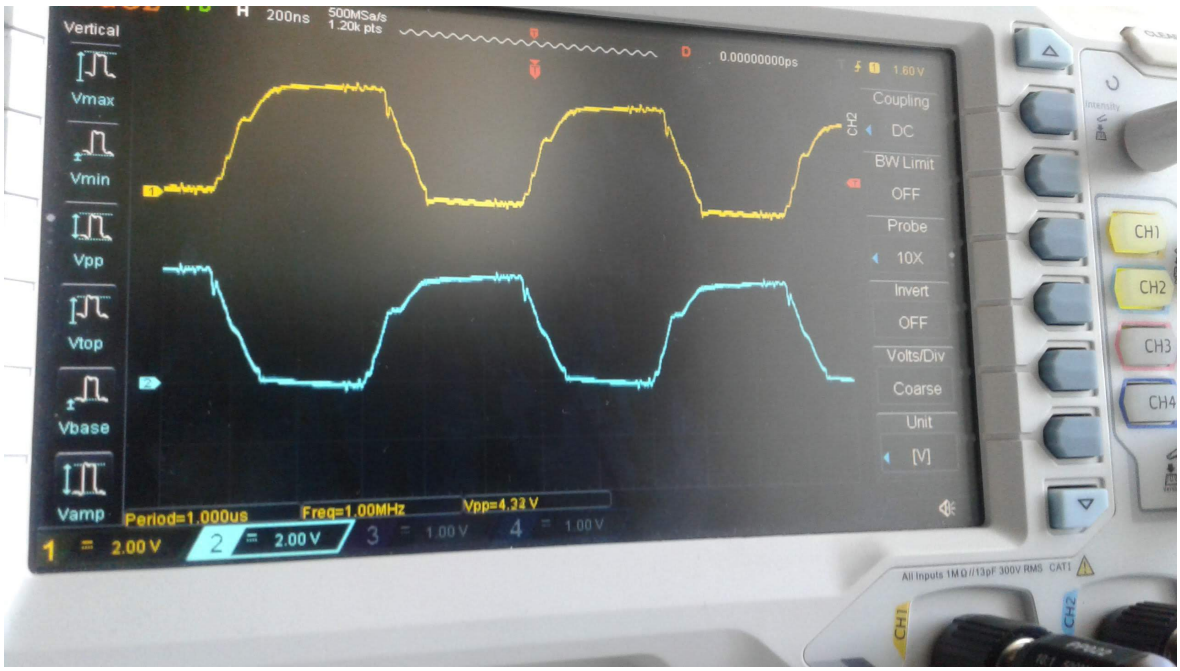


Figure 3.23. Transceiver PCB transmission switching gate driving signal

By looking at Figure 3.23, we can see that the gates are being driven with an overlapping signal. This is the primary cause of the overshoots observed in Figure 3.22.

Using another test setup in Figure 3.24, the PCB board is connected to HOLT2579 which is another manufactured 1553 transceiver, through a bus stub and transmission and receiving is tested. Figure 3.25 is the signal picked up by the PCB which is transmitted from HOLT2579.

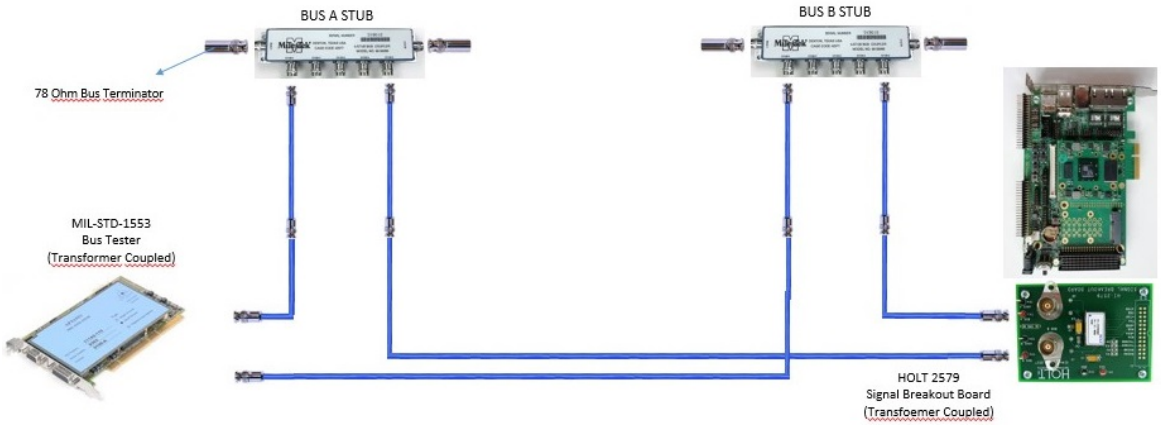


Figure 3.24. Transceiver PCB communication test setup with HOLT2579

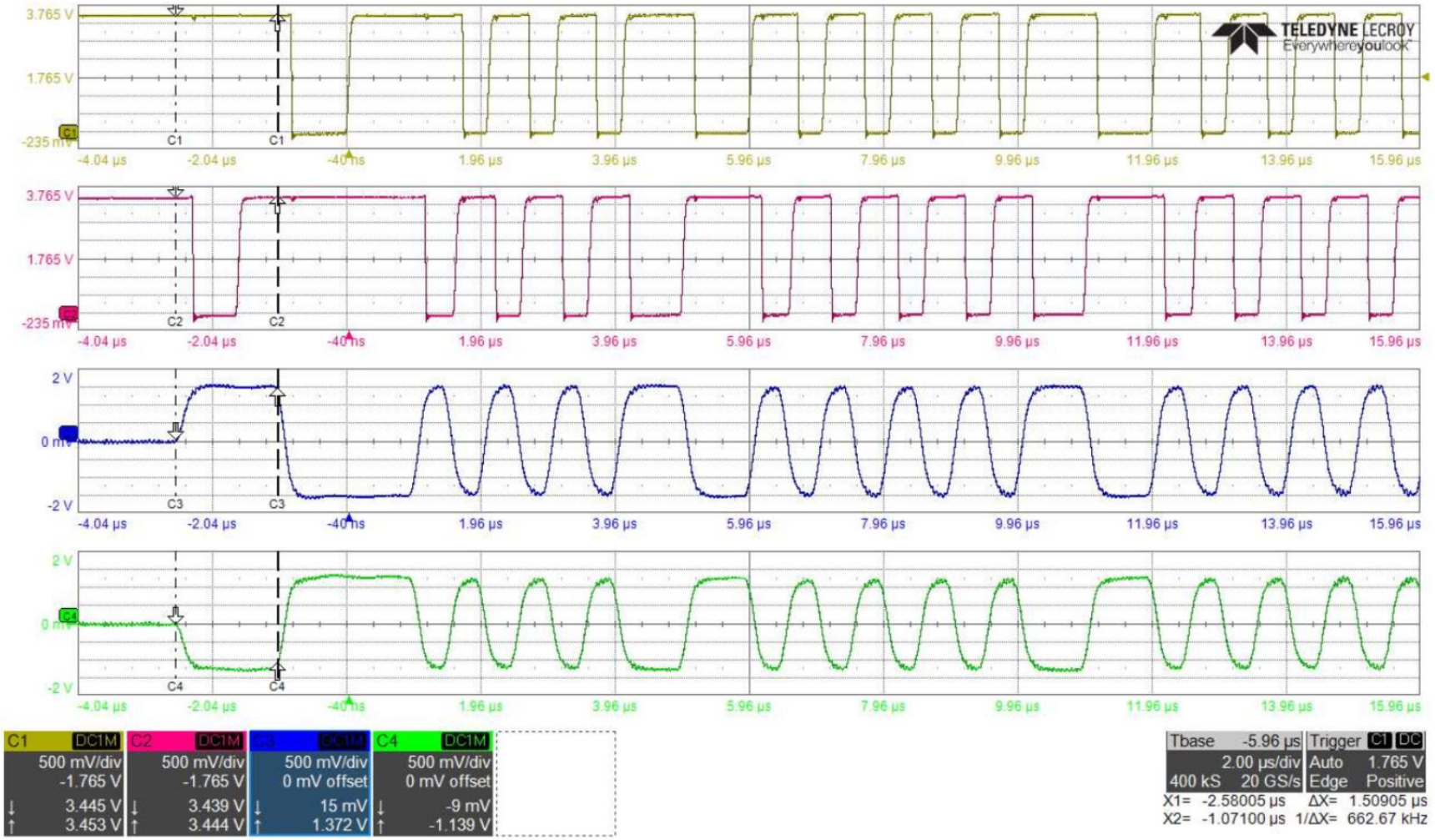


Figure 3.25. Transceiver PCB receiving message signal from HOLT2579

Top two signal in Figure 3.25 are the received signals which the bottom two are the terminal signals. As we discussed before, there is a relatively larger zero crossing delay at the received first bit which was simulated in Figure 2.19 in LTSpice. That effect was captured in simulation by exaggerating the value of the input capacitor for the DC block. From the same logic, this problem can be improved for the PCB by reducing the 100pF capacitors (C_5 and C_6) in Figure 3.1 to around 20pF.

Using the same setup in Figure 3.24, test message signal from the PCB is transmitted and received (decoded) successfully by HOLT2579. In Figure 3.26, the bottom signals are the transmitted signals from the PCB on the stub, and top ones are the received signals by HOLT2579. Finally, the transmitted word from the board to the stup with a residual voltage of 200mV is measured in Figure 3.27.

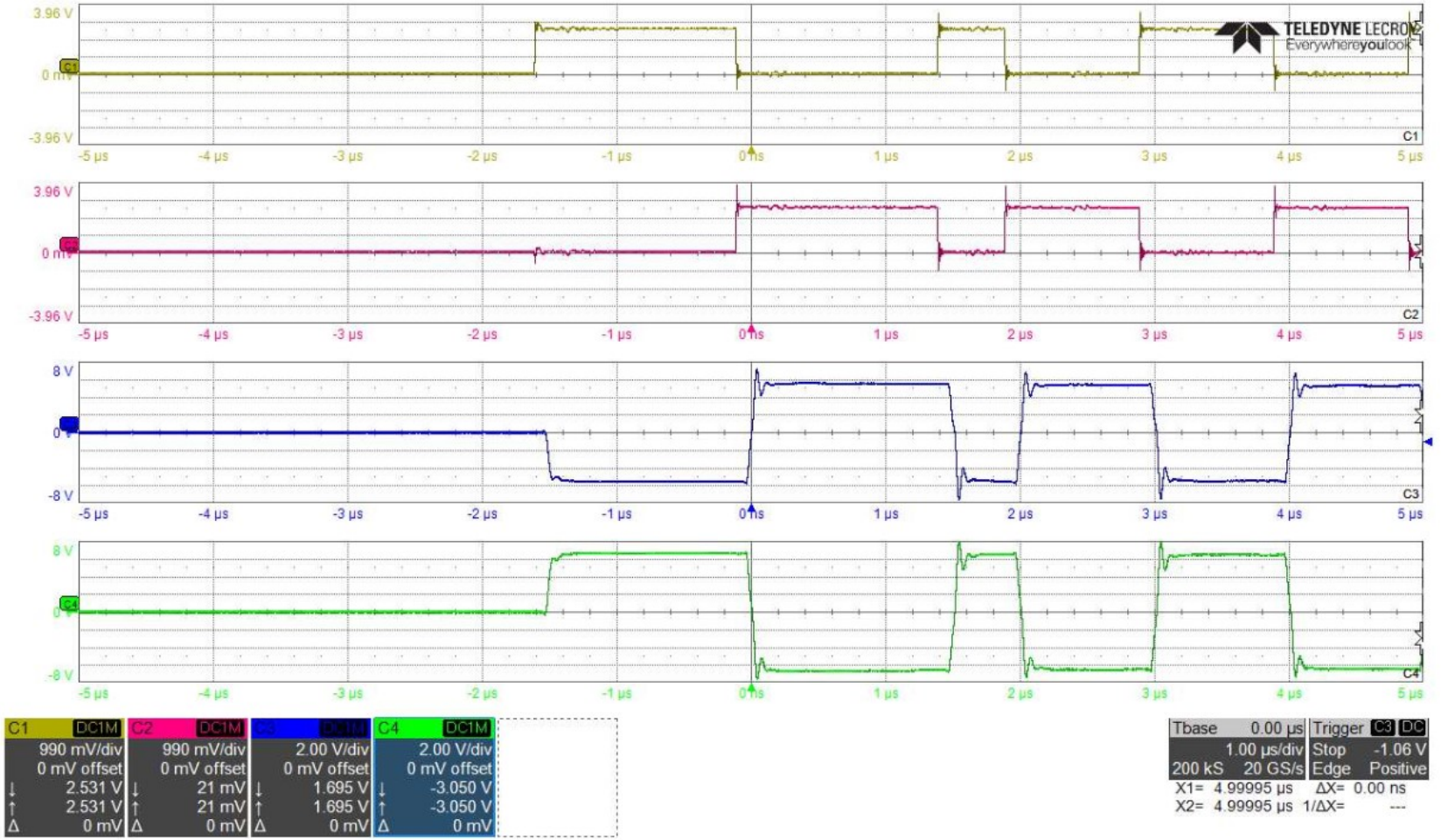


Figure 3.26. Transceiver PCB transmitting message signal to HOLT2579

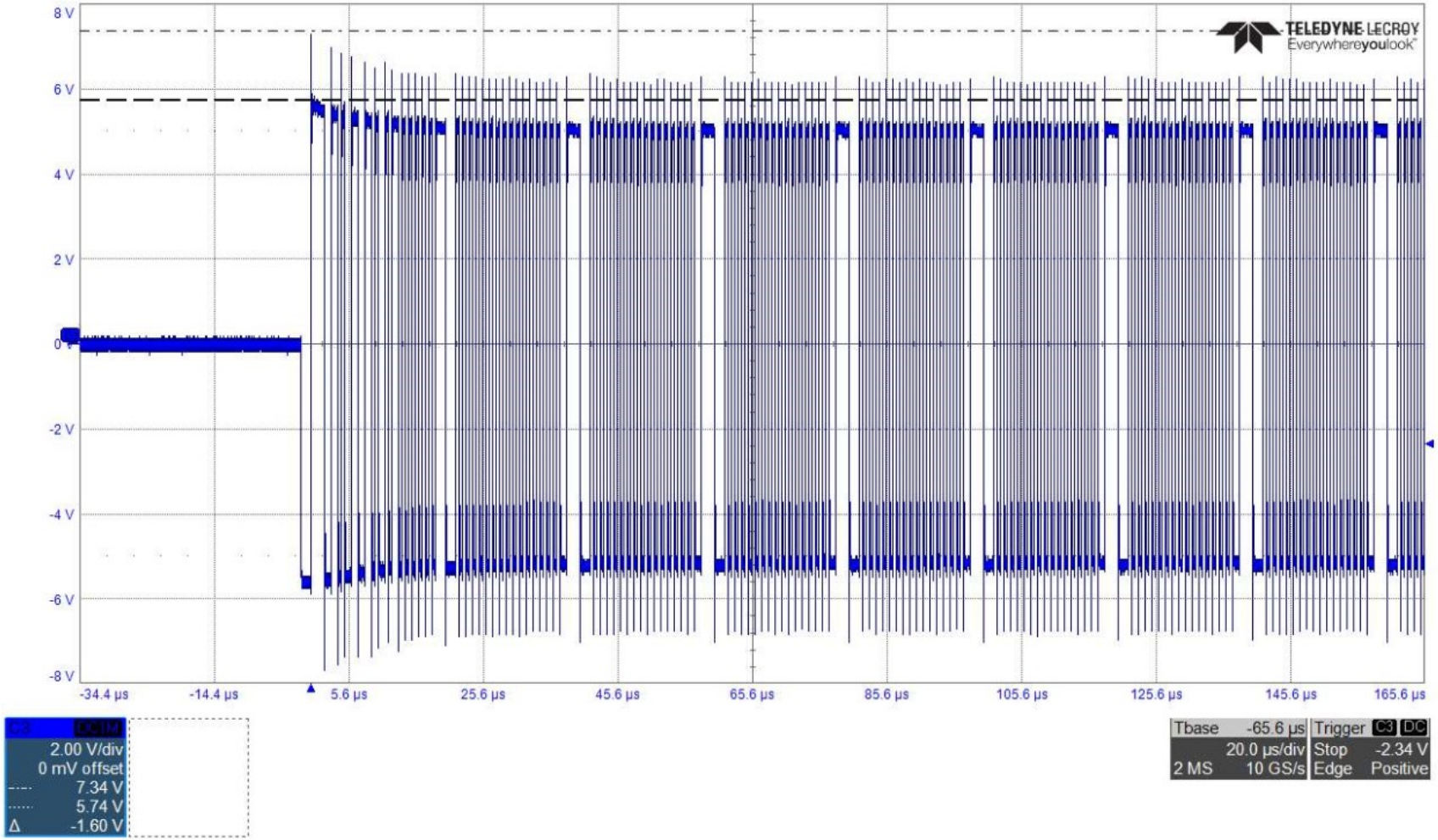


Figure 3.27. Transceiver PCB transmitting message signal to HOLT2579, stub residual voltage of 200mV

3.2.2. IC extracted layout post simulations

Figures 3.28, 3.29, 3.30 and 3.31 are the post layout simulations for the IC part of the project. These figures are very similar to that of Figures 3.10, 3.11, 3.12 and 3.13 discussed in schematic simulations. Peak to peak transmission is about 21.4 V. Rise time 108 ns, fall time 104 ns, rms current consumed by 3.3 V supply is around 30 mA and through 5 V supply is approximately 289 mA. The main discrepancy between the post layout and schematic simulation is evidently the DRIVERIN+ and DRIVERIN- signals. This slow transition (which is not particularly undesirable in this case) is due to the large poly capacitance of the switching NMOS transistors drawn in layout. It is for this very reason that the delay capacitances of 2pF or even less in Figure 3.9 suffices for the non-overlapping effect. Recall that the larger the slope (or rise/fall times for that matter) at the switching gates, the less need for the large non-overlapping signals. Worst case zero crossing delay at the receiver is measured to be 297 ns in Figure 3.30 and as we can see, given the maximum terminal voltage in Figure 3.31 which is 14 Vp-p, the signal arriving at the receiver comparator differential input is just below 3.3 V (otherwise the transistor could be damaged).

As a final note on how the resistor network was determined in Figure 3.9, we can shortly say that the limiting factors for the resistors just after the DC blocking capacitor is the 3.3 V limit arriving at the comparator input. But increasing that resistor (R_2 in Figure 2.7) while it introduces large attenuation to prevent transistor damage, it also demands the reduction of C_2 in Figure 2.7.

Figures 3.32, 3.33, 3.34, 3.35, 3.36, 3.37 and 3.38 are the layouts of the IC part of the project.

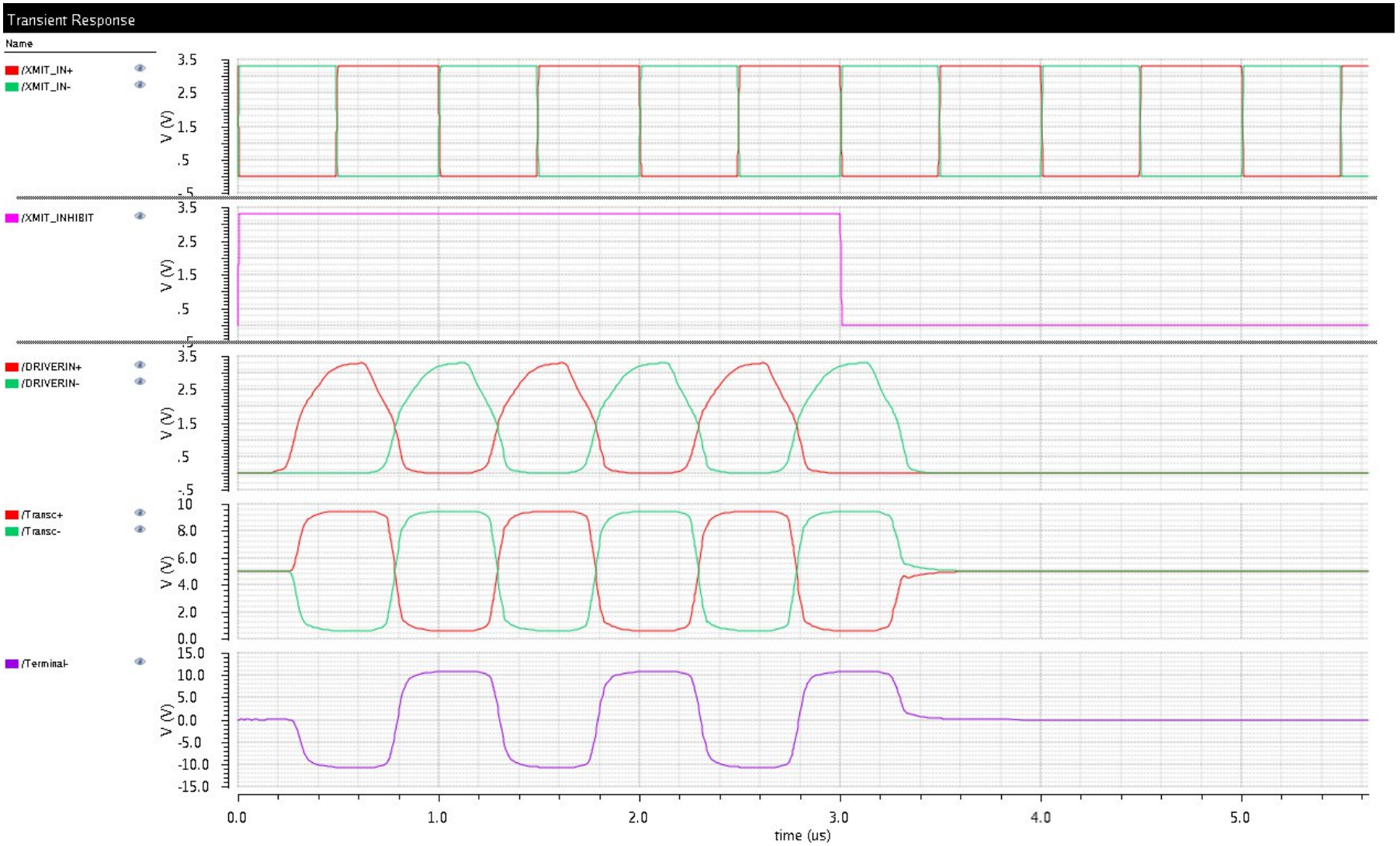


Figure 3.28. Transceiver circuit post layout transmission simulation results 1, Cadence UMC130nm, IC

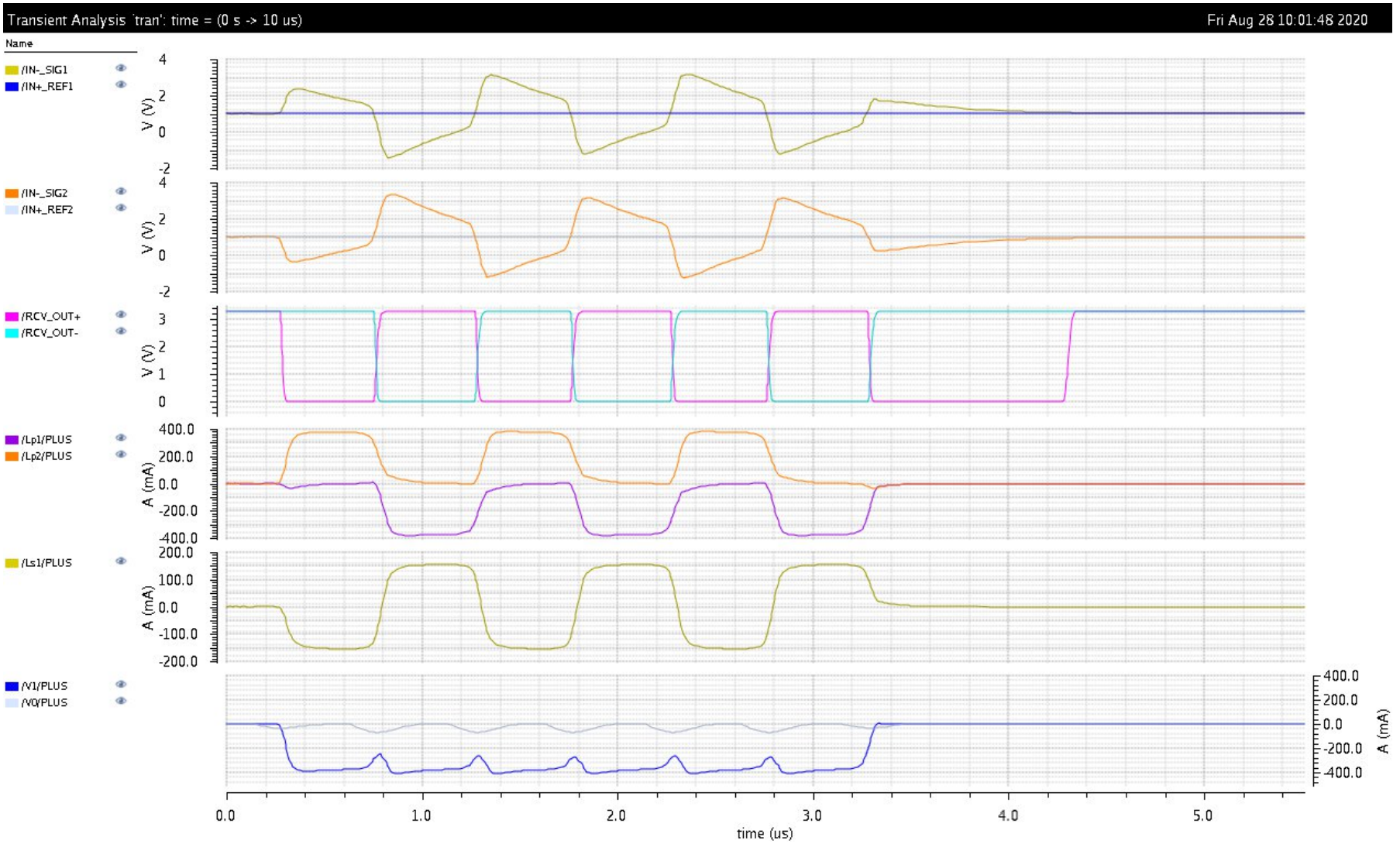


Figure 3.29. Transceiver circuit post layout transmission simulation results 2, Cadence UMC130nm, IC

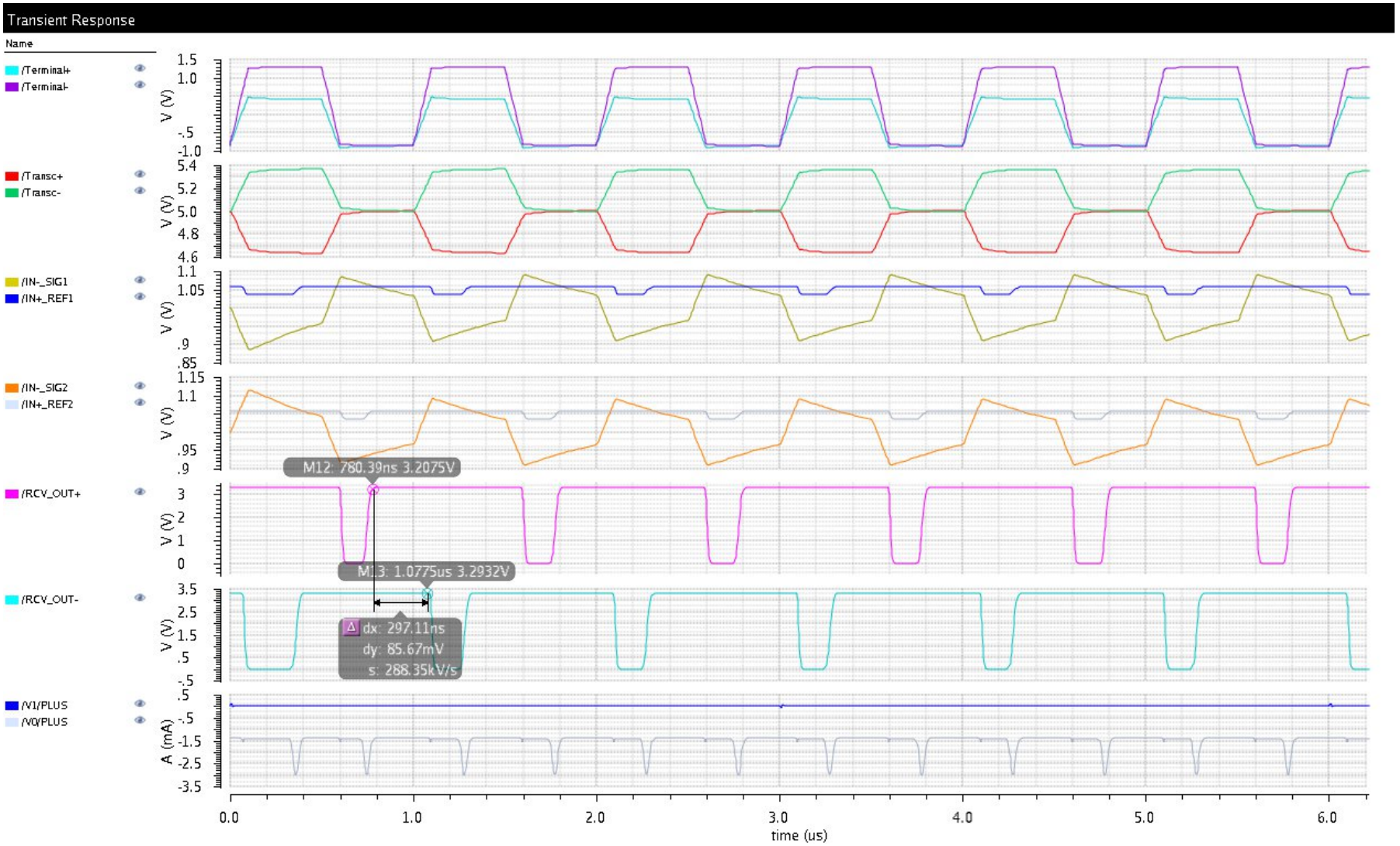


Figure 3.30. Transceiver circuit post layout receiving simulation results 1, Cadence UMC130nm, IC

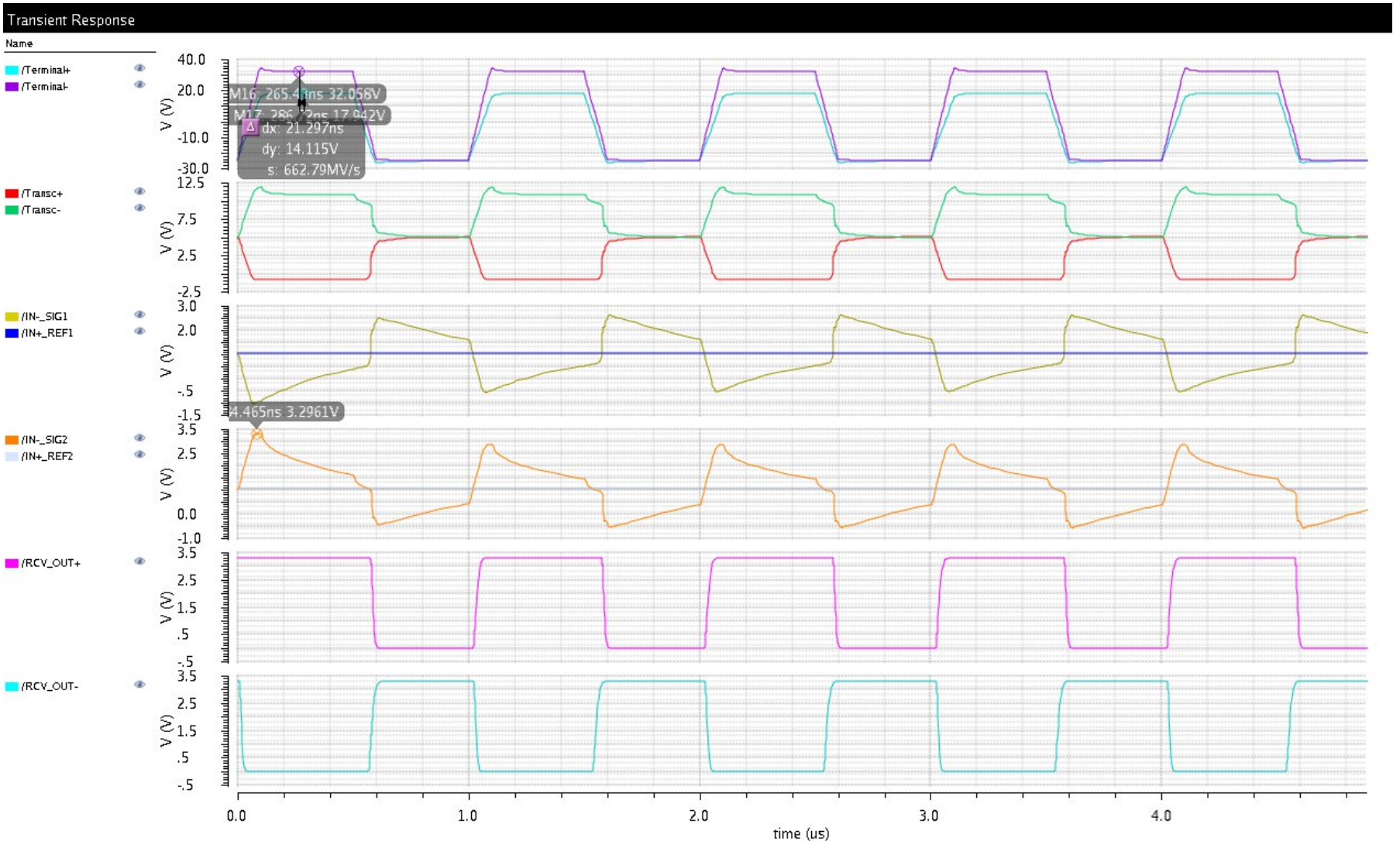


Figure 3.31. Transceiver circuit post layout receiving simulation results 2, Cadence UMC130nm, IC

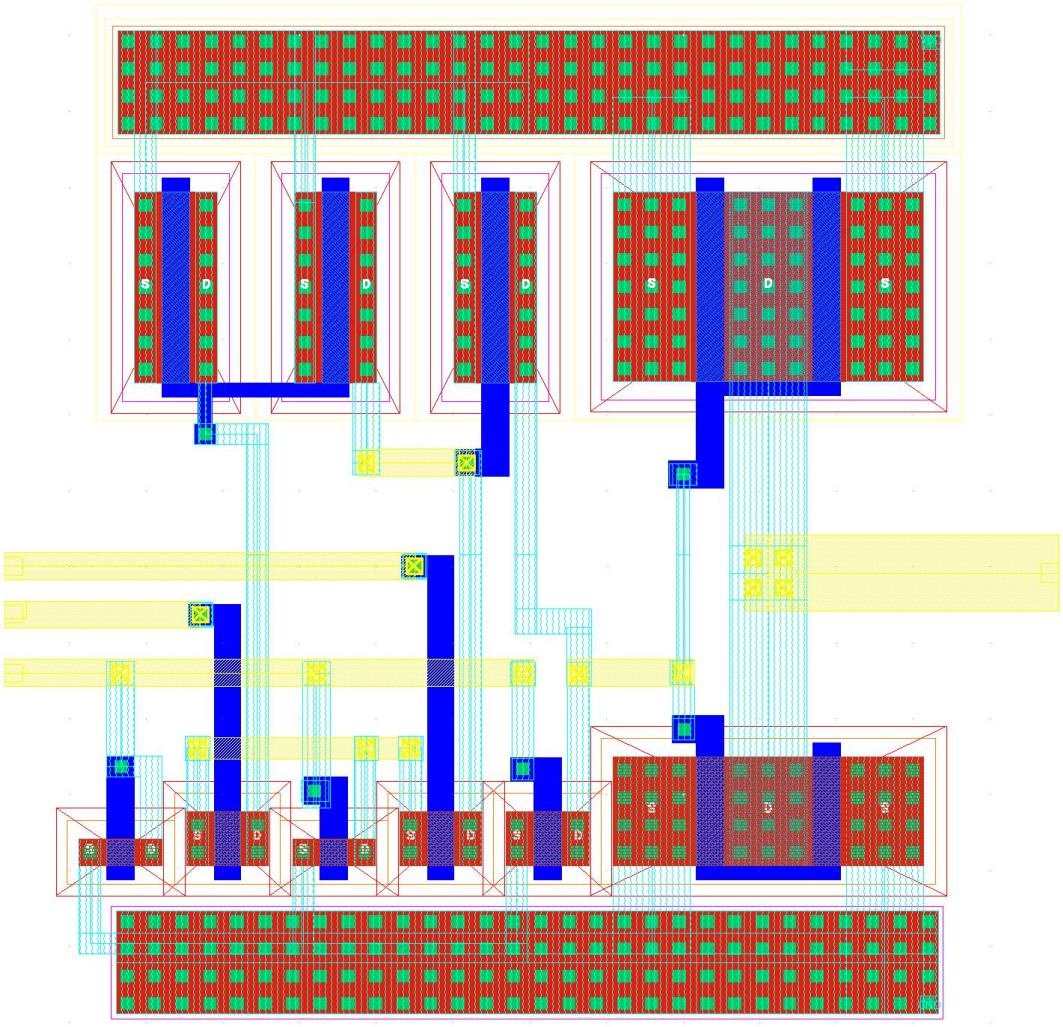


Figure 3.32. Comparator layout, Cadence UMC130nm, IC

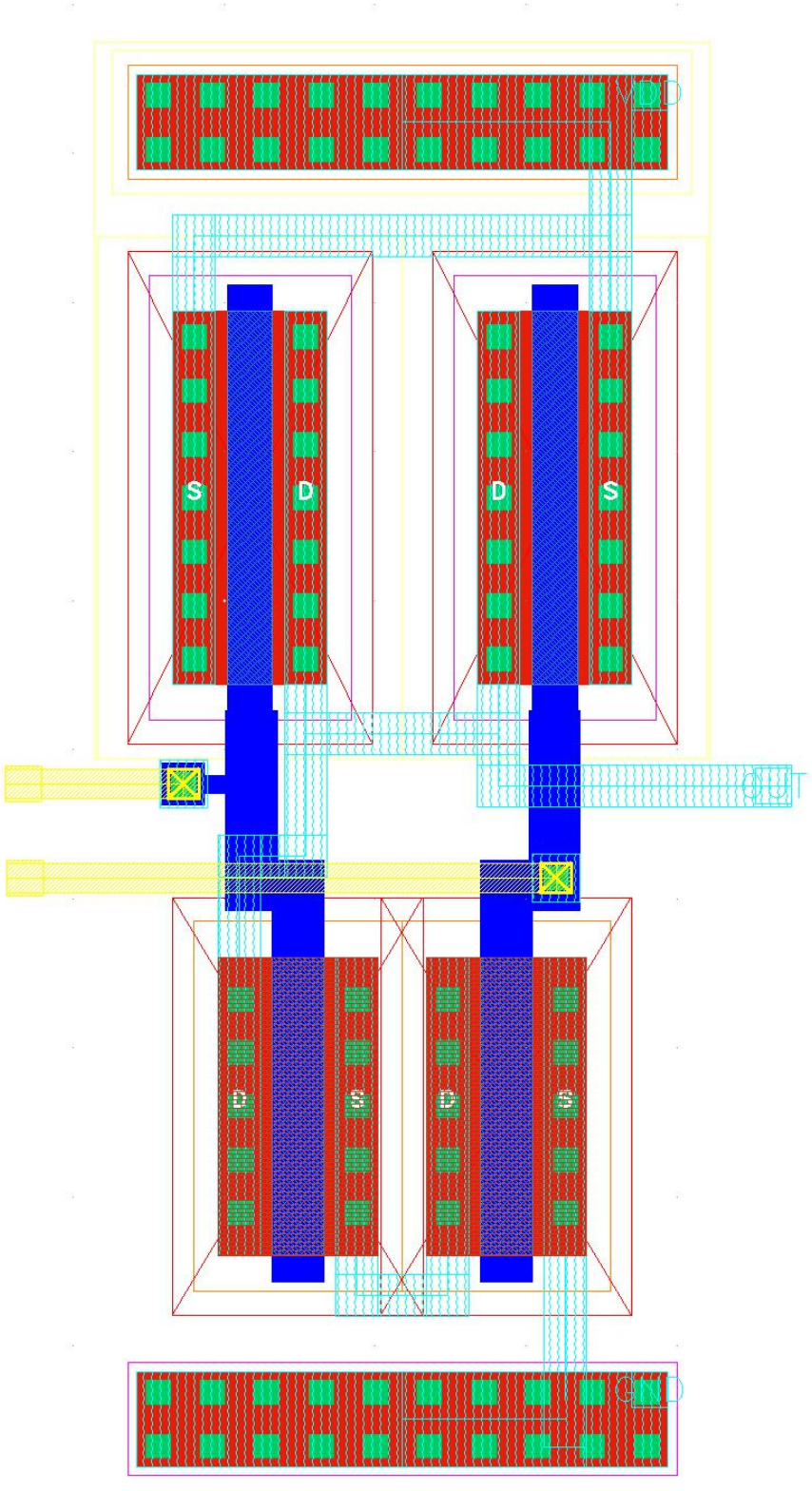


Figure 3.33. NAND2 layout, Cadence UMC130nm, IC

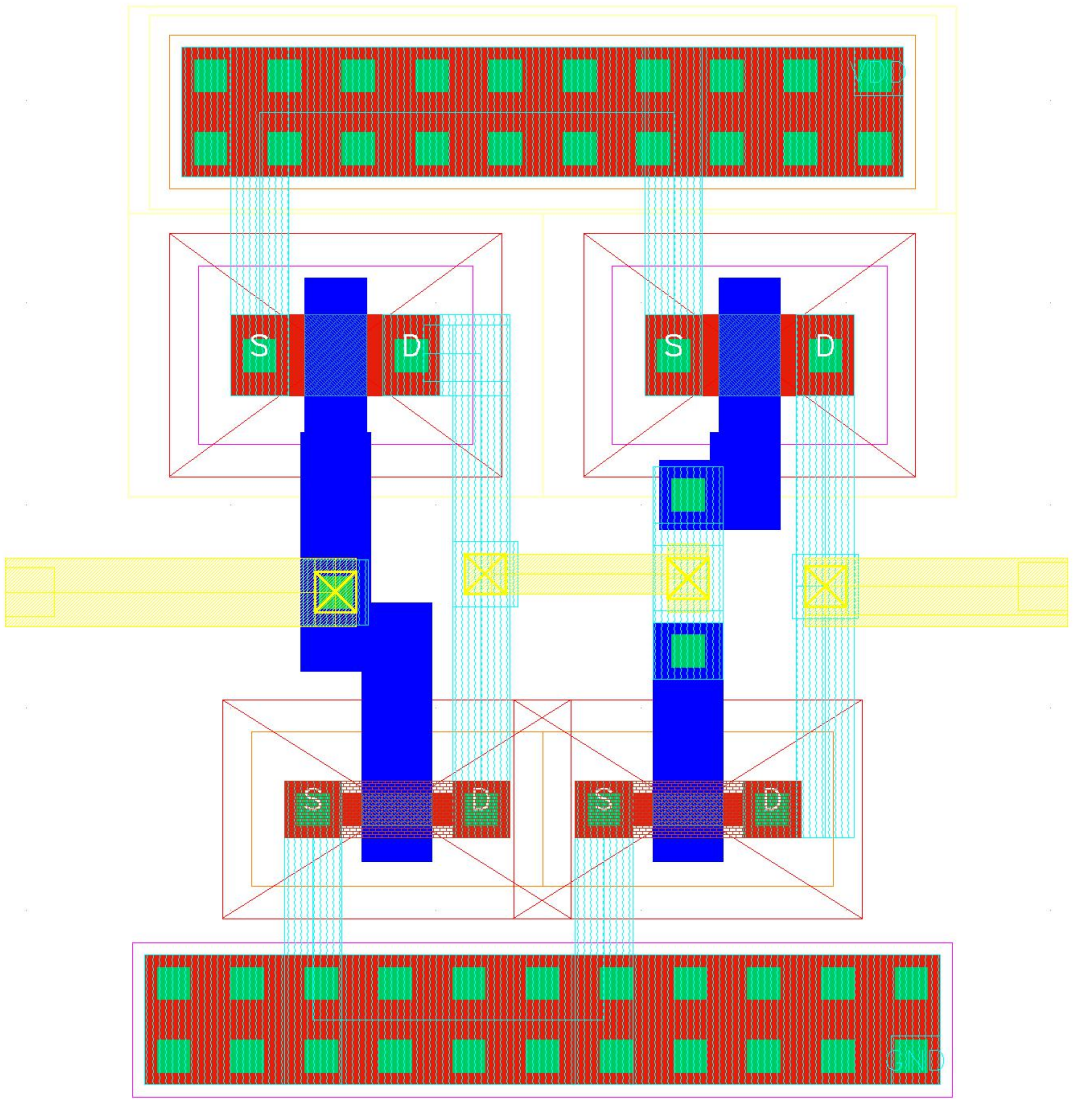


Figure 3.34. BUFF (Buffer) layout, Cadence UMC130nm, IC

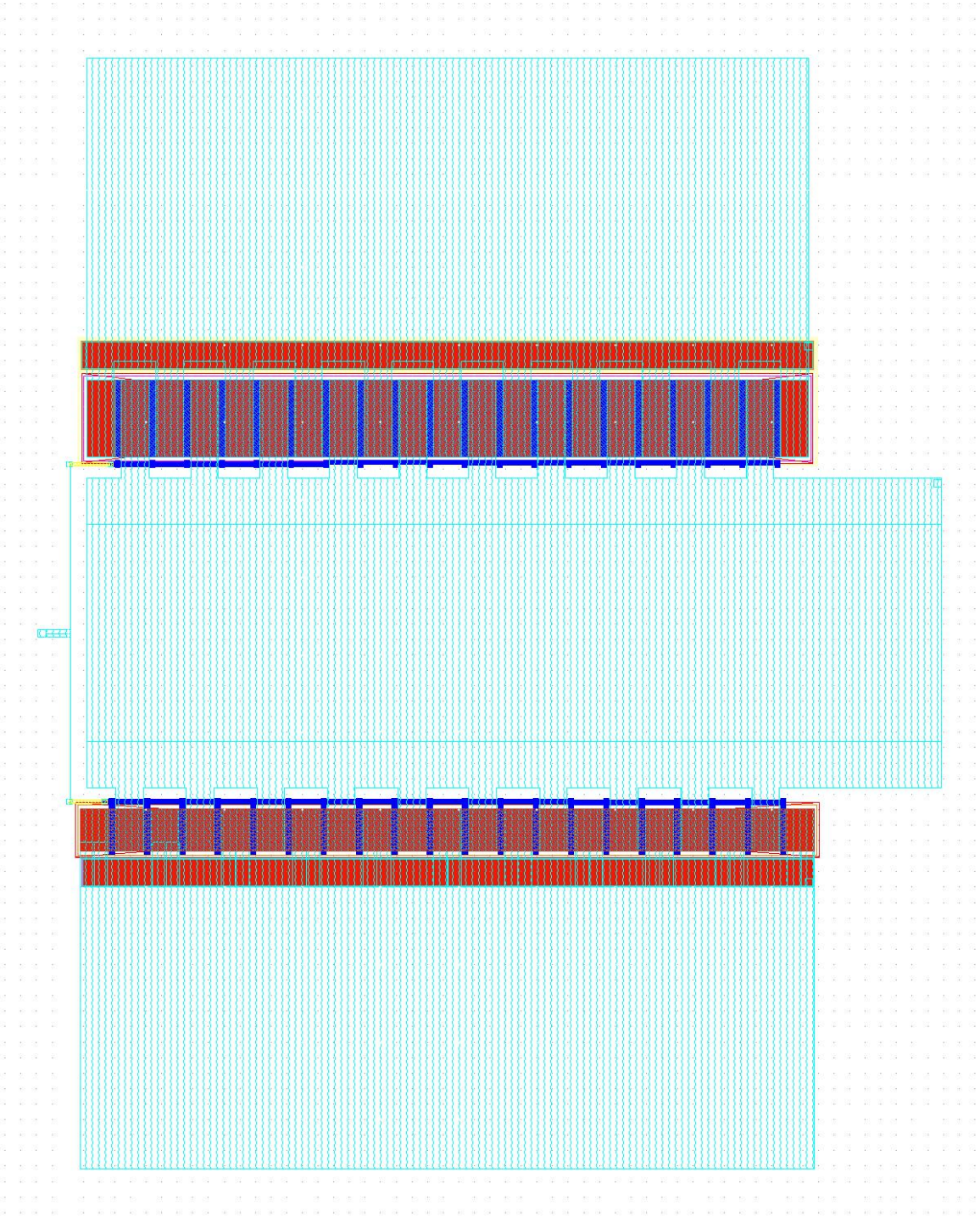


Figure 3.35. INV (gate driving inverter) layout, Cadence UMC130nm, IC

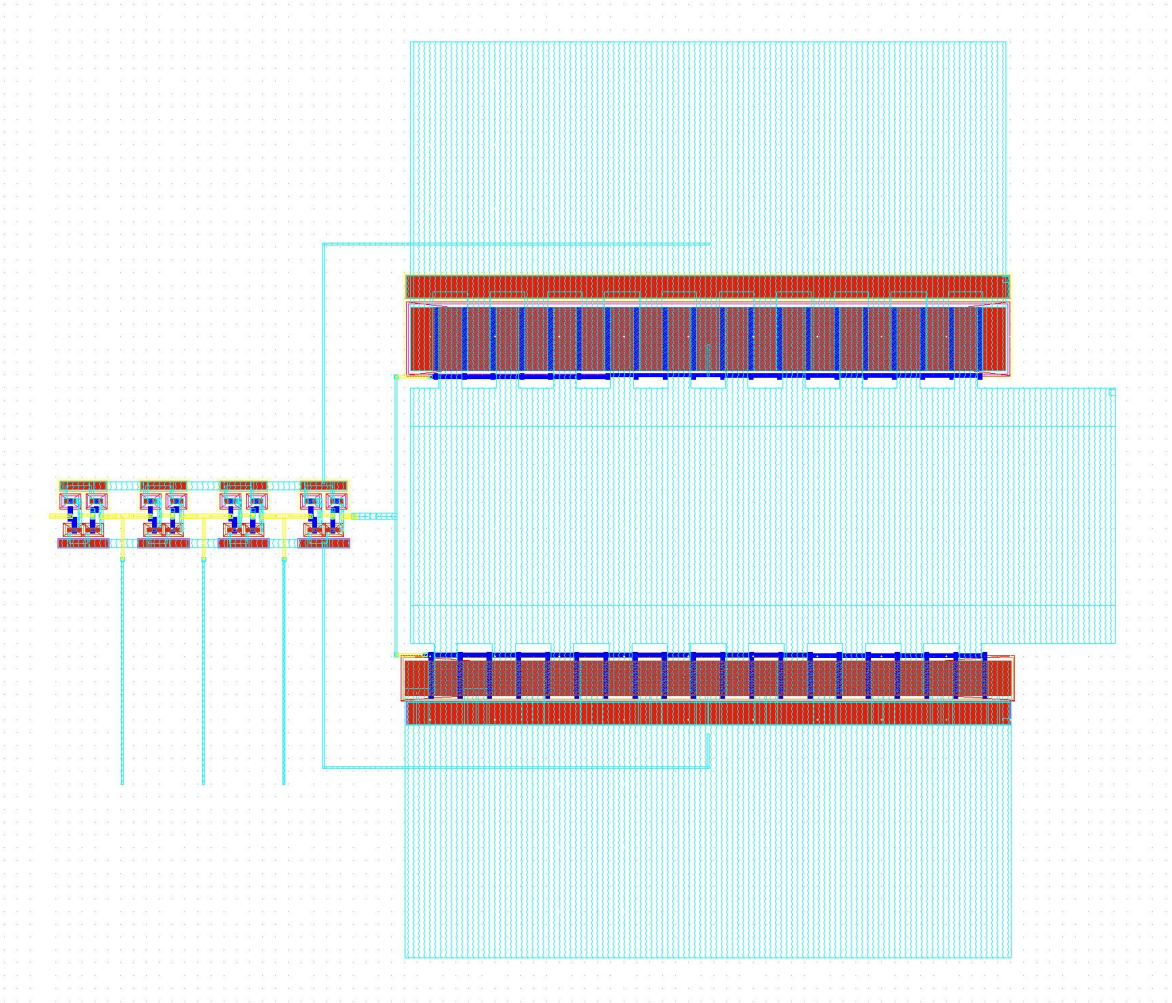


Figure 3.36. PREDRIVER layout, Cadence UMC130nm, IC

Figure 3.37. LINE DRIVER (NMOS Switches) layout, Cadence UMC130nm, IC

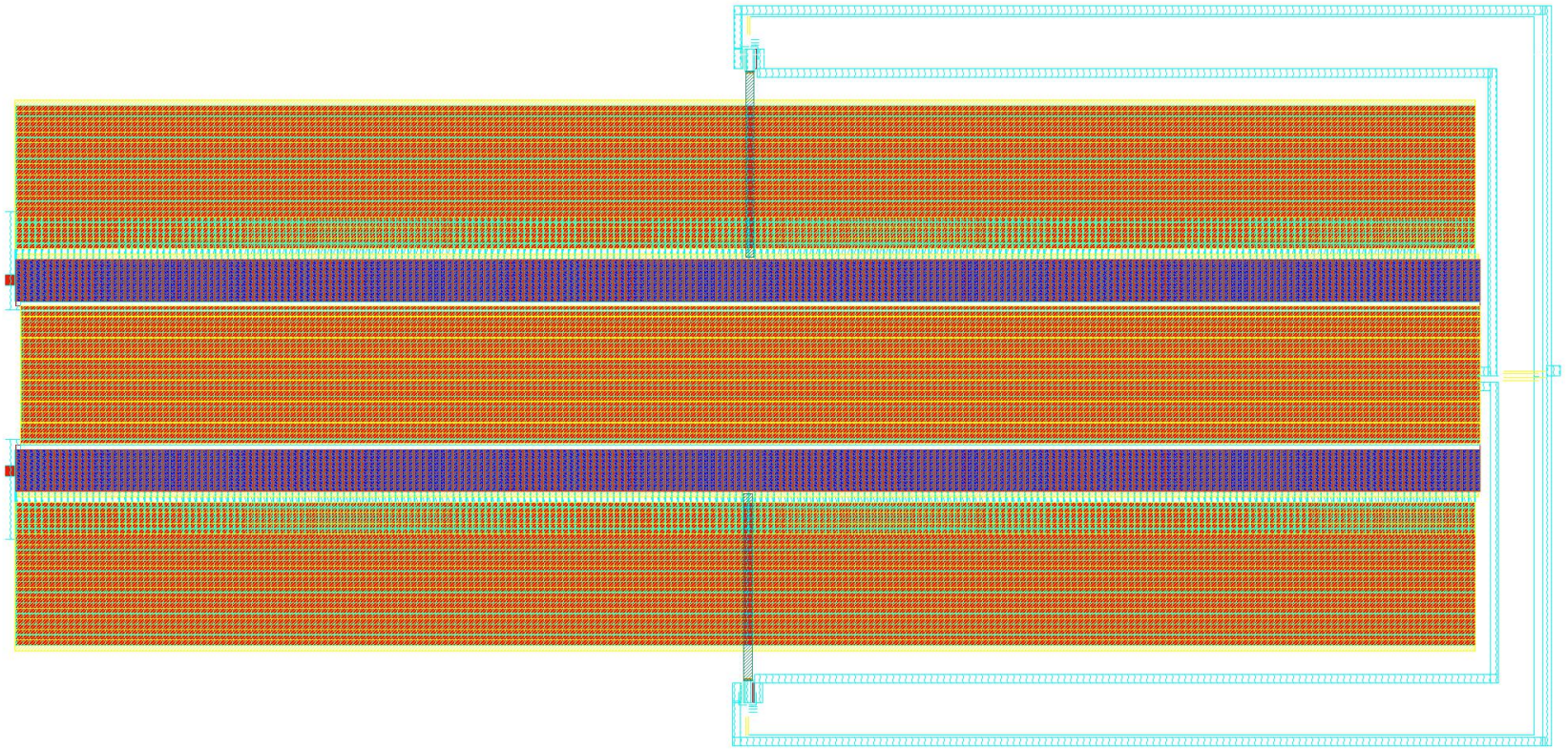


Figure 3.38. Transceiver layout, Cadence UMC130nm, IC

Proper layout considerations is necessary for high currents in the circuit [22]. To be able to accommodate as large currents as 380 mA, we decided to divide the task by connecting several NMOS transistors in parallel for the driving NMOS transistors. In order to keep each drain current to below 2mA, 228 transistors in parallel with max width of 100μm is designed. A μm metal conduction width per mA of current assumption is made. For that reason, drain and source widths are set to maximum of 1.7μm (below 2mA per transistor drain). To reduce or prevent unwanted drain to source breakdown under 9.6 V_{DS}, the gate width are chosen to be 10μm (this is a speculation at this point. Physical constraint process documentation is needed to fully comment on this issue, but for the meantime any precaution is helpful). Large widths also introduce large gate capacitances which is desirable to increase the driving slope.

Several bulk to ground ohmic contact are placed to reduce the resistance, latch-up effect as well as substrate voltage oscillations. This also prevents unwanted charge injection to the substrate.

Connection metal widths are also large, for the NMOS switch layout in Figure 3.37, the drain, source and ground metal connection have chosen to be around 350μm for 380 mA. Also the metal width in Figure 3.35 is 20 μm in order for the gate driving inverter to accommodate for 28 mA. All layouts have passed through DRC, LVS and PEX extraction without any errors.

Finally, the complete results for the simulation and experimental analysis of PCB and IC are summarized at Tables 3.1 and 3.2.

Table 3.1: PCB results

PCB	LTSpice	PCB Board
Transmission peak to peak voltage (Vp-p)	19.2	20
Transmission rise time (ns)	169	70
Transmission fall time (ns)	165	65

Table 3.1: PCB results (Cont)

PCB	LTSpice	PCB Board
Transmission over/under shoot (mV)	65	1200
Transmission 50% duty cycle rms current 5V source (mA)	362	580
Receiving rms current through 5V source (mA)	15	50
Receiving zero crossing typical (ns)	38	100
Receiving zero crossing max (ns)	286	400
Inter-transmission residual voltage (mV)	0	200

Table 3.2: IC results

IC	Schematic	Layout
Transmission peak to peak voltage (Vp-p)	21.8	21.4
Transmission rise time (ns)	137	108
Transmission fall time (ns)	136	108
Transmission over/under shoot (mV)	0	0
Transmission 50% duty cycle rms current 5V source (mA)	288	289
Transmission 50% duty cycle rms current 3.3V source (mA)	9.2	30
Receiving zero crossing typical (ns)	10	5
Receiving zero crossing max (ns)	282	297

4. CONCLUSION AND FUTURE WORKS

Towards the end of the project, we realized there are several points of improvement we can discuss. Upon the construction of the PCB board, having observed its successful operation and the very nature of it also having commercial and industrial side, made it imperative for us that there needs to be few more milestones before deploying the board to the field of operation in aircraft. For one, although it would further complicate the circuit, it is highly beneficial to have active filters at the input side of the receiver as opposed to passive filters we used here. This would block the unwanted frequencies without signal attenuation and highly increase the sensitivity range at the comparator inputs. At the moment resistor network designed for the receiver comparators are crafted as such to detect the terminal voltage above 0.86 Vp-p, and the attenuation present generates extra sensitive values for the resistors from Equations 2.9, 2.10, 2.11, 2.18 and 2.19. Only a few Ωs resistor error introduced from temperature and/or component mismatch, may alter the operating threshold values, therefore active filters are highly desirable. The transmitter topology we adopted worked without problems. However, a non-overlapping signal generation at the input of the transmitter with discrete elements would generate transmissions with less overshoots. So as a future work, these steps could be a good point of start for the second prototype of the PCB board which will be more industrially applicable.

We are convinced that the modeling, and exact operation of the isolation transformer has an overwhelming significance on the development of the board. This thesis dealt with a practical approach to the analog front end of bus transceiver and literature has been used to analyze and simulate the circuit. Without a good model for the transformer, none of the analysis and approximations done could be reliable.

Process in which we used to implement the IC only supported 3.3 V transistors. As a future work, a well compatible MOS could be drawn in Cadence to endure higher voltages in UMC130nm. Here we tried accommodating large currents by building large

drain and source metal widths for the available transistor models as well as large gates. Process specific physical documentation can be investigated for making higher voltage transistors with several different WELL layers (such as twin well in UM130nm library) as a new component model to the library perhaps.

We used two voltage sources for the IC part of the project 5V and 3.3V. It normally is more desired to operate the chip with a single supply. For that matter, a boos or buck (depending on which source we wanted to use) converter can be added to the package [23]. It is less complicated and unstable to use a buck converter to generate 3.3V from 5V supply as opposed to boost converter. However, depending on the manufacturing vendor, if 3.3V chip is required, 5V boost needs to be generated.

We finally conclude that this thesis analyzed the initiative project towards building a full industrially operational MIL-STD-1553 Analog front end Bus Transceiver which is built and used by handful of overseas companies where the details of implementation are company confidential.

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