A CONFIGURABLE INTERFACE FOR ANALOG SENSOR OUTPUTS

by

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ABSTRACT

A CONFIGURABLE INTERFACE FOR ANALOG SENSOR OUTPUTS

Reading out analog sensor outputs can be a challenging task at low frequencies because of the low frequency noise. To obtain a sensor signal clearly, special interface circuits are required. By using such circuits, analog signals are cleaned from offset, drift and 1/f noise. Besides, if the interface circuitry is configurable, it can be possible to interface to inputs at different frequency ranges.

At the interface block, analog sensor output signal is moved to a frequency band where low frequency noise effects are not dominant by using chopping modulation technique. The frequency-shifted signal is then filtered using various filter types. To remove the low frequency noise before moving the signal back to the original band, three types of filters used in the interface are Active RC, G_m-C, and Switched Capacitor filters.

The entire topology can be configured by a 5-bit digital to analog converter (DAC) called Biasing DAC (BDAC). This allows us to digitally change the biasing current of operational transconductance amplifiers (OTA). Therefore, OTA based amplifiers and filters can operate in different frequency ranges.

As conclusion, a configurable analog sensor interface has been designed. The design and layouts have been realized in Cadence Virtuoso using UMC 130nm techology.

ÖZET

ANALOG ALMAÇ ÇIKIŞLARI İÇİN YAPILANDIRILABİLİR BİR ARAYÜZ

Analog almaç çıkışlarını okumak, alçak frekanslardaki gürültü nedeniyle zor bir görev olabilmektedir. Almaç işaretini temiz bir sekilde elde edebilmek için özel arayüz devreleri gerekmektedir. Analog işaretler özel arayüz devrelerini kullanarak kayma(ofset), sürüklenme ve 1/f gürültüsünden arındırılmaktadır. Bunun yanında, arayüz devresi eger yapılandırılabilir ise, farklı frekanslarda çalışmak mümkün olmaktadır.

Arayüz bloğunda analog almaç çıkışındaki işaret, doğrama modulasyon teknigini kullanarak alçak frekans gürültü etkilerinin çok etkin olmadığı bir frekans bandına kaydırılır. Frekansı kaydırılmış işaret daha sonra farklı tipte suzgeçler ile süzülüp alçak frekans gürültülerinden temizlenerek tekrar asıl frekans bandına döndürülür. Tasarımda aktif RC, G_m-C ve anahtarlamalı kapasitörlü olmak uzere üç tip süzgeç kullanılmıştır.

Bütün topoloji, kutuplama sayısal analog dönüştürücüsü (BDAC) adı verilen 5-bitlik sayısal analog dönüştürücüleri (DAC) ile kontrol edilmektedir. Bu sayede işlevsel transiletkenlik yükselticilerinin (OTA) kutuplama akımları sayısal olarak kontrol edilebilmektedir. Bu sayede OTA tabanlı yükseltici ve süzgeçler farklı frekans bölgelerinde çalışabilmektedir.

Sonuç olarak, analog almaç çıkışları için yapılandırılabilir arayüz tasarımı yapılmıştır. Tasarım ve serimler UMC 130nm teknolojisinde Cadence Virtuoso programında gerçeklenmiştir.

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LIST OF SYMBOLS

V_{TH}	Threshold Voltage
V_{os}	Offset Voltage
V_n	Noise Voltage
f_{chop}	Chopping Frequency
C_{ox}	Gate Capacitance per Unit Area
ω	Angular Frequency
μ	Mobility of Carriers

LIST OF ACRONYMS/ABBREVIATIONS

AC	Alternating Current
ADC	Analog to Digital Converter
BDAC	Biasing Digital to Analog Converter
BJT	Bipolar Junction Transistor
CAB	Configurable Analog Block
CAD	Computer Aided Design
CLB	Configurable Logic Block
CMOS	Complementary Metal Oxide Semiconductor
CMFB	Common mode feedback
CMRR	Common Mode Rejection Ratio
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Complex Programmable Logic Device
CTAT	Complementary to Absolute Temperature
DC	Direct Current
DFF	D type Flip Flop
DNL	Differential Non-Linearity
FPAA	Field Programmable Analog Array
FPGA	Field Programmable Gate Array
INL	Integral Non-Linearity
LUT	Look Up Table
MEMS	Micro Electro Mechanical Systems
MPGA	Mask Programmable Gate Array
MOS	Metal Oxide Semiconductor
MUX	Multiplexer
NMOS	Negative-Channel Metal Oxide Semiconductor
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
PAL	Programmable Array Logic

PLD	Programmable Logic Device
PMOS	Positive-Channel Metal Oxide Semiconductor
SC	Switched Capacitor
PTAT	Proportional to Absolute Temperature
SNR	Signal to Noise Ratio
UMC	United Microelectronics Corporation
VLSI	Very Large Scale Integration

1. INTRODUCTION

In Electronic Circuit design, design objectives are not only determined by technical aspects, but also the economical aspects. Thus, market influence on electronic circuit design is at a level that can not be ignored. At this point, time becomes a major factor because the electronic circuit industry has a risk of designs becoming outdated. Designs and products must be able to respond to changes in consumer demands such as having additional features that were not taken into account during the initial design and manufacturing stages. Therefore, customizability and configurability of designs after production brings competitiveness in the market. This is also valid for sensors and sensor interfaces. In order to make a sensor interface more competitive in the market, it has to be designed as a configurable circuit.

Sensors and sensing devices have had a significant role in our lives in the last decades. By definition, a sensor means an electronic device that detects changes and events in its environment. This can be a temperature change [12], illumination change, change in the value of a resistance or a capacitance. Therefore, there is a wide range of sensor types. From measuring the temperature, biomedical signals [13], and seismic earthquake signals [14] to reading out blood sugar [15], sensors are used in almost every field in our lives. However, it is not enough to measure or sense but also important to transmit these singals to a circuit where they will be evaluated correctly. In order to perform this, sensors need interface circuits that read, evaluate, modulate, clean, and amplify the analog output of sensors. Interface circuits are also used for removing the noise at low frequencies. Especially 1/f noise and DC offset components at low frequencies are not welcome while sensing or measuring, because they can interfere into the real signal, deform it, and decrease the signal to noise ratio SNR resulting in false measurement or sensing [16]. Thus, interface circuits have significant role and responsibility to obtain true and precise measurement and sensing [17]. For a multipurpose interface circuit, configurability is vital. Designing a configurable interface circuit facilitates the measurement of continuous and discrete signals. Besides, designing internal blocks as fully differential input and output rejects more common mode signal and noise [18].

This thesis focuses on a configurable analog interface circuit which is based on the chopping modulation technique with various configurable filters. To understand how the entire topology works, it is important to analyze the functionality of each block in a detailed manner. However, before analyzing the whole system, historical background and literature will be presented. The next chapter summarizes the existing literature and background on different configurable circuits as well as analog interface topologies. In the following chapter, the design of each block has been shown and explained. In chapter 4, the simulation results are presented. Individual block performances as well as the performance of the entire system after connecting all blocks have been demonstrated in this chapter. In chapter 5, performance of the entire system is discussed in the light of simulation results. In the final chapter, conclusion will be drawn and future work in which how design could have been improved, and what sort of developments could have been made, will be discussed.

2. BACKGROUND

In this chapter, historical background of thesis and existing literature is covered. The first section is about configurable circuit systems such as FPGA, FPMA and CPLD. Properties of each system and their contribution to this thesis are explained in a detailed way. In the second section, some of the analog sensor interface systems in literature are mentioned briefly. Moreover, literature on chopping technique, tunable filters, and different topologies of these circuits are presented.

2.1. Configurable Circuit Systems

Configurable systems are mostly programmable circuits that consist of array combinations. The organization of these array combinations, their reprogrammability and configurability determine the type of that particular circuit system. Below, the most common types of configurable circuit systems are discussed.

2.1.1. Field Programmable Gate Array (FPGA)

FPGA is a complex logic device that has logic arrays organized in two dimensions and programmable switches. In Figure 2.1, on FPGA architecture has been illustrated where configurable logic blocks (CLB), I/O blocks, switch boxes, connection boxes, and interconnection resources can be seen. A logic function can be implemented in logic cells and configurable switches connect the cells via interconnection among themselves [2]. In order to configure a design, cells, switches, and interconnections of a particular region have to be specified, which is performed via a programming environment. FPGAs are programmed electrically similar to PLDs. Actually an FPGA is a PLD, but FPGA is much more advanced in terms of programmability and internal structure. In a conventional PLD, two level AND-OR logic with wide input AND gates are used during implementation. However, in FPGA, multi-level fan-in gates are used during implementation and this facilitates being compact rather than two level implementation [2].

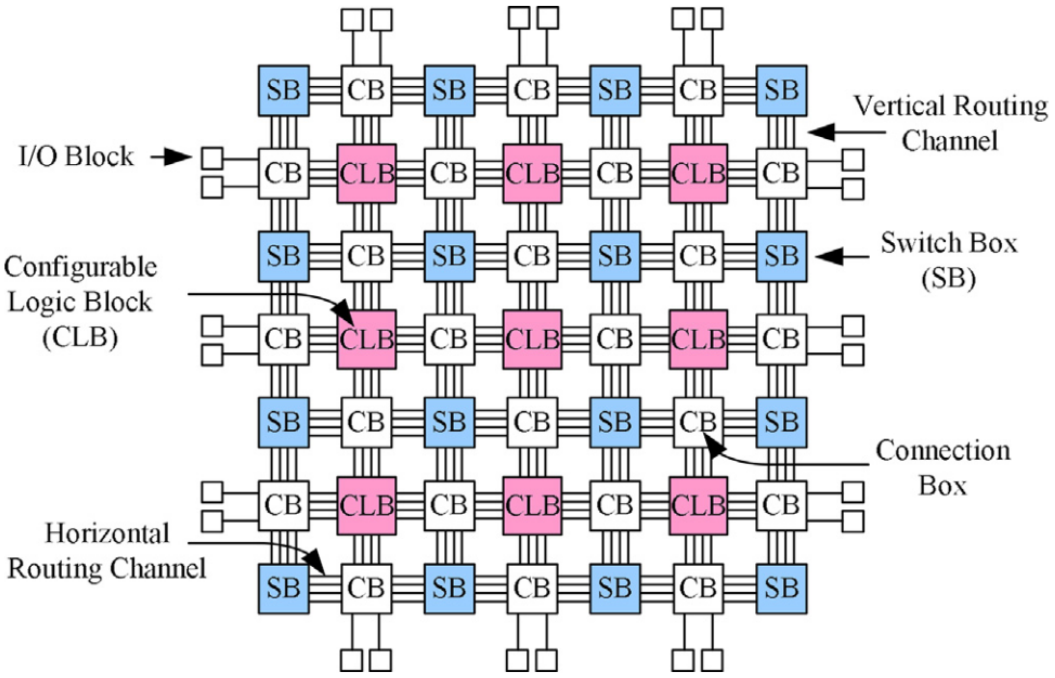
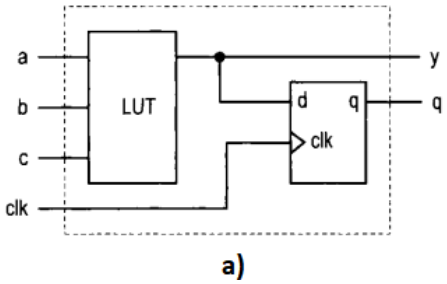


Figure 2.1. FPGA Architecture [1]

Logic cells mostly consist of small configurable combinational circuits with DFF. The most efficient and commonly used method to implement combinational and configurable circuits is using a look up table (LUT). A n-input LUT can be considered as 2^n-by-1 memory unit. In order to implement any n-input combinational function, LUTs can be used as memory units. In Figure 2.2, a three input LUT with its truth table has been shown.

The logic function stored in this particular LUT corresponds to $a \oplus b \oplus c$. The output of LUT can be used directly or via DFF. Most commercial FPGAs have 4 to 7 input LUTs. In addition to LUTs, there may be multiplexers (MUX), basic logic gates, and wide fan-in AND-OR structures in FPGAs [19].

The routing architecture of an FPGA puts together different wire segments that can be interconnected via switches. Length of wire segments is a significant factor that has a major effect to determine the complexity of FPGA routing architecture. Moreover, it is vital to use wire segments efficiently to avoid under-utilized logic blocks



a b c	y
0 0 0	0
0 0 1	1
0 1 0	1
0 1 1	0
1 0 0	1
1 0 1	0
1 1 0	0
1 1 1	1

b)

Figure 2.2. (a) Diagram (b) Truth table of look up table [2]

that leads to wasted area. Besides, routing with longer wire lengths increases the delay of the configured circuit. On the other hand, choosing shorter wire segments for long interconnections will need lots of switches in series connection that will lead to increased delay as well [19].

In FPGA, during the implementation of programmable switches, the three types of programmable switching technologies used commonly are SRAM, Antifuse, and EPROM. All these topologies require large area and result in large parasitic resistances and capacitances. In order to optimize the design and its performance, it is crucial to choose appropriate logic blocks with an efficient routing architecture and optimum number of switches. Each design requires its architecture and programming technology for only that particular design. Therefore, there is a not multi-purpose design, because design constraints restrict architectural choices [19].

2.1.2. Field Programmable Analog Array (FPAA)

Although digital circuits dominate the electronic market, analog circuits preserve significance as being an interface between digital processing and the real world in applications such as analog signal processing, motion control and reading sensor outputs. Since there is a time constraint and pressure in analog integrated design cycle, the most efficent and flexible method to achieve this is the FPAA. As a definition, FPAA is the combination of analog building blocks, a configurable routing network used for

connections between blocks and collection of memory elements used for configuring both the function and structure [3].

In FPAA implementation, there are several choices that affect the design such as the time domain type, voltage-current mode operation, CAB design, interconnection architecture, and programmable components. First, one must decide whether to work on discrete or continuous time domain. In discrete time, there are some techniques that are used such as switched capacitor, controlled duty cycle signal chopping and reconstruction, and switched current techniques. These techniques perform well with digital circuits and do not need very complex tuning circuitry for programmable components in VLSI applications. However, these techniques need band limited input signals so anti-aliasing and reconstruction filters have to be used. In continuous time, there is no requirement for bandlimited input signals. However, there might be more complex implementations to run circuit components in a large dynamic range [20]. Another important parameter that has to be considered during FPAA implementation is whether to use voltage or current mode signals. Voltage signals have high fan-out. On the other hand, choosing current as a signal parameter has some advantages like simpler implementation, high accuracy and high bandwith. Since low voltage applications in voltage mode implementation reduce the dynamic range, current mode signaling has become more preferable [20]. CAB design is another significant parameter because CAB is the basic cell unit in the FPAA chip. Besides, there are many factors that affect the CAB design such as semiconductor technology and area efficiency of routing sources. Fine grain FPAA chips need more routing resources and switches in the signal path than coarse grain ones. However, coarser grain FPAAs may implement fewer circuit types than the fine grain ones because coarser grain FPAA has larger blocks than the fine grain ones which are configured at a level closer to transistor level. The next major factor is architecture and implementation of FPAA. Interconnection architecture and how it is implemented have a huge impact on routability of the designed circuits and their performance. Analog circuits are affected by high fan-out, noise, and the number of switches on the signal path more than the digital ones. Regarding these problems and their solutions, hierarchical or full crossbar interconnection architectures can be used. There are different methods to implement programmable resistors and capacitors such

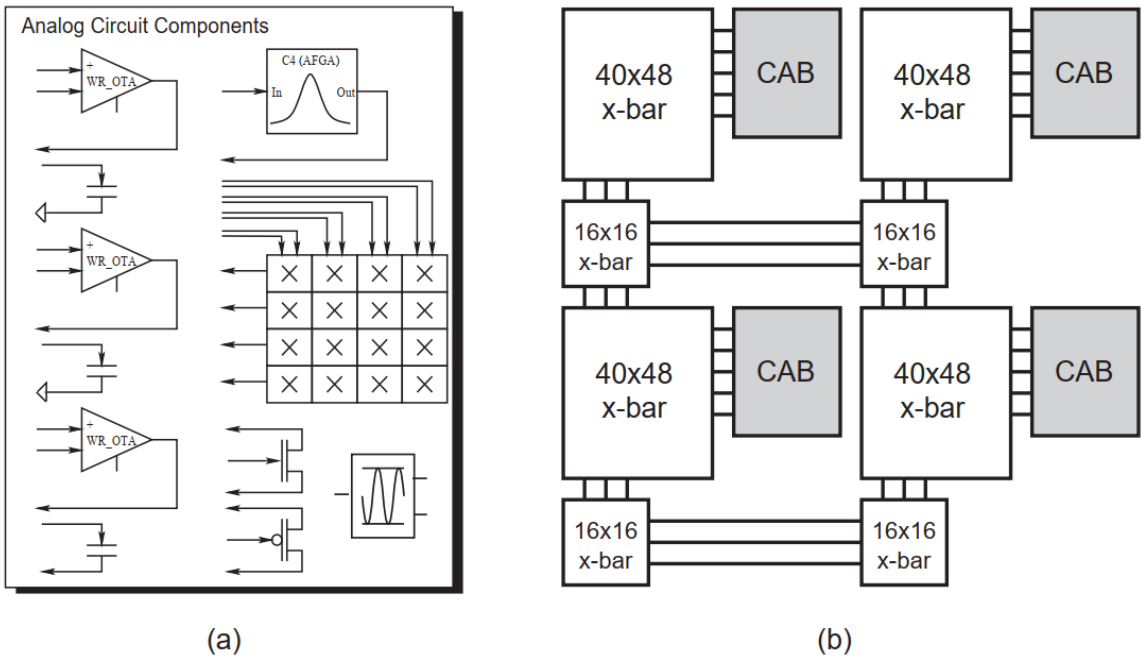


Figure 2.3. (a) CAB for a FPAA based on floating-gate devices, where each CAB contains a four-by-four matrix multiplier, three wide-range OTAs, three fixed-value capacitors, a capacitively coupled current conveyor (C^4), a signalby-signal multiplier, one PFET, and one NFET. (b) Overall block diagram for a large scale FPAA. The switching interconnects are fully connectable crossbar networks built using floating-gate transistors. [3]

as metal oxide transconductances and voltage controlled pass transistors. Capacitor arrays are also commonly used in SC circuits.

2.1.3. Complex Programmable Logic Device (CPLD)

A complex programmable logic device is (PLD) the combination of a larger number of PALs in a single chip. Their interconnection has been implemented by crosspoint switches. The difference between FPGA and CPLD has been demonstrated in Figure 2.4 [4]. CPLD architecture consists of input/output blocks, function blocks, and an interconnection matrix. According to the manufacturer's desire CPLDs can have programmable units such as EPROM, EEPROM, and Flash EPROM cells.

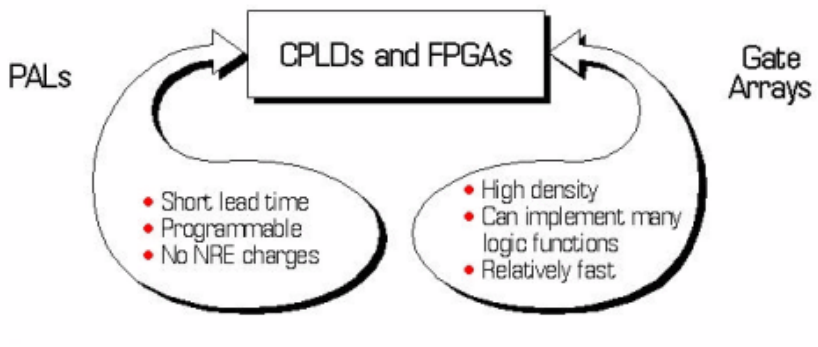


Figure 2.4. Comparison of CPLD and FPGA [4]

In the function block, the AND plane accepts inputs from all other blocks, then they are ORed by using fixed OR gates. Large multiplexers select minterms. Like

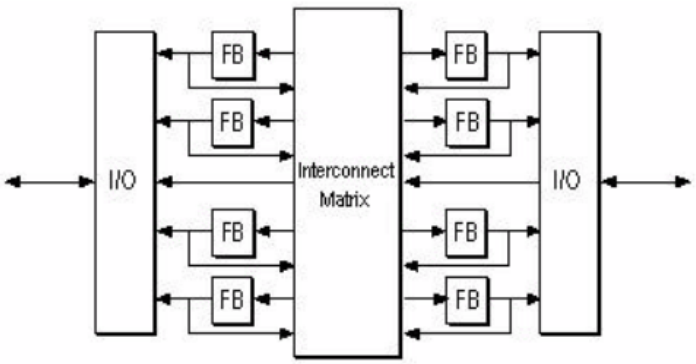


Figure 2.5. Architecture of CPLD [4]

FPGA LUT structure, outputs of MUX can be sent directly or stored into DFF. This function block mostly uses the same architecture with existing PALs. The aim of the I/O block is to transmit the right signal to the right pins of the CPLD device by maintaining current and voltage levels. Clocked inputs are transmitted by using DFFs, so the signals are sent to the output without considerable delay. This is valid for the inputs, thus there is not much delay before the DFF, otherwise the need for device hold time increases. A very large switch matrix resolves the interconnection issue by permitting the signals from all over the CPLD to particular ends. Since all internal function blocks are not connected to all other function blocks, the interconnection matrix has adequate flexibility to permit all combinations of connections [4].

2.2. Analog Sensor Interface Systems

Before explaining and discussing analog sensor interfaces, micro electro mechanical systems or microsystem technology will be mentioned briefly. MEMS are miniature and multifunctional systems that include sensors, actuators, and their interface systems. From semiconductor devices to analog and digital integrated circuits, MEMS are used in a very wide range of topics. Analog sensor interfaces perform with MEMS sensor outputs. These outputs can be biological signal data, accelerometer data, seismic sensor data, shock sensor data, ultrasonic sensor data, or acoustic sensor data. Reading different types of sensors up to 15kHz frequency effectively, are in the scope of this thesis. Besides, reading out these sensor outputs, cleaning out non-idealities such as noise, offset, and drift is one of the most significant achievements done by analog sensor interfaces.

In CMOS technology, the offset voltage at the input of a differential pair can be as high as 10mV due to variations during manufacturing or uncertainty [21]. In MOS devices, V_{TH} is a function of doping amount in the channel and gates. Since these parameters may have different values depending on the device, there might be mismatch in the V_{TH} [5]. Also, there might be micron level mismatch during fabrication of MOS transistors that result in the offset. Enlarging device size might be a solution but that costs too much chip area [5].

The main reason of the 1/f noise is the defects in the gate oxide and silicon substrate. Thus, 1/f noise has a dependence on the purity of oxide-silicon interface. In CMOS technology, 1/f noise is the dominant noise factor at low frequencies and it is modeled as in the equation below.

$$V_n^2 = \frac{K}{W.L.C_{ox}.f} \tag{2.1}$$

In the equation, K is process parameter, W is the width, L is the length of the MOS transistor, C_{ox} is the capacitance per unit area, and f is the frequency. 1/f noise performance of PMOS is better than NMOS in most technologies [5].

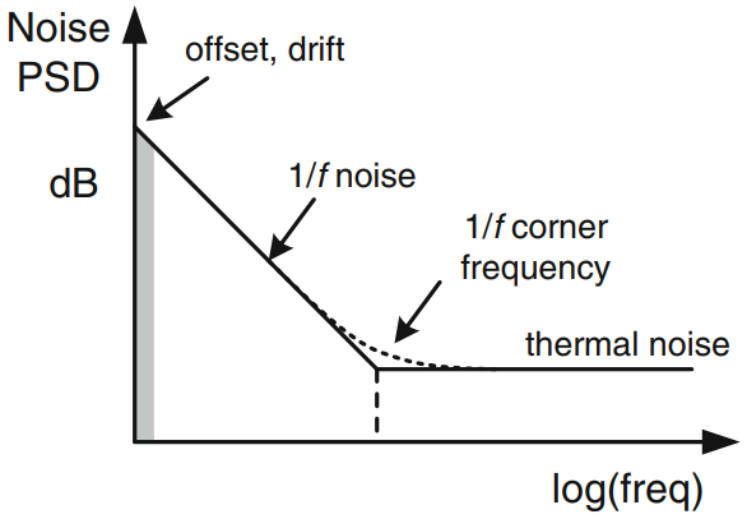


Figure 2.6. Low frequency noise spectrum of CMOS and 1/f noise [5]

Drift is caused by the cross-sensitivity of some error sources to temperature or time. Keeping drift low is a significant condition for high precision temperature measurement because the drift of overall circuitry can not be detected, if it is not detected on component level. There are two main types of drift: gain drift and offset drift. In order to decrease the drift level, the errors in gain and offset have to be eliminated.

As a conclusion, CMOS low frequency non-idealities are mainly caused by 1/f noise, offset, and drift as in Figure 2.6. In order to eliminate these errors, there are some precision techniques that are applied to the output of sensors that are autozeroing, corelated double sampling, dynamic element matching, and chopping. In the next subsections, autozeroing and chopping technique will be discussed.

2.2.1. Auto-Zeroing

Autozeroing is a sampling technique used in discrete time domain. In autozeroing, the offset of the amplifier is sampled in one clock phase, then it is subtracted from the input signal in the other clock phase. It has three types such as input offset storage, output offset storage and closed-loop offset cancellation using an auxiliary amplifier. In

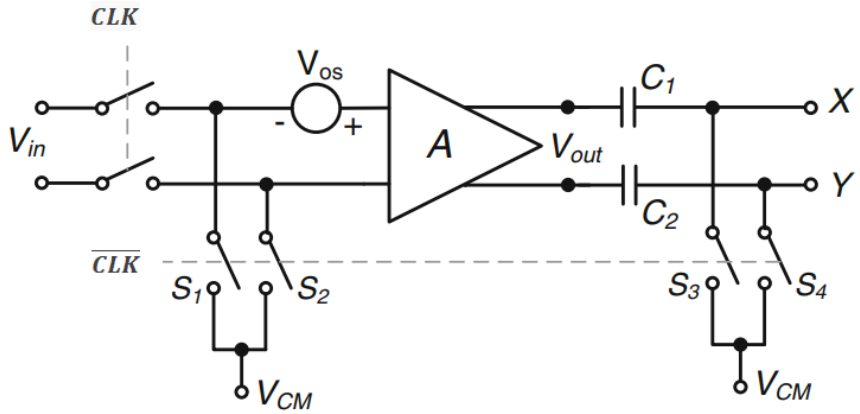


Figure 2.7. Output offset storage autozeroing circuit diagram [5]

Figure 2.7, output offset storage autozeroing circuit diagram has been shown. During autozeroing phase CLK is 1 and $V_{out} = A.V_{os}$ is stored in C_1 and C_2. When CLK is 0, the circuit is at amplification phase where V_{in} and V_{os} are amplified and stored in C_1 and C_2. However, since V_{os} is already stored in C_1 and C_2, V_{os} is eliminated and does not appear in V_X and V_Y [5]. The previous technique limits the gain, so for higher gain another topology with input offset storage autozeroing is shown in Figure 2.8. When CLK is 1 which is the autozeroing phase, the input of the amplifier is short circuited by the switches S_1 and S_2 resulting in unity gain. V_{os} is produced at X and Y nodes of the amplifier to be kept on C_1 and C_2. Here the most important point is to match switches S_1 and S_2 in order to make input referred offset V_{os}/A [5]. Another approach is closed-loop offset cancellation with an auxiliary amplifier. The main difference of this topology is the isolation the capacitors C_1 and C_2 where offset is stored, from the signal path as illustrated in Figure 2.9. When CLK is 1 which is autozeroing phase,

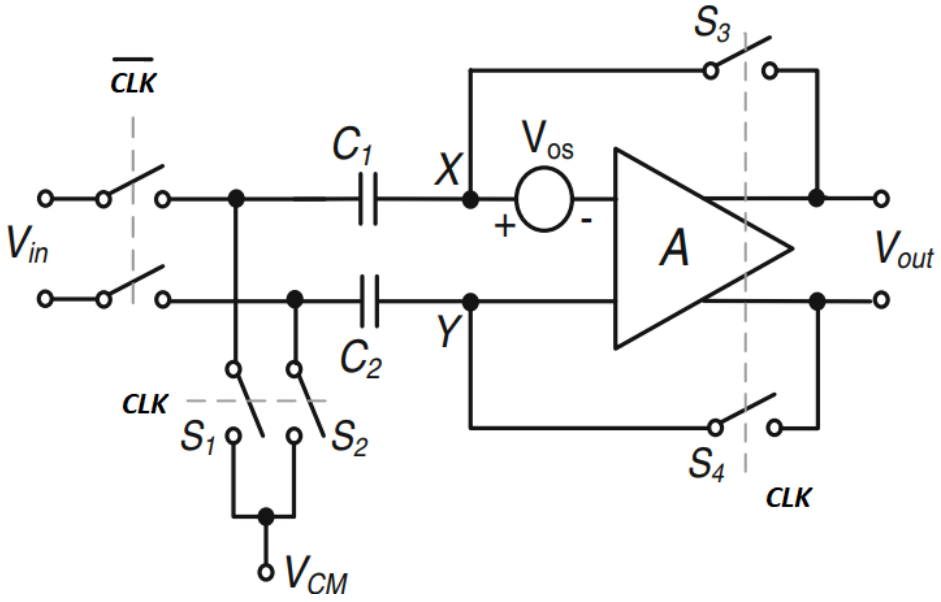


Figure 2.8. Input offset storage autozeroing circuit diagram [5]

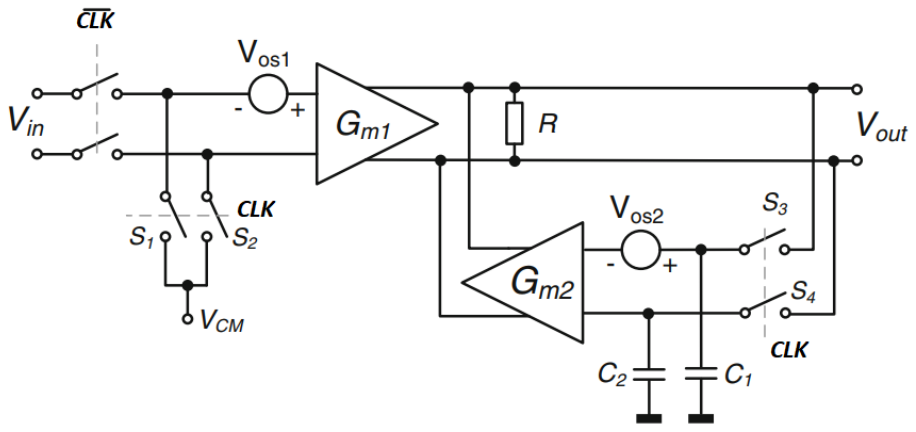


Figure 2.9. Closed-loop offset cancellation with an auxiliary amplifier circuit diagram [5]

inputs of Gm_1 are short circuited. Then $V_{out,AZ}$ becomes:

$$V_{out,AZ} = \frac{Gm_1.R.V_{os1} + Gm_2.R.V_{os2}}{1 + Gm_2.R} \tag{2.2}$$

When S_3 and S_4 switches turn on, $V_{out,AZ}$ is stored on C_1 and C_2. The charge injection between S_3 and S_4 switches increase the offset of Gm_2. In order to eliminate this issue, Gm_2 is chosen 50 times smaller than Gm_1. Since these topologies cannot produce a continuous time output, ping-pong topology that is combination of chopping and autozeroing, is used [5].

To conclude, three offset cancellation techniques with autozeroing are introduced and each of them subtracts the offset before the next sampling cycle. These techniques are useful to eliminate 1/f noise and drift as well because low frequency noise and DC offset can not be separated from each other [5]. It has to be noted that in the frequencies lower than the sampling frequency, autozeroing might affect the noise performance of the amplifier [17].

2.2.2. Chopping Technique

Chopping is a modulation and precision technique introduced about 70 years ago with the vacuum tube amplifiers. It is used to obtain high precision signals from the analog sensor outputs. Unlike autozeroing chopping is a continuous time precision technique and does not cause signal folding.

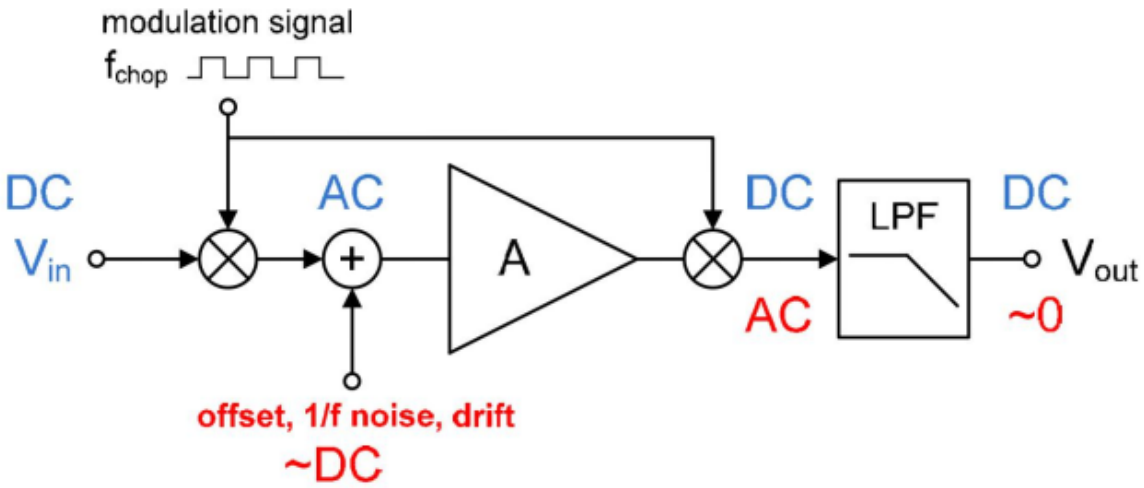


Figure 2.10. General scheme of chopping topology [5]

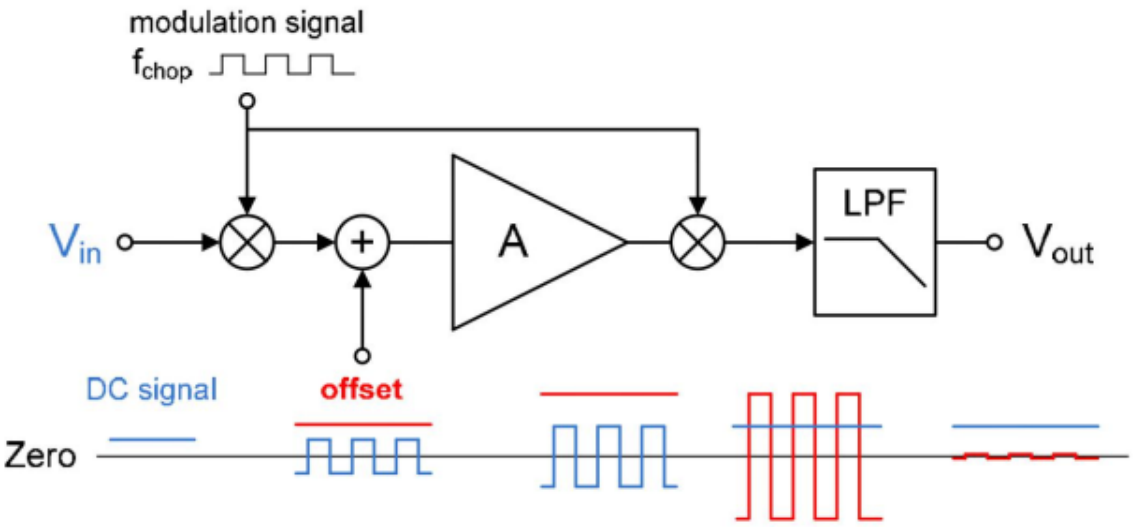


Figure 2.11. Chopping in time domain [5]

As indicated in Figure 2.11 V_{in} is first chopped at f_{chop} and converted to a square wave. Then, the modulated signal is amplified with its own offset. The amplified signal is demodulated to DC the by second chopper. Meanwhile, the DC offset is modulated to odd harmonics of f_{chop}. Low frequency non-idealities such as offset, 1/f noise, and drift are left at the odd harmonics of f_{chop}. After demodulation, the signal is filtered by a low-pass filter to be removed from low frequency artifacts. Thus, input signal is seperated from non-idealities [5].

Frequency domain chopping scheme is indicated in Figure 2.12. To remove 1/f noise completely f_{chop} has to be much larger than 1/f noise corner frequency. At the beginning V_{in} is modulated to f_{chop}. Noise and offset are superposed onto the modulated signal. Amplification and demodulation sends V_{in} to DC while V_{os} and V_n are modulated to odd harmonics of f_{chop}. They appear as chopping ripple as in Figure 2.12. Amount of ripple can be reduced by increasing f_{chop}. However, for optimum chopping f_{chop} has to be 3dB point of the amplifier bandwith [5].

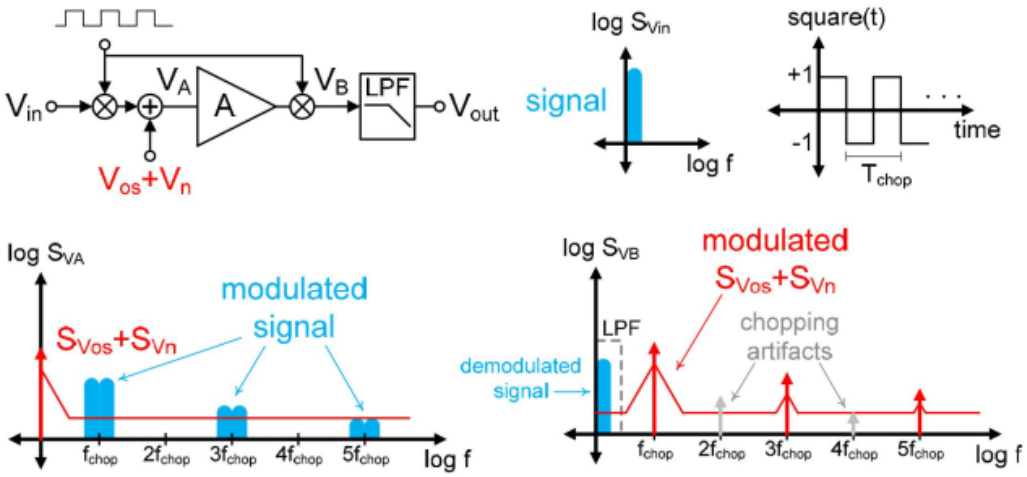


Figure 2.12. Chopping in frequency domain [5]

3. DESIGN AND LAYOUT OF BLOCKS

In this chapter, the circuit design and layout of each block in the thesis will be presented. Design properties and explanations are provided with references. The entire design has been implemented in UMC 130nm technology using Cadence Virtuoso CAD tool.

3.1. Biasing Circuit

The biasing circuit is used to bias OTAs and OPAMPs via voltage and current. All biasing voltage or current levels are produced internally using a digital input value, making the whole design self biased. The biasing circuitry of the interface system includes a bandgap reference circuit that produces the biasing voltage and reference current of BDACs, OTAs, and OPAMPs. Bandgap reference circuit has CTAT and PTAT temperature independent voltage sources that will be discussed in the next subsection. Biasing scheme of the overall design is shown in Figure 3.1.

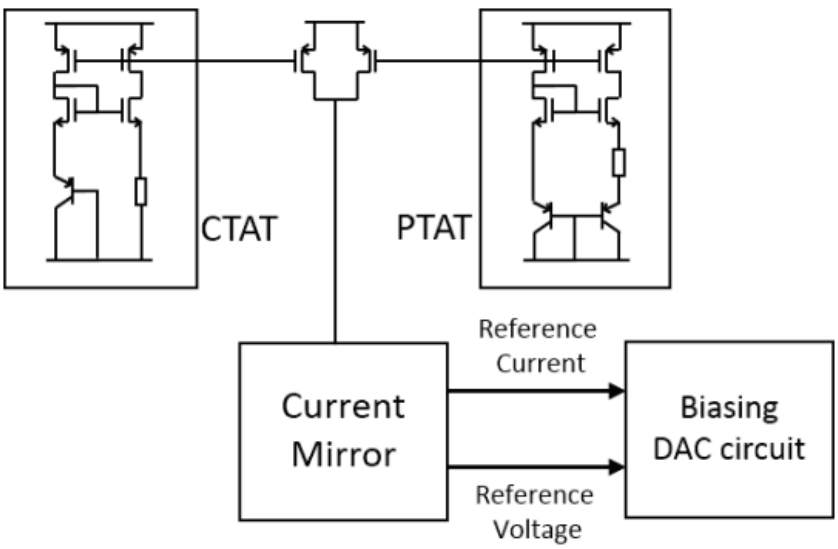


Figure 3.1. Biasing scheme of overall design [6]

3.1.1. CTAT and PTAT Circuits

Complementary to absolute temperature (CTAT) and proportional to absolute temperature (PTAT) circuits are voltage references that work together to generate a stable reference independent of temperature variations. As the temperature increases, the CTAT circuit decreases the voltage or current output level while the PTAT circuit increases the voltage or current output level. The first step in such design is the idenfication of a voltage level that increases with the temperature and another voltage level that decreases with the temperature. Next, the smallest absolute value of the slope of change determined. The PTAT slope is multiplied with a coefficent K in order to equate the absolute values of the slopes. The aim is to obtain a constant voltage value independent of the temperature. Original and multiplied versions of PTAT are illustrated in Figure 3.2 [7] .

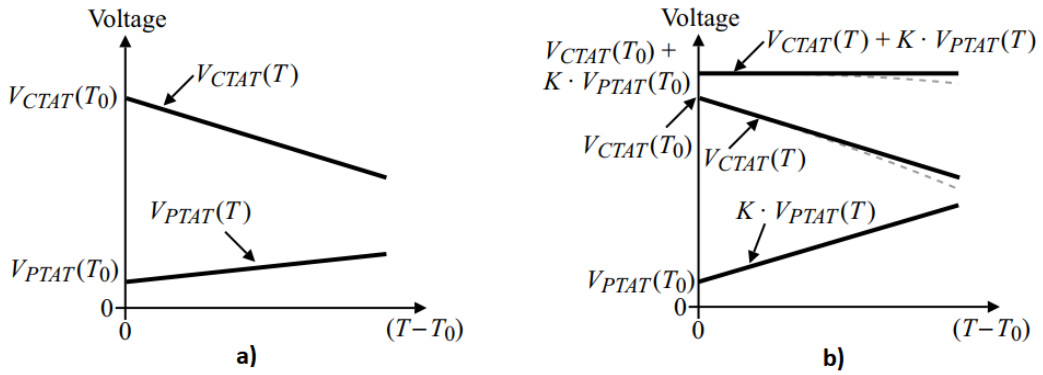


Figure 3.2. (a) Voltage variations with respect to temperature change, (b) Multiplication of slope of PTAT with K to equate absolute value of the slopes (Right) [7]

The proposed interface system has a CTAT, a PTAT, and a pair of transistors that add the currents obtained from CTAT and PTAT before they are mirrored to the bandgap reference part as depicted in Figure 3.3. In CTAT, the current on the BJT transistor varies complementary with respect to the temperature. In the PTAT part, there are two BJT transistors where the one on the right side is 5 times larger than the left one. V_{BE} voltages of these two BJT transistors vary directly proportional to

the temperature. The voltage on the resistance is generated by the difference between base-emitter voltages of these two transistors as shown in equation 3.1 [7]. The currents flowing through CTAT and PTAT are mirrored via a pair of PMOS transistors between these blocks. The summation current then flows into a cascode current mirror to generate the reference and biasing voltages V_R and V_B.

$$V_{Res} = V_{EB2} - V_{EB1} = V_t.ln(\frac{I_2.A_{E1}}{I_1.A_{E2}}) \tag{3.1}$$

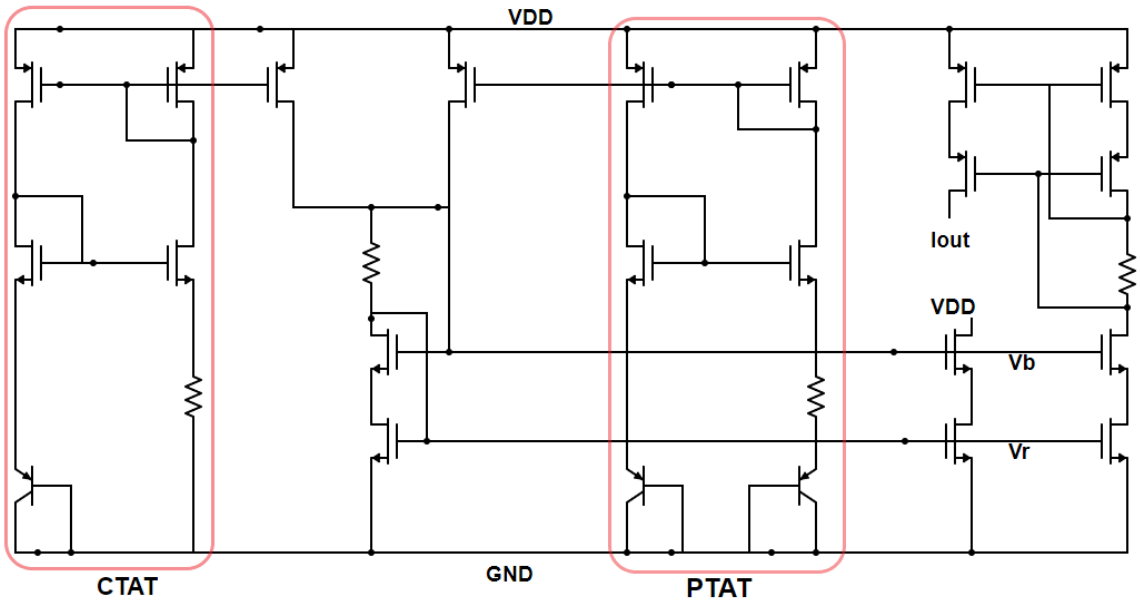


Figure 3.3. Bandgap reference circuit with CTAT and PTAT circuits

3.1.2. Bandgap Reference Circuit

As a definition, bandgap reference circuit is a circuit that provides current and voltage independent of both temperature and power supply [7]. The bandgap reference circuit in the proposed design is not completely independent from the supply voltage. The name of the topology comes from the fact that the circuit supplies constant V_R, V_B, and I_{bias} independent from the temperature. The current obtained of CTAT and PTAT are mirrored to generate reference voltages and currents. The bandgap reference circuit in Figure 3.3 is able to generate two currents and four voltage values independent from temperature, but since the design requires only one current and two voltage values, the others are not used. At the I_{out} port, the biasing current is generated with 1μA value. At the V_R and V_B nodes, voltage values of 623mV and 903mV are generated respectively.

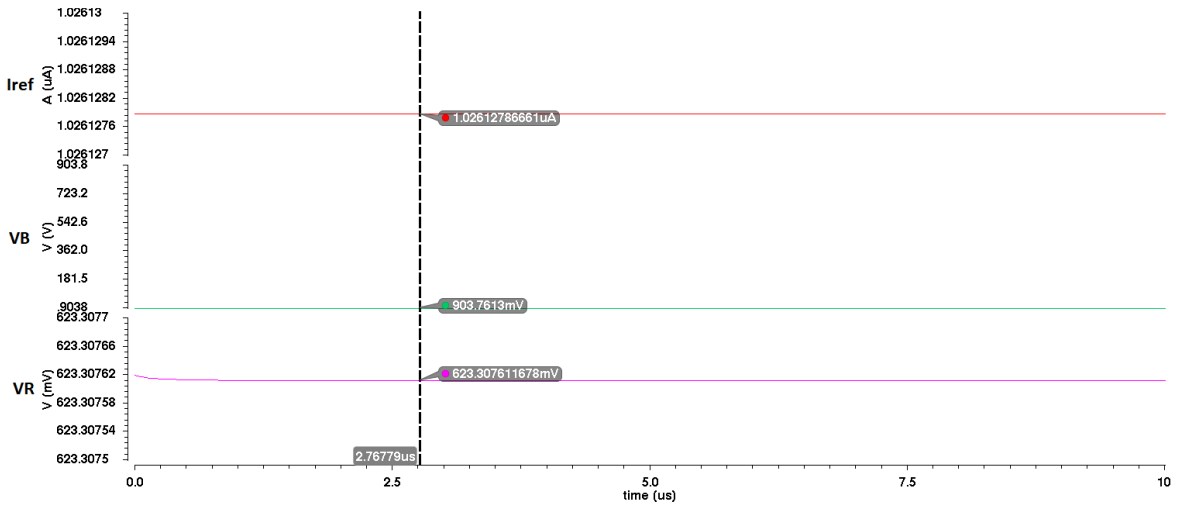


Figure 3.4. V_R, V_B, and I_{bias} values of bandgap reference circuit

In Figure 3.5, the variation of V_R, V_B, and I_{bias} values with respect to temperature changes are shown. It can be easily seen from this figure that all current and voltage values are reasonably independent from temperature changes.

After connecting the bandgap reference circuit to BDAC, although the generated values are not changing, some spikes may be observed as depicted in Figure 3.6 because

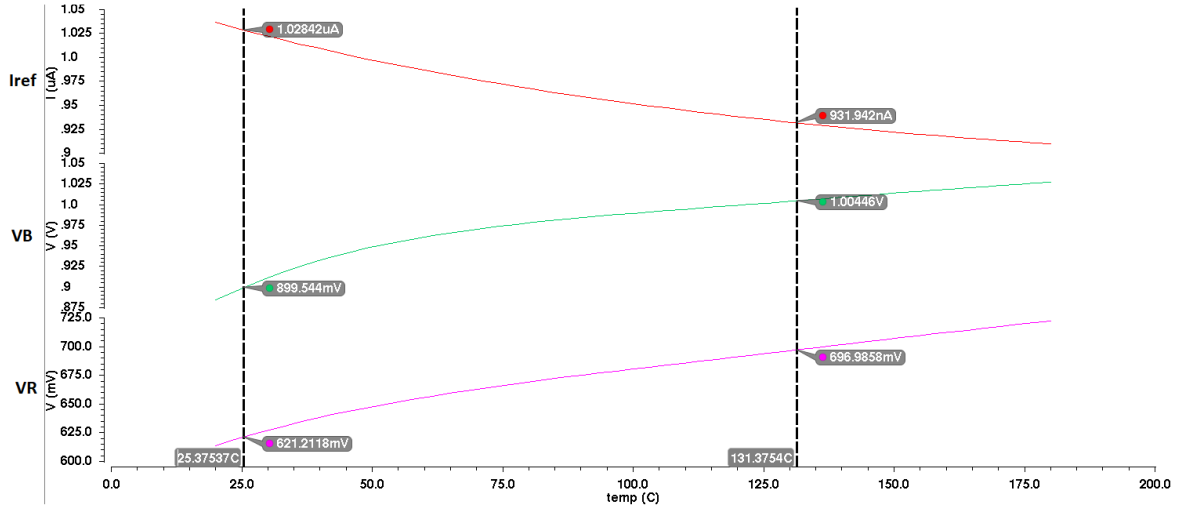


Figure 3.5. V_R, V_B, and I_{bias} values of bandgap reference circuit with respect to temperature variation

of switching. Spikes at the output of the bandgap reference circuit can be partially removed by connecting a source follower transistor as a buffer before the BDAC. The load capacitor of source follower is 1pF.

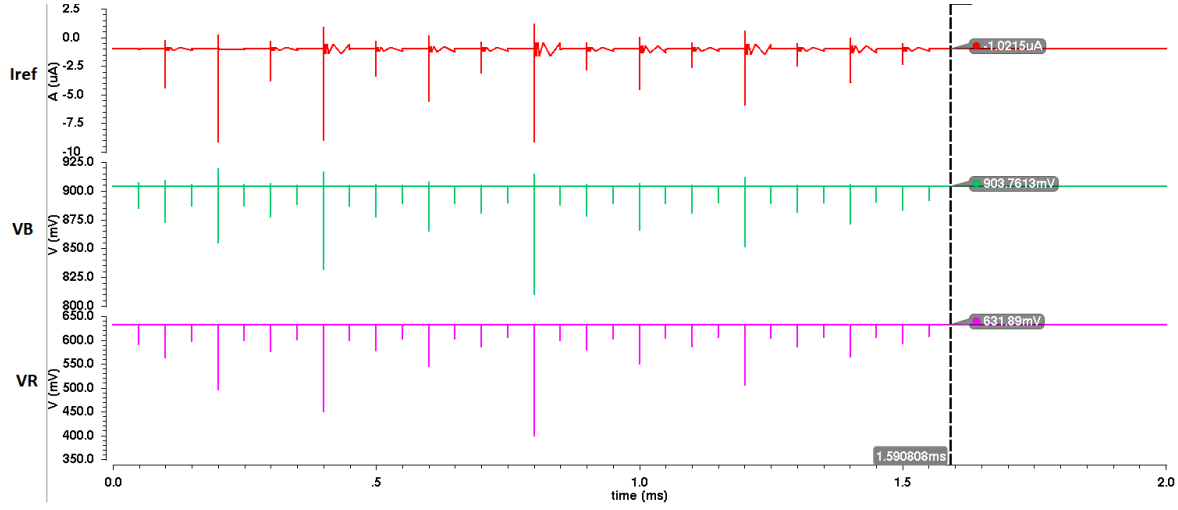


Figure 3.6. V_R, V_B, and I_{bias} values of bandgap reference circuit after connecting to BDAC

The temperature analysis has been applied again after connecting the bandgap reference circuit to BDAC. The result is not surprising and very similar to the previous

situation. As indicated in Figure 3.7, it can be stated that bandgap reference circuit is reasonably independent of temperature variations. To show that bandgap reference circuit is also independent of supply voltage, transfer function analysis (XF) has been done. Power supply rejection ratio is shown in Figure 3.8 as 20dB.

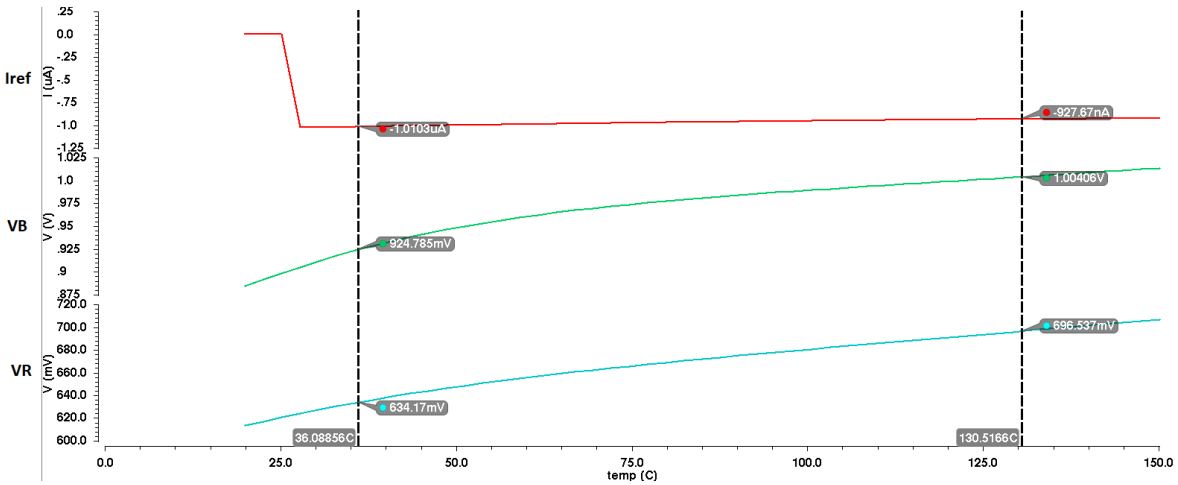


Figure 3.7. V_R, V_B, and I_{bias} values of Bandgap Reference Circuit after connecting to BDAC with respect to temperature variation

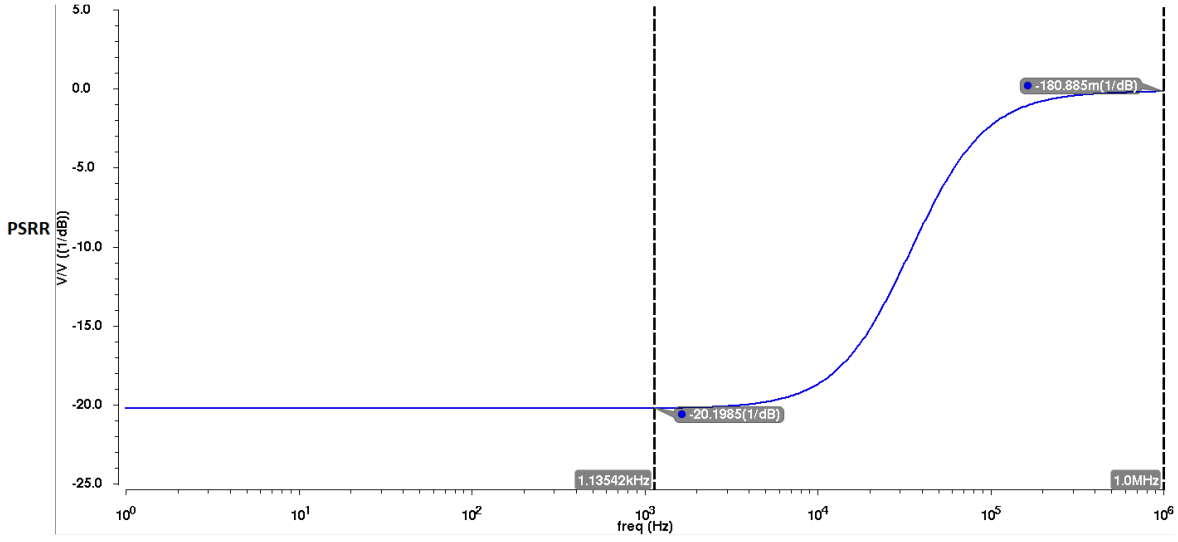


Figure 3.8. Power supply rejection ratio of bandgap reference circuit

3.2. Biasing DAC

Biasing digital to analog converter (BDAC) is a current mirror based topology, which uses current steering technique to bias OTAs and OPAMPs in the design. Current steering topology is preferred because it has less dynamic errors that stem from switching [22]. The since proposed BDAC is only used for biasing, voltage level at the output of DAC does not change too much. Therefore, the proposed design does not require fast operation. Differential non-linearity error (DNL) is the deviation of the step size of a real data converter from the ideal width of the bins Δ. Assuming that X_k is the transition point between successive codes k $-$ 1 and k, then the width of the bin k is $\Delta_r(k) = X_{k+1}$ - X_k [23]. Then, DNL is calculated using the formula in equation 3.2.

$$DNL(k) = \frac{\Delta(k) - \Delta}{\Delta} \tag{3.2}$$

DNL values vary between 0.01 and 0.03 LSB. Integral non-linearity (INL) is a measure of the deviation of the transfer function from the end-point fit line. INL is also used for estimating harmonic distortion. G is the gain error which is defined as the error on the straight line interpolating the transfer curve [23]. INL is calculated using formula in equation 3.3 and is less than +/-1 LSB.

$$INL(k) = (1 + G) \sum_{i=1}^{k} DNL(i) \tag{3.3}$$

DNL and INL graphic were drawn in cadence using viva calculator. Since inputs are given as transient signals and BDAC output current I_{out} is obtained in time domain, DNL and INL graphics are obtained as least significant bit (LSB) versus time. Figures 3.9 and 3.10 depict DNL and INL graphics respectively.

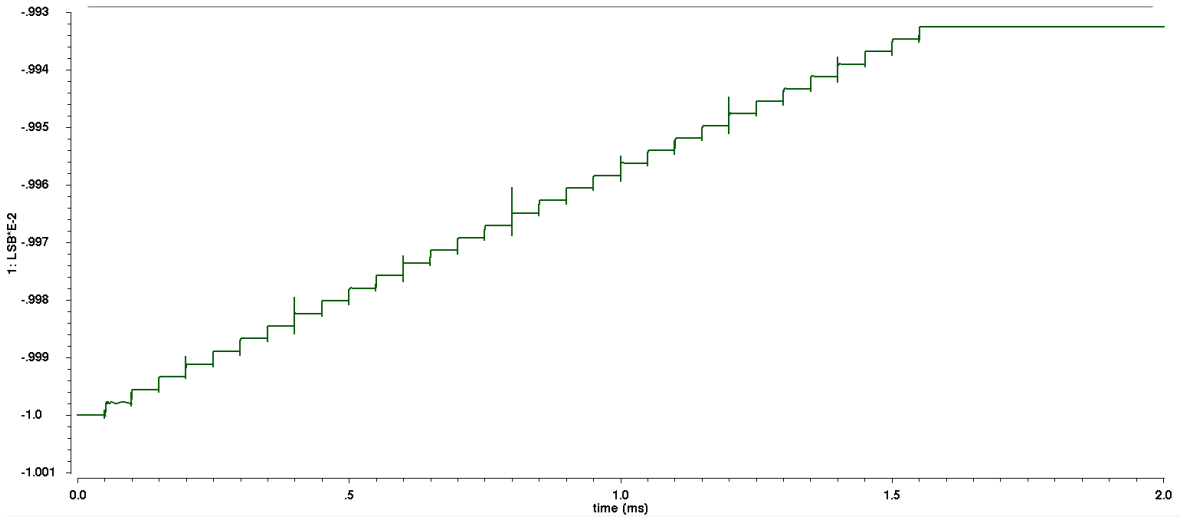


Figure 3.9. DNL chararacteristic of BDAC

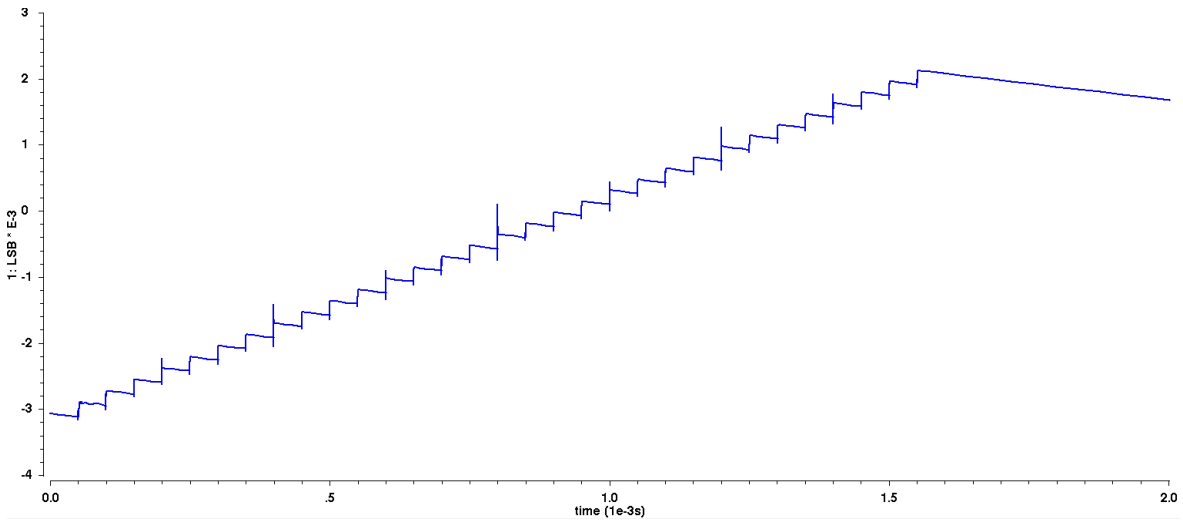


Figure 3.10. INL characteristic of BDAC

The input current obtained from the bandgap reference circuit is 1uA, and this current is multiplied by a value between 0 and 31 using 31 parallel connected current mirrors switched on or off by a 5-bit digital control word. A simple schematic of the BDAC topology used is illustrated in Figure 3.11. Transmission gate based switches are turned on or off by a digital word to set the output current to a desired value. Each current cell is a pair of series NMOS transistors as depicted in Figure 3.12. . The total output current is the sum of the currents carried by the mirroring current cells that

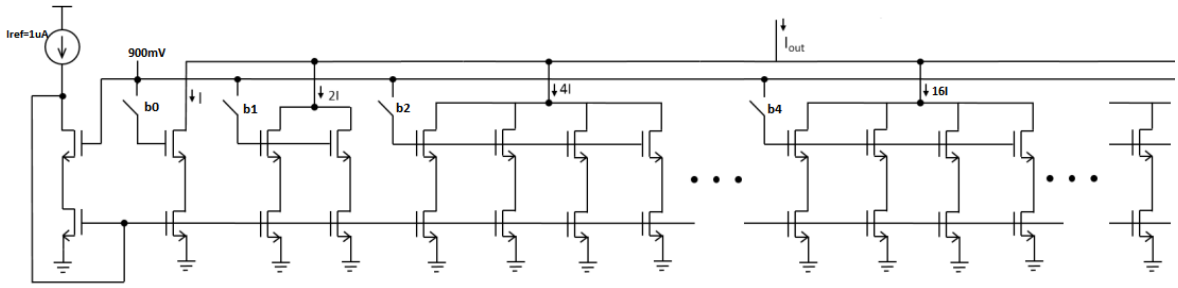


Figure 3.11. 5 bit current mirror based biasing DAC [8]

are turned on. Number of turned on current cells is determined by the digital input word n resulting in the output current $I_{out} = n.I_{ref}$. The value of I_{out} varies from 0 to 31μA since BDAC has 5-bit input. The 5-bit digital input is connected to BDAC

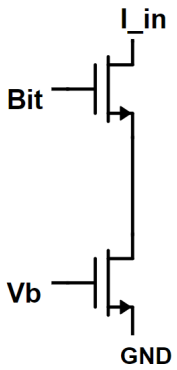


Figure 3.12. Currentcell of BDAC

via 5 transmission gate switches. In Figure 3.13, 5-bit digital input combinations are shown. This 5-bit pattern source was also used in the test bench of the BDAC circuit. Each pattern generates square waves that correspond to different bit combinations as shown in Figure 3.14. Thus, 32 different current values including 0 can be generated. Figure 3.14 displays the output current I_{out} in detail. Current values vary from 0 to 31μA and each bit combination corresponds to a current value. The error at the I_{out} can be observed from Figure 3.15.

```
B0: 01010101010101010101010101010101
B1: 00110011001100110011001100110011
B2: 00001111000011110000111100001111
B3: 00000000111111110000000011111111
B4: 00000000000000001111111111111111
```

Figure 3.13. Bit combinations of bit sources at the input of BDAC

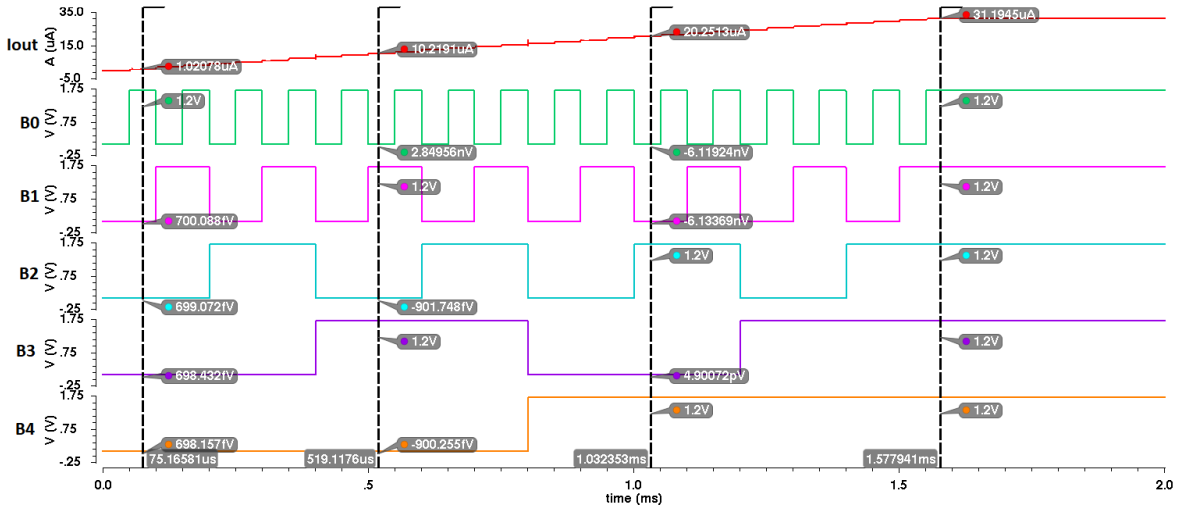


Figure 3.14. 5 bit digital input and I_{out} of BDAC

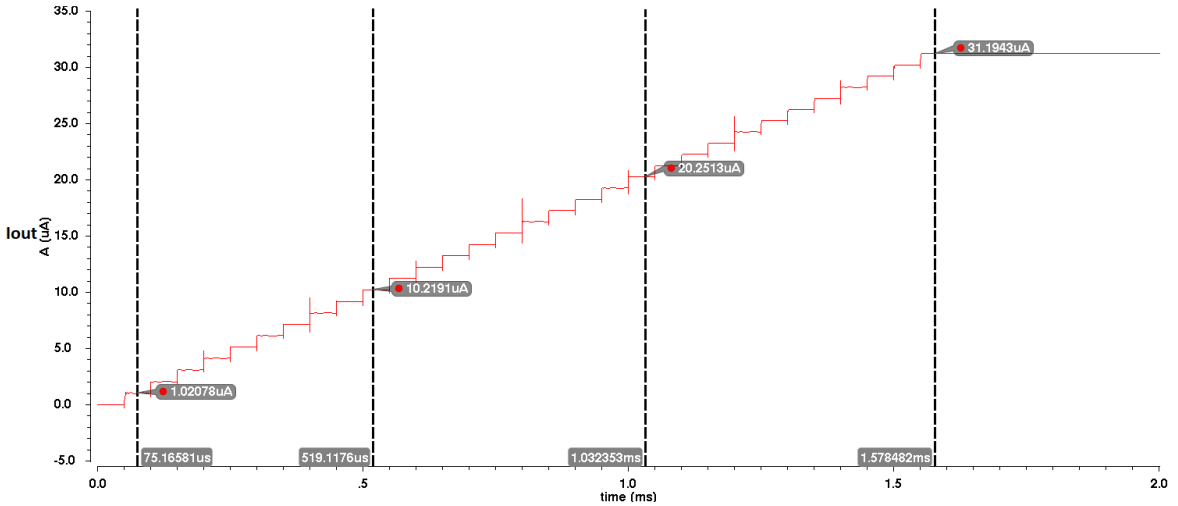


Figure 3.15. Output current I_{out} of BDAC

3.3. Chopping Amplifier

In this section, chopping amplifer design will be presented. All schematics from the design have been provided as figures. How chopping works and why it was chosen have been already discussed in Chapter 2. Therefore, only the design details will be described in this section. The type of amplifier, common-mode feedback, and the output stage will also be discussed.

3.3.1. Chopper

Chopper is a switching block that has four switches driven by clock and complementary clock at the chopping frequency the f_{chop}. In CMOS technology, switches can be implemented as NMOS. However, in proposed design, transmission gates have been used as switches to prevent V_{TH} drop during switching. Transmission gate based chopper has several advantages over NMOS based chopper such as increased noise margin, less switching resistance, and less power dissipation. [16]. Figure 3.16 depicts details of a chopper switch.

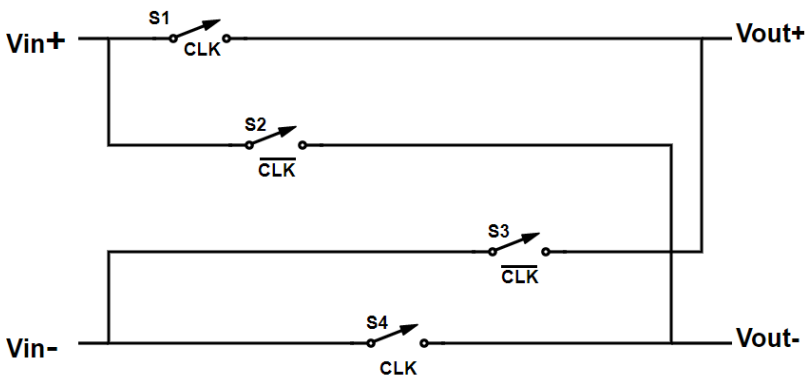


Figure 3.16. Detailed diagram of chopper

In Figure 3.17, a period of differential input signal is shown as bold outline. Both negative and positive polarities of the differential signal are chopped from peak to peak. Input and output signal is overlapped to illustrate how the chopper switch works.

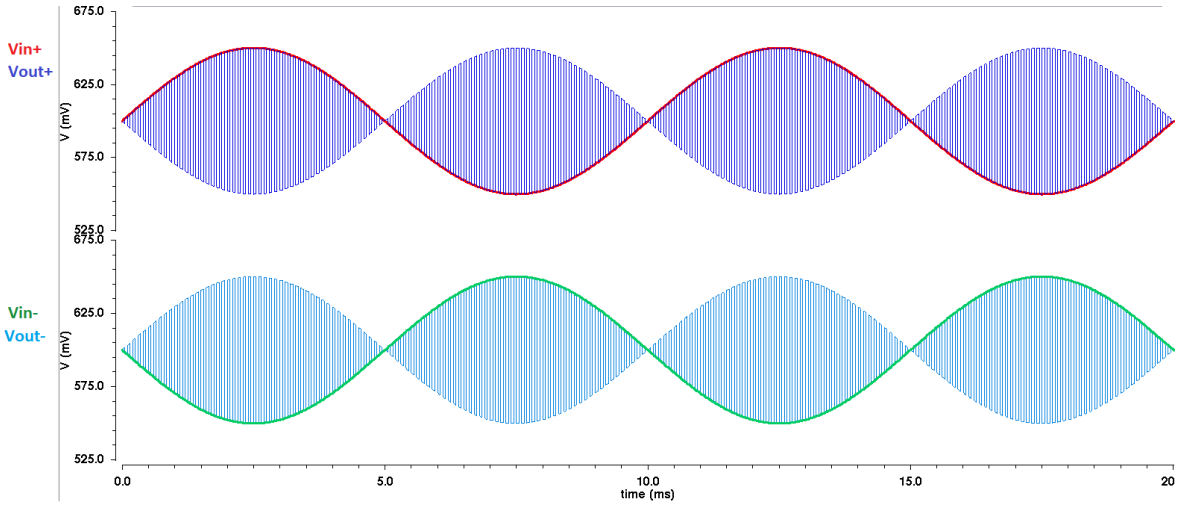


Figure 3.17. A period of input differential a signal with different polarities are shown abold. Their chopped forms are shown as differential output signal with different polarities. Signal is chopped symmetrically from peak to peak in both positive and negative polarities of signal.

3.3.2. Amplifier

In this part, a chopping amplifier and its operation with modulator and demodulator choppers are presented. A folded cascode OTA and a Class AB output stage with error amplifier is used as the amplification block of chopping topology. The scheme of chopping topology has already been illustrated. The schematic of the amplifier is shown in Figure 3.18.

The chopping amplifier is a combination of a fully differential folded cascode OTA with CMFB and CMOS class AB output stage with error amplifier. Folded cascode topology, is chosen because it has better output swing and common mode input range than the telescopic counterpart [9]. At the input of the folded cascode topology, a PMOS differential pair is chosen due to its better noise performance than the NMOS pair. The cascode part is biased by the biasing part of the circuit, which is on the left of the PMOS differential pair. At the right, the CMFB block is seen. In order to control the output common mode voltage level and reject the common-mode activity

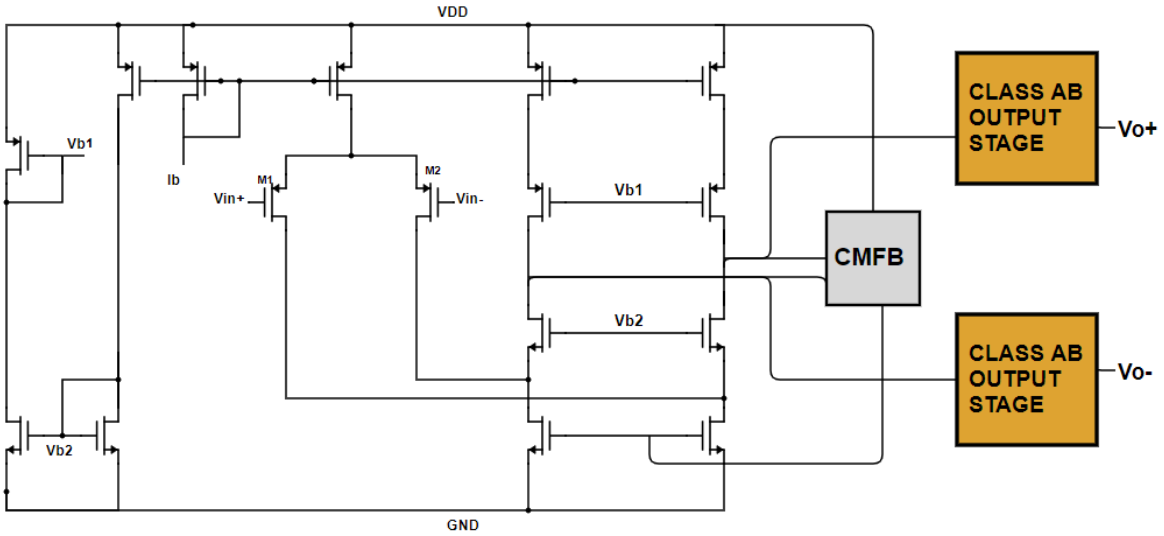


Figure 3.18. Amplifier of chopping topology with CMFB and class ab output stage.

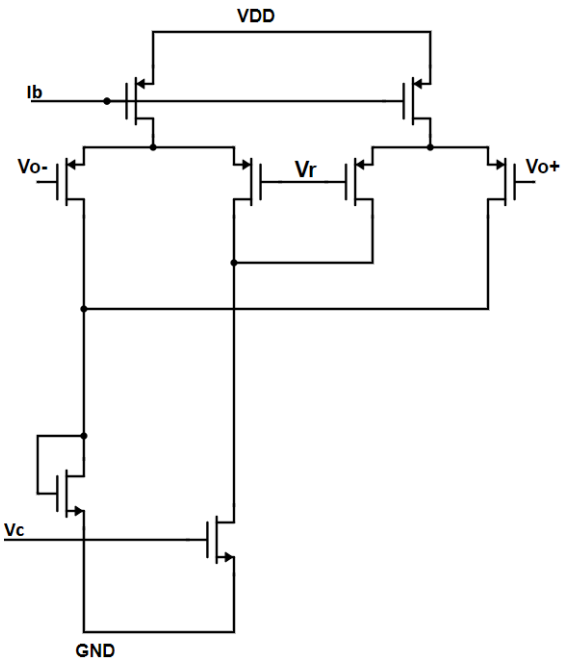


Figure 3.19. Common mode feedback with two differential pair.

of some components, CMFB with two differential pairs has been applied. Figure 3.19 depicts the CMFB circuit. However, the folded cascode amplifier suffers from low output swing due to CMFB, because the differential pair transistors of CMFB have to be on during its operation and the output swing of the folded cascode is limited by

gate overdrive voltages of these transistors [9]. In order to increase the output swing and the gain, an output stage is needed. There are several types of CMOS output stages such as Emitter Follower, Source Follower, Class B Push-Pull and CMOS Class AB Output Stages [9]. In this design, a CMOS class AB output stage was chosen. There are also several types of class AB output stage configurations. The first is the Common-Drain configuration as shown in Figure 3.20. By using this common-drain or source follower topology, large output swings can be obtained. In order to achieve this, the transistor size has to be increased that resulting in large parasitic capacitances that might affect the performance of amplifier [9]. The second one is Common-Source

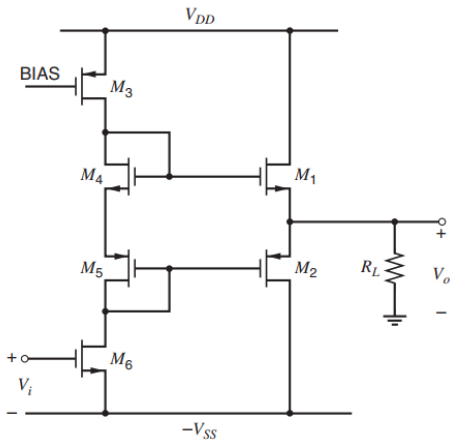


Figure 3.20. Common drain CMOS output stage [9]

configuration with error amplifiers as shown in Figure 3.21. This topology increases the output swing but has other problems. Error amplifiers of this configuration require large bandwith to prevent cross-over distortion, but this time stability issues occur due to large bandwith. Also, non-zero offset voltage of the error amplifiers change the quiescent current limiting the cross-over distortion rejection. However, increasing this current too much increases the power dissipation and decreases the output swing. Thus, error amplifiers are designed to have low gain.

Finally, combined Commond-Drain Common-source configuration, which is the preferred configuration is chosen. In this circuit, two types of buffers that are class AB common-drain buffers (M_1 and M_2) and class B quasi-complementary common-

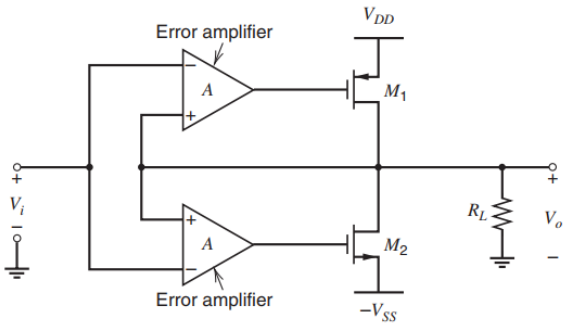


Figure 3.21. Common source configuration with error amplifiers [9]

source buffer (M_{11} and M_{12}) and the error amplifiers are used. The common source buffer is dominant with the maximum output swing, otherwise it is off. The mission of common-drain buffer is to control the quiescent output current and improves the frequency response.

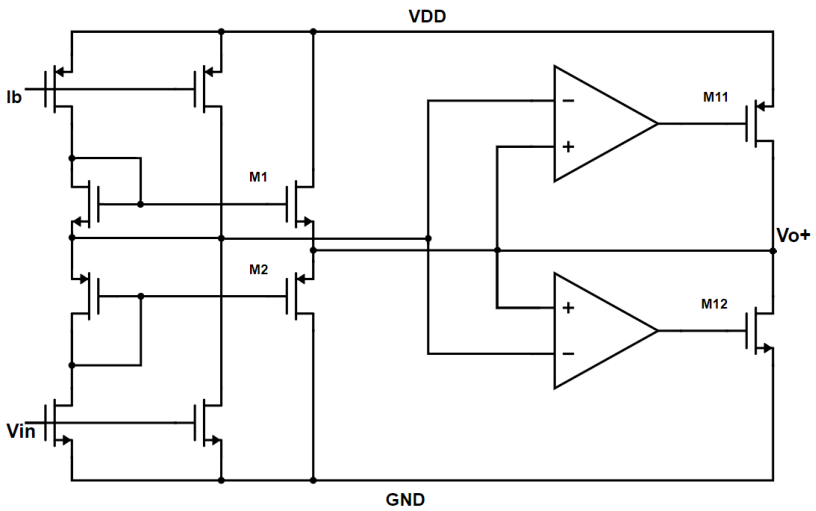


Figure 3.22. Combined common drain common source with error amplifiers [9]

After deciding on the amplifier configuration, it has been implemented and simulated in Cadence. The biasing current has been swept from 1μA to 31μA and in Figure 3.23, the differential gain varies from 28dB to 47dB with V_{pp} 200mV. Phase margin of the folded cascode with class AB output stage is at least 144 degree as shown in Figure 3.24. Since phase margin is more than 45 degree, amplifier is stable.

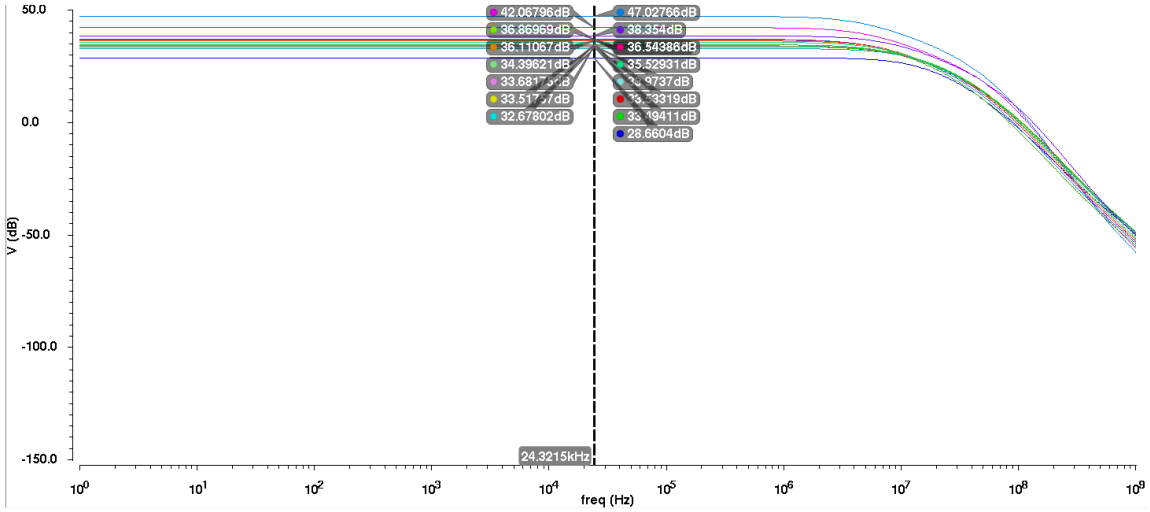


Figure 3.23. Amplifier gain for different I_{bias} values

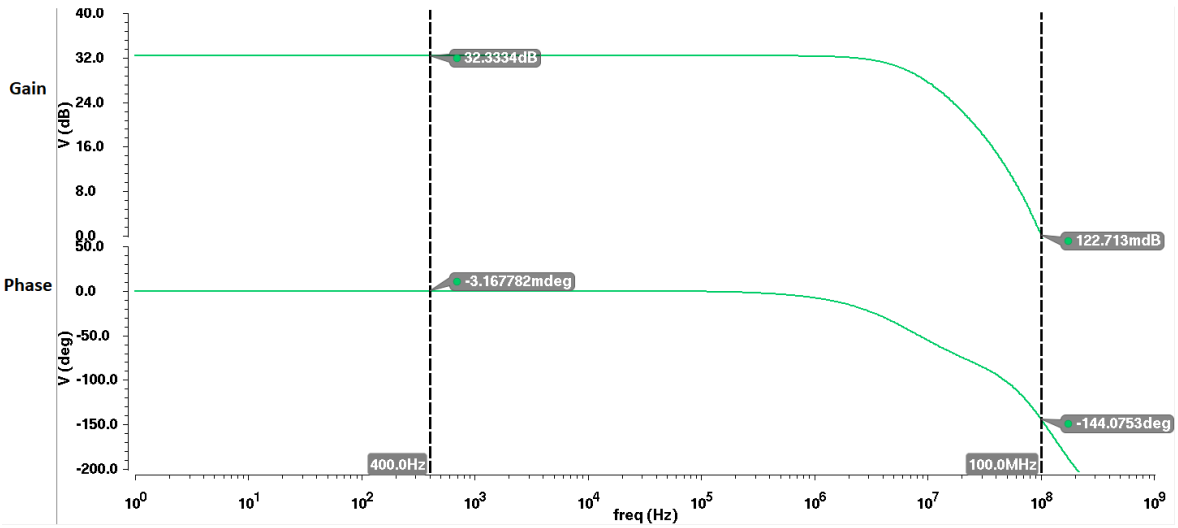


Figure 3.24. Amplifier gain with phase

3.4. Low Pass Filters

Three types of low-pass filters have been implemented. Since all filters are OTA based filters, they are tunable via the BDAC. The amplifiers of active RC and switched capacitor filters are OTA based as well. Thus, they can be tuned by the BDAC. In the following sections, the implemented filter will be explained.

3.4.1. Active RC Filter

Active RC filters consists of OPAMPs, resistors, and capacitors. In this work, a second order low-pass Chebyshev filter has been implemented. The filter function is shown as in equation 3.4 and the schematic of the filter is illustrated in Figure 3.25.

$$H(s) = \frac{\frac{1}{R^2.C_1.C_2}}{s^2 + \frac{s}{R.C_2} + \frac{1}{R^2.C_1.C_2}} \tag{3.4}$$

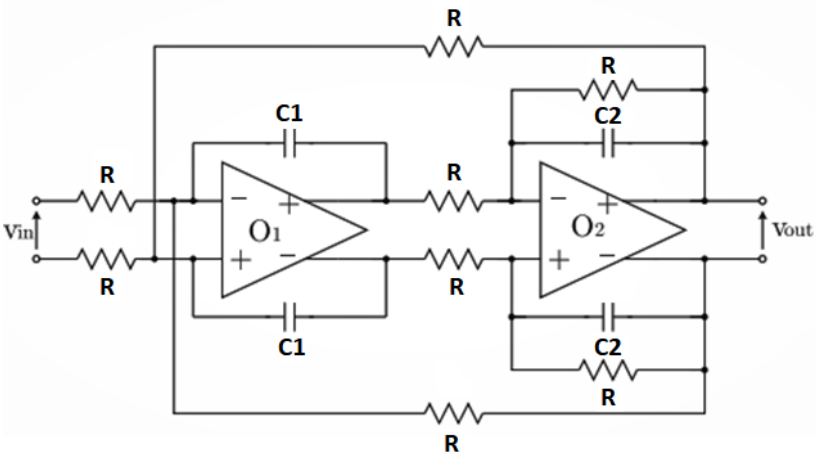


Figure 3.25. Fully differential 2nd order low pass active rc filter [10]

It is assumed that the OPAMP gain A = A(s) = $\frac{A_0}{1+s/w_0}$ where w_0 is the 3-dB point of the OPAMP bandwith. Then, the filter transfer function is transformed into equation 3.5.

$$H_A(s) = \frac{\frac{1}{R^2.C_1.C_2.(1+A^{-1})^2}}{s^2 + s(\frac{1+2A^{-1}}{R.C_2.(1+A^{-1})} + \frac{1}{R.C_1(1+A)}) + \frac{1+3/(1+A)^2}{R^2.C_1.C_2}} \tag{3.5}$$

This active RC filter was implemented on Cadence. For simplicity, all resistance values were kept the same as 10 kΩ. Capacitor values of C_1 and C_2 are 1 nF and 800 pF respectively.

Tunability of the Active RC filter is between 1kHz and 16.4kHz cut-off frequencies when capacitance value is swept. This means that, using the designed active RC filter, signals in the frequency range of the active RC filter can be read and evaluated. Therefore, a capacitor array can be used to tune the capacitance of active rc filter. Figure 3.26 depicts filter characteristic.

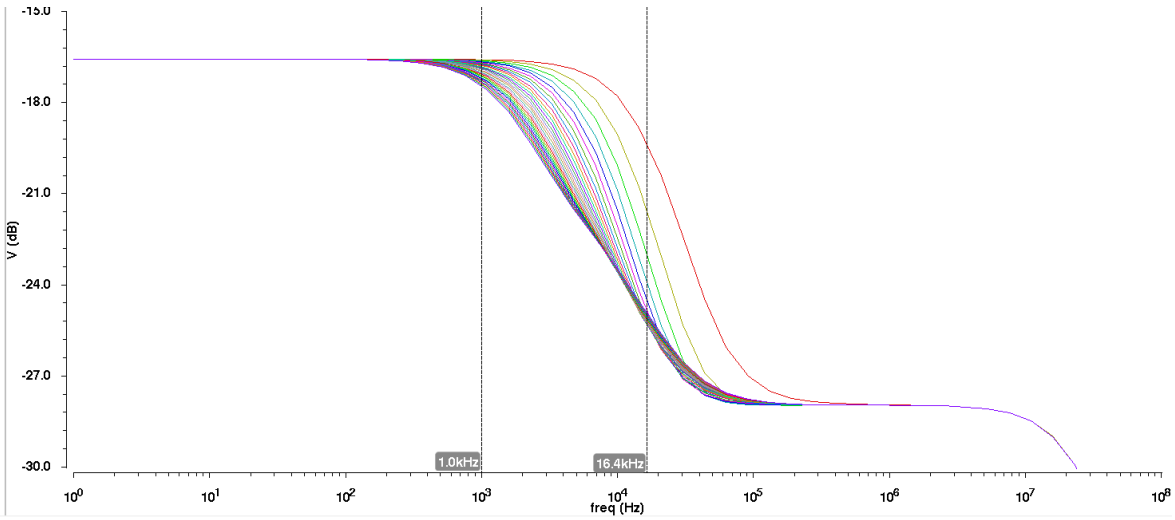


Figure 3.26. Fully differential active rc filter characteristic for different capacitor values

3.4.2. Switched Capacitor Filter

In this section, the design of the low-pass switched capacitor filter has been explained. Fully differential configuration of Low Q Biquad topology Figure3.27 has been implemented [24]. Switches used in filters are transmission gate switches to prevent V_{TH} drop. The amplifier is the previously discussed OPAMP that was used in active RC filters as well. The component values are found by following a series of steps. Initially, frequency warping is carried out. Then, by using bilinear transform, the transfer function is transformed from the s domain to the z domain. Using the z domain transfer functions, capacitor values can be found. The filter is implemented in Cadence. Frequency warping and s domain transfer function of the biquad is shown in equations 3.6 and 3.7 respectively.

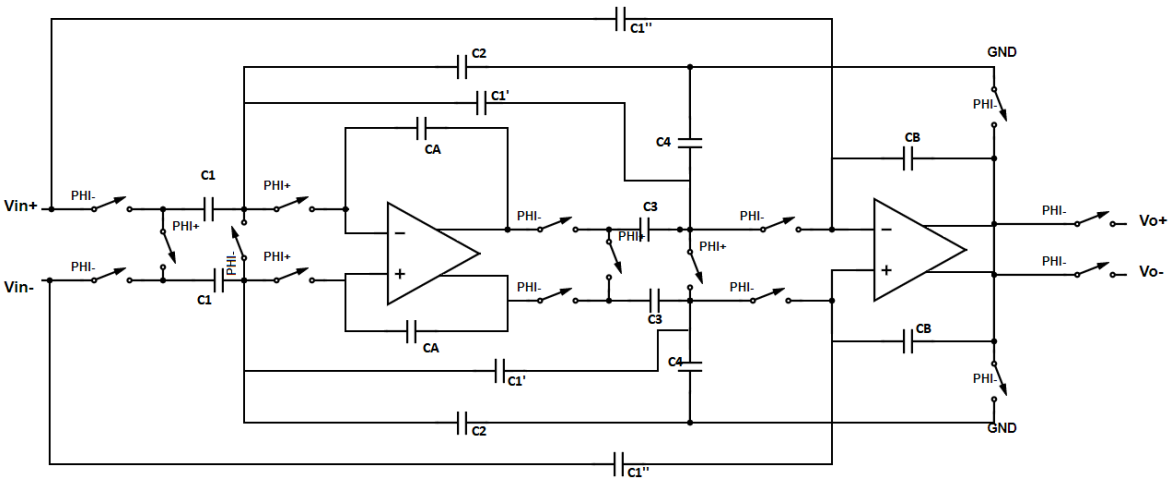


Figure 3.27. Fully differential low-q biquad switched capacitor filter

$$f_{PRLC} = \frac{f_s}{\pi}.tan(\pi.\frac{f_p}{f_s}) \tag{3.6}$$

$$H(s) = \frac{1}{1 + \frac{s}{\omega_{PRLC}Q_p} + \frac{s^2}{\omega_{PRLC}^2}} \tag{3.7}$$

Then, the bilinear transform is applied to H(s) where $f_{BL} = 10\text{kHz}$ $Q_p = 5$, $f_s = 1\text{MHz}$ and s is

$$s = \frac{2}{T_s}\frac{1 - z^{-1}}{1 + z^{-1}} \tag{3.8}$$

H(z) is found as in equation 3.9.

$$H(z) = \frac{0,033z^2 + 0,066z + 0,03}{1.11z^2 - 1.98z + 1} \tag{3.9}$$

$$H(z) = \frac{-(C_1' + C_1'')z^2 + (C_1C_3 - C_1' - 2C_{1''})z + C_{1''}}{(1 + C_4)z^2 + (C_2C_3 - C_4 - 2)z + 1} \tag{3.10}$$

Using equations 3.9 and 3.10, component values have been calculated and the filter has been implemented in Cadence. After implementation, the filter has been simulated using periodic AC (PAC) analysis. This filter can be tuned using a capacitor array. Thus, tunability of switch capacitor filter derives from changing capacitor values of capacitor array.

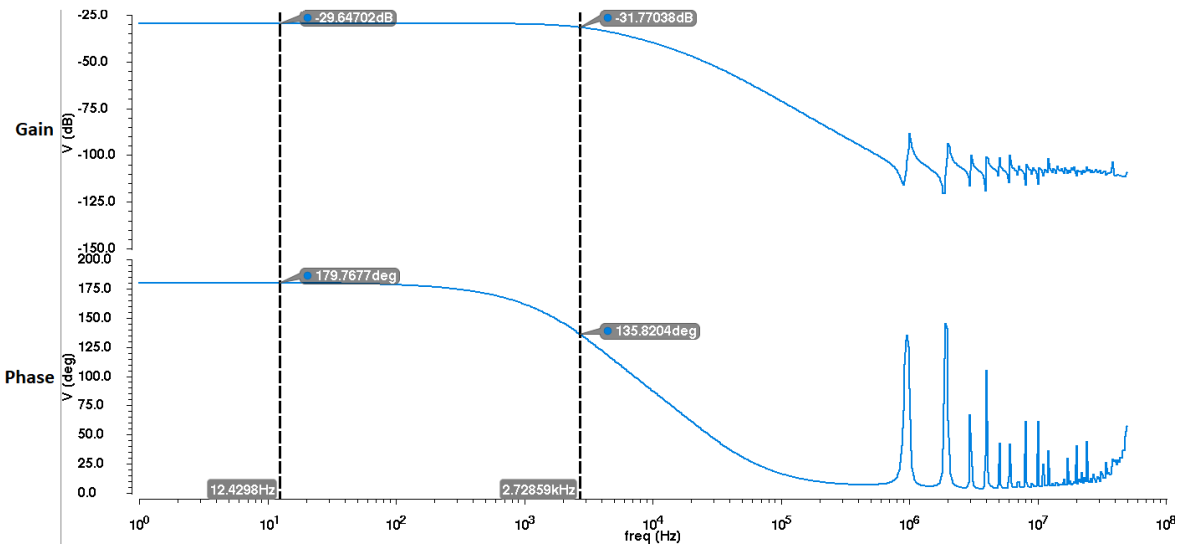


Figure 3.28. Result of periodic ac analysis of fully differential low-q biquad switched capacitor filter

3.4.3. Gm-C Filter

G_m-C filters are the most tunable filter topology used in both industry and academic designs because gm-c filters or OTA-C filters are easy to tune via the biasing current of OTAs. Besides, they consume low power and they have less phase shift than other filter types. Tuning the transconductance value of OTAs gives flexibility during filter design. However, in filter design, transconductance characteristics of the OTAs used in amplifiers are not as linear as desired. In order to achieve linear transconductance or G_m characteristics, linearization techniques such as current division [25] and source degeneration [26] are required. Transconductance of the OTA is the same

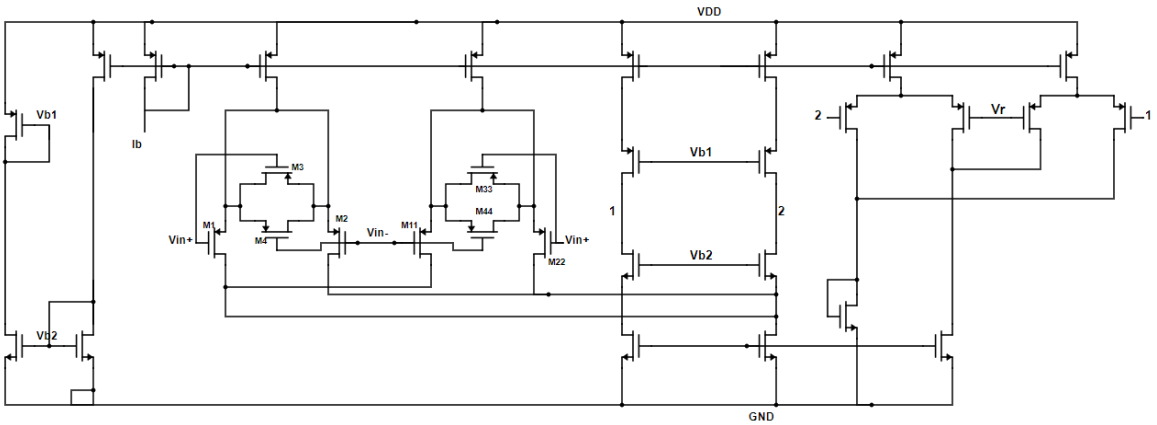


Figure 3.29. Schematic of linearized OTA with source degeneration and current division

as the transconductance of the differential PMOS transistors $g_{m1,2}$, which is equal to $\sqrt{2.K_{1,2}.I_b}$. The relationship between input differential voltage V_{id}, G_m, and output current I_o in the linear operating region of OTA is given by;

$$I_o = G_m.V_{id}\sqrt{1-(\frac{V_{id}}{2.V_{ov}})^2} \tag{3.11}$$

OTAs can be biased via biasing current I_{bias} under a vital constraint which is $V_{id} < 2.V_{ov}$ for low voltage operations. Thus, in order to remove second harmonics, linearization techniques have been applied, and the source degeneration resistors have been replaced with transistors which are operating in sub-threshold region [11].

Current division method linearizes the transconductance characteristics of the OTA by adding two input pair transistors to the differential input of the OTA as shown in the Figure 3.30.

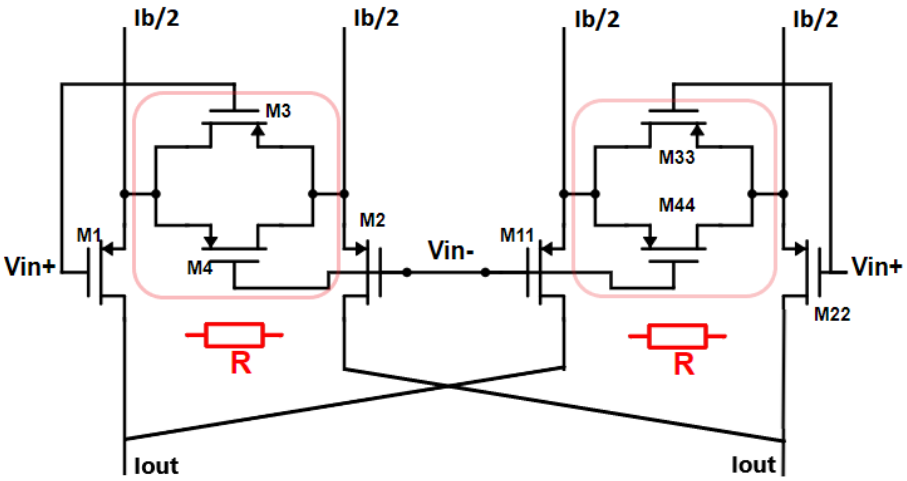


Figure 3.30. Current division and source degeneration method scheme [11]

$$\frac{G_{m1}}{(V_{ov1})^2} = \frac{G_{m2}}{(V_{ov2})^2} \tag{3.12}$$

$$I_{oi} = G_{mi}.V_{id}(1 - (\frac{(V_{id})^2}{8.(V_{ov})^2}) \tag{3.13}$$

The most important point in this step is to remove the third harmonic term of I_o. To achieve this, the transistors $M_{1,2,11,22}$ in Figure 3.30 have to satisfy the condition in Equation 3.12. This equation states that these transistors have to be matched as much as possible. However, even if this condition is satisfied, the third harmonic term in Equation 3.13 cannot be cancelled completely due to mobility degradation. In other words, in small geometry devices, carriers in the channel of the MOSFET scatter due to high electric field between the gate and the channel which decreases the mobility

of the carriers resulting in mobility degradation. Thus, μ_{eff} decreases as in Equation 3.14 which shows effective μ has third harmonic term in itself [27].

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_{GS} - V_{TH})} \tag{3.14}$$

Since current division method alone is not adequate to remove the third harmonic term, source degeneration method has been applied to the OTAs. In the conventional approach, source degeneration method uses resistors; however, they are replaced by transistors operating in triode region since resistors add parasitics, cause thermal noise, occupy large area, and decrease individual and overall transconductance of OTAs [26]. As shown in Figure 3.30, transistors $M_{3,4,33,44}$ are used for source degeneration and if they are matched, it is possible to obtain higher transconductance. By combining current division and source degeneration methods, the effect of third the harmonic term is decreased further. This can be observed in the output current as shown in equation 3.15 [11].

$$I_o = \frac{G_m.V_{id}}{S}\sqrt{1 - 2.(\frac{V_{id}}{S.V_{ov}})^2} \tag{3.15}$$

where

$$S = 1 + \frac{\beta_{1,2}}{4.\beta_{3,4}} \tag{3.16}$$

Applying source degeneration method by adding source degeneration transistors transforms Equation 3.12 to Equation 3.17.

$$\frac{G_{m1}}{(S_1)^3(V_{ov1})^2} = \frac{G_{m2}}{(S_2)^3(V_{ov2})^2} \tag{3.17}$$

S_1 and S_2 are the parameters of $M_{3,4}$ and $M_{33,44}$ respectively. As it is obvious from Equation 3.15, the S parameter decreases the third harmonic term and also total transconductance according to Equation 3.15. Then, the total transconductance can be express as Equation 3.18.

$$G_{mtotal} = \frac{G_{m1}}{S_1} - \frac{G_{m2}}{S_2} \tag{3.18}$$

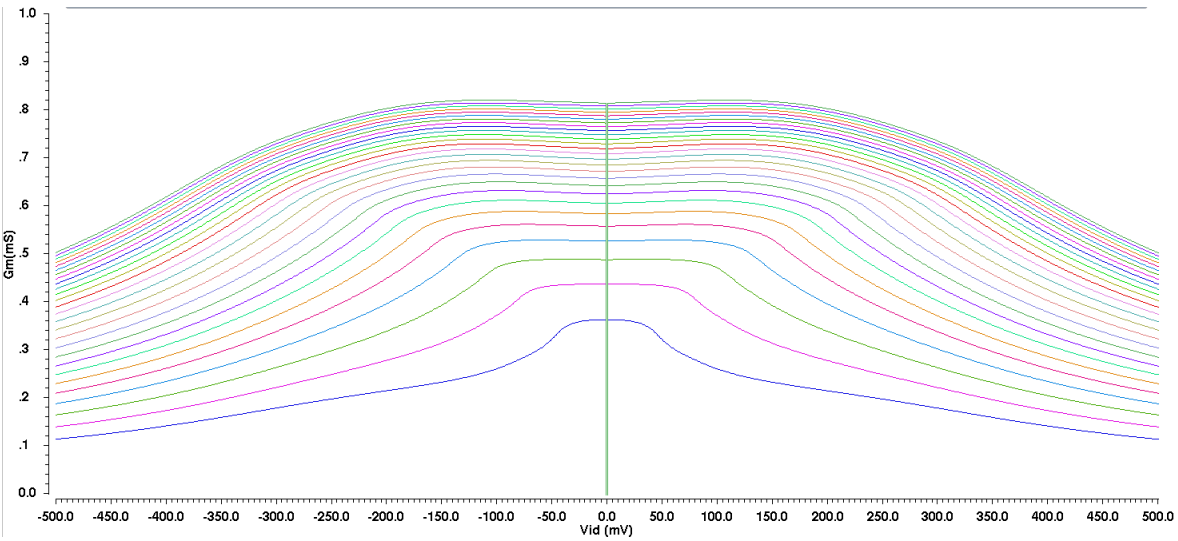


Figure 3.31. Overall transconductance characteristics of G_m

However, equation 3.18 is valid for the source degeneration topology with resistors. Replacing resistors with transistors limits the loss in G_{mtotal}. The output current and transconductance characteristics of Linear OTA have been simulated in Cadence and the results are shown in Figure 3.31. The biasing curent from BDAC is swept from 0μA to 31μA, V_{id} is swept from -0.3V to 0.3V, and overall G_m of the linearized OTA varies from 360uS to 825uS.

Similarly, simulation results for the output current I_{out} is shown in Figure 3.32. Between -0.3V and 0.3V V_{id}, the output current I_{out} has linear characteristics as in Figure 3.32. The designed OTAs are combined to implement fully differential 5th

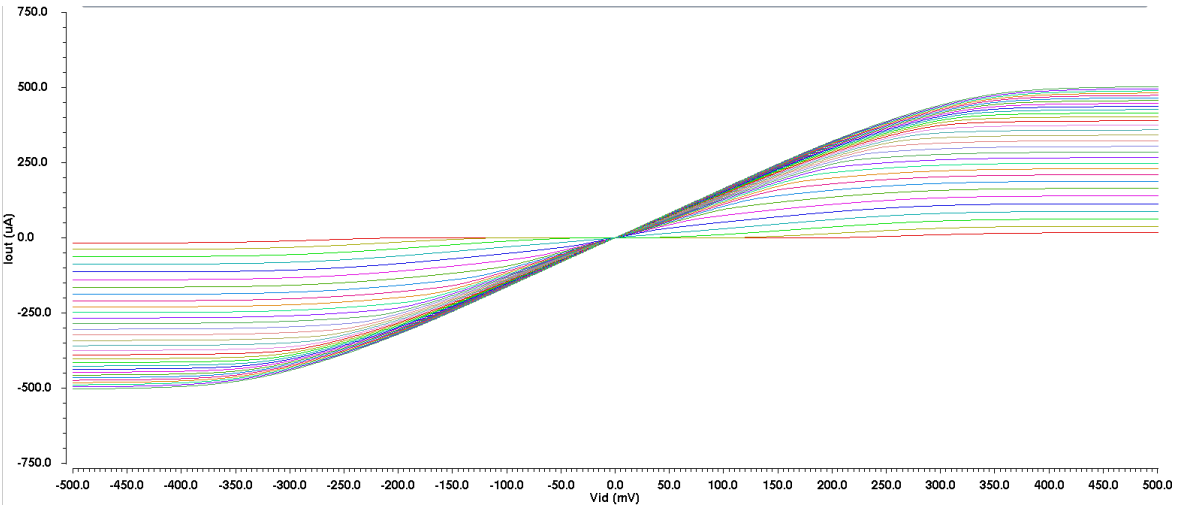


Figure 3.32. Output current I_{out} characteristic of linearized OTA

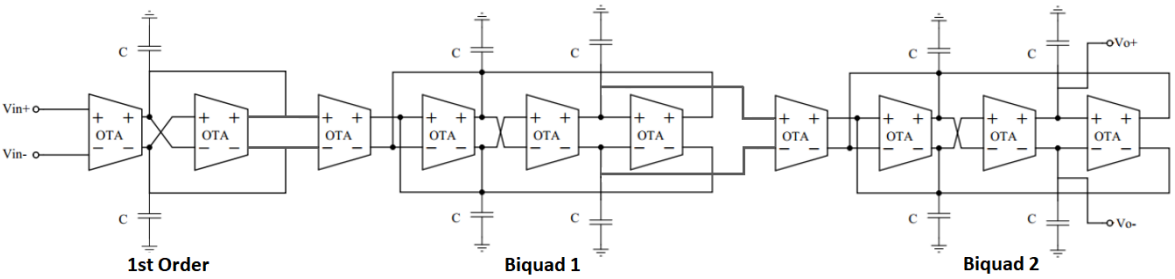


Figure 3.33. Fully differential 5th order butterworth G_m-C filter

order Butterworth G_m-C filter as shown in Figure 3.33. 10 identical OTAs are used in G_m-C filter. All g_{mi} values are equal to each other and C = C_1 = C_2. The cut-off G_m-C filter can be found as $f = \frac{g_{mi}}{C}$ and the quality factor Q can be calculated as $Q = \frac{g_{mi}}{g_{mi2}}$. The transfer function of the filter is shown in equation 3.19. The first part of equation is the first order transfer function, the other parts are the biquad sections.

$$H(s) = [\frac{G_{m1}}{G_{m2} + C_s}].\frac{\frac{g_{m11}}{g_{m14}}.\frac{gm_{13}.gm_{14}}{C_1.C_2}}{s^2 + s(\frac{g_{m12}}{C_1}) + \frac{g_{m13}.g_{m14}}{C_1.C_21}}.\frac{\frac{g_{m21}}{g_{m24}}.\frac{gm_{23}.gm_{24}}{C_1.C_2}}{s^2 + s(\frac{g_{m22}}{C_1}) + \frac{g_{m23}.g_{m24}}{C_1.C_21}} \tag{3.19}$$

This filter is then implemented in Cadence and simulated. In order to show its tunability, the biasing current from BDAC is swept from 1μA to 31μA and various cut-off frequencies are observed. The 1μA biasing current corresponds to the cut-off frequency 13.2 kHz, 31μA bias current corresponds to cut-off frequency 132 kHz as shown in Figure 3.34. As a result, the tunability range of G_m-C filter is better than the other filter types since G_m of the OTA can be tuned linearly via I_{bias} in a wide frequency range without gain loss.

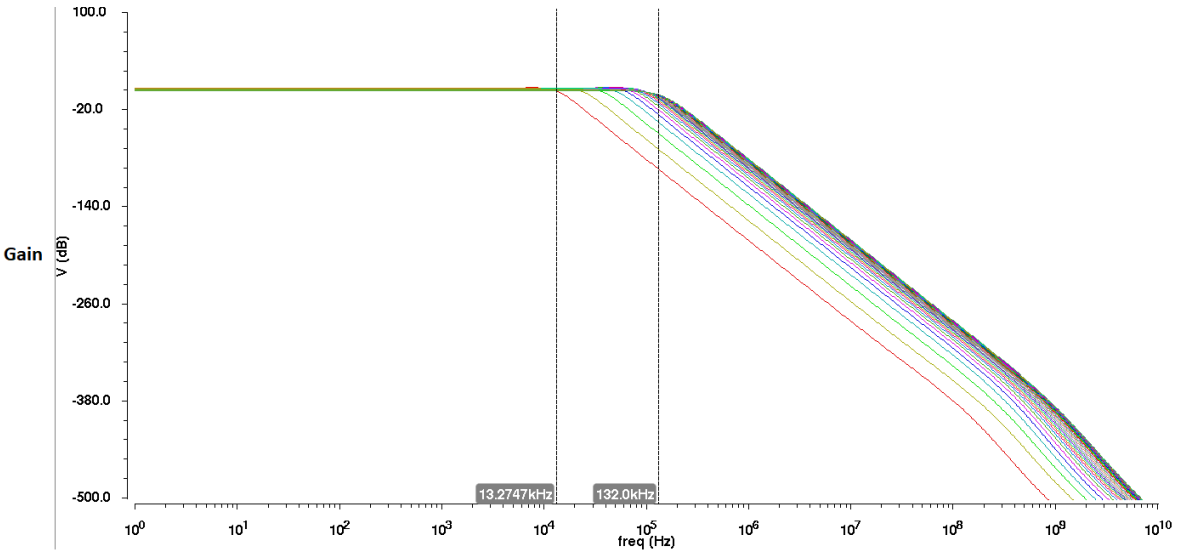


Figure 3.34. Fully differential 5th order Butterworth G_m-C filter after tuning I_{bias}

4. SIMULATIONS AND RESULTS

In this chapter, pre-layout and post-layout simulations of the entire system will be presented and the results will be evaluated.

4.1. Pre-layout and Post-layout Simulations

All designed circuits are merged in a test bench to simulate the entire topology. Each filter topology with chopping amplifiers, BDACs, and Bandgap Reference Circuit have been implemented on test bench circuits. The first topology is the one with the active RC filter as displayed in Figure 4.1. At the input V_{pp}= +/ -1mV, f= 100Hz

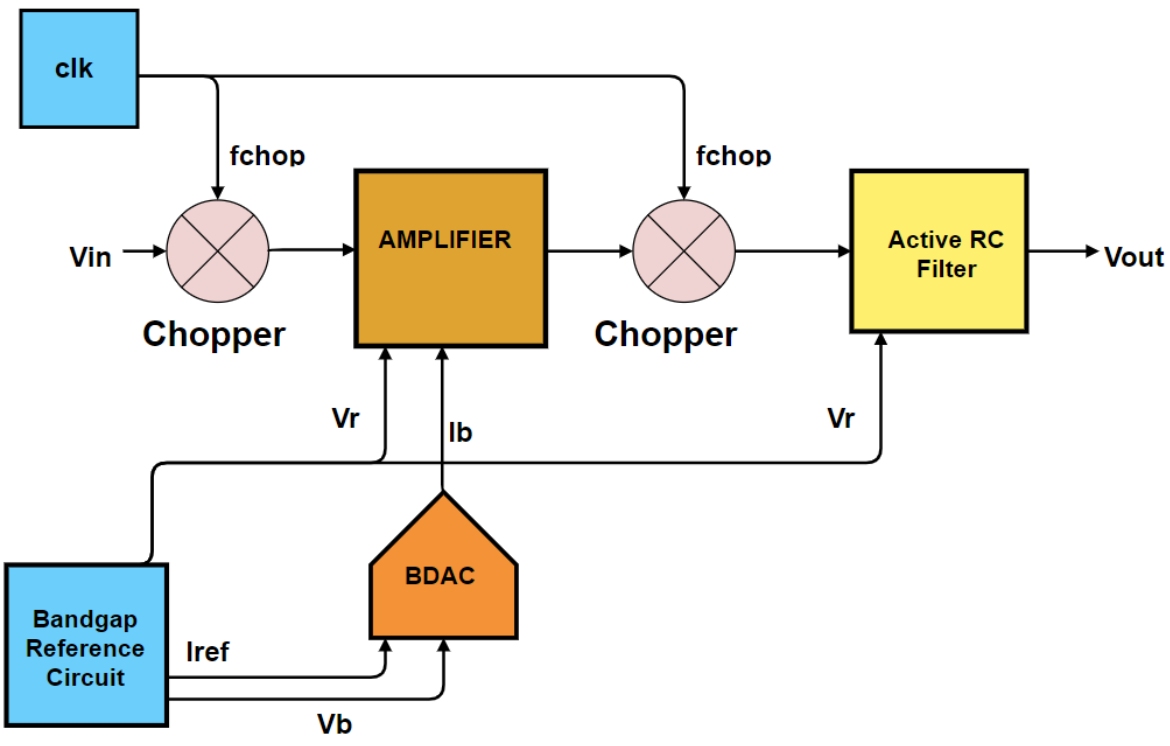


Figure 4.1. Proposed chopping topology with tunable active rc filter

signal is applied. Simulation results are displayed in Figure 4.2. The two rows at the top are the differential input signals, the next two rows are their chopped form, and below the chopped form, the filter input is observed. At the bottom two rows, the

differential signals at the filter output are illustrated. The output signal has the same V_{pp} value as the input signal. In the next step, an artificial 10mV offset is applied to one of the inputs of the amplifier as in Figure 4.3. The result is the same as the topology without offset, which means that the offset is eliminated.

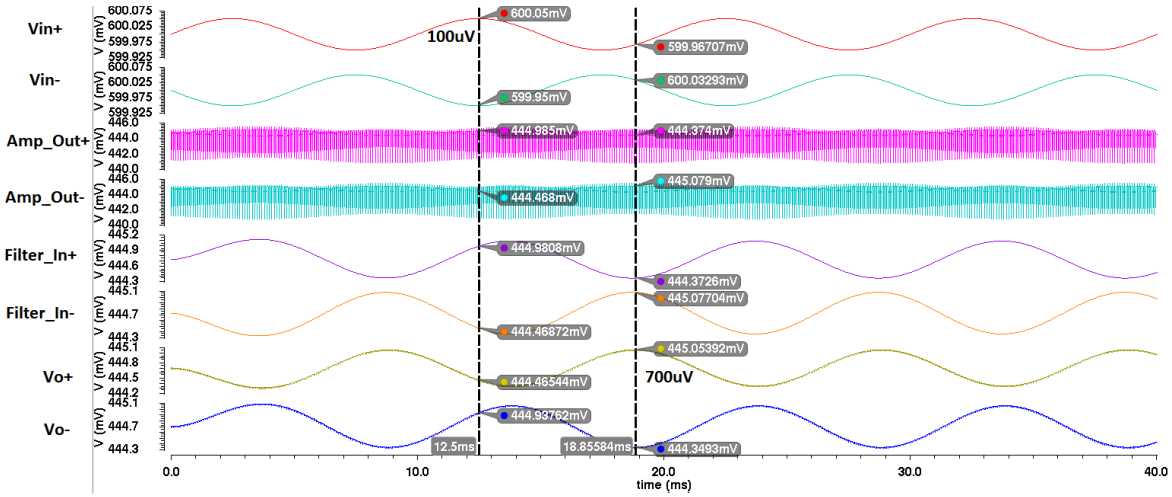


Figure 4.2. Simulation results of chopping topology with tunable active rc filter

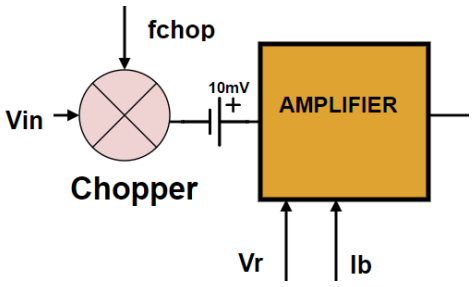


Figure 4.3. 10mV offset source between chopper circuit and amplifier

The next topology is with the switched capacitor filter. The same input signals are applied to the input of the chopping topology. In Figure 4.4, the chopping topology with SC Filter, Biasing Circuit and BDACs are shown. Simulation results are as good as the results of active RC filter but V_{pp} of output signal is decreased from 100mV to 71mV due to filter atenuation. Similar to the previous topology, 10mV offset voltage is applied to this configuration and at the output that offset was eliminated. Results of the simulations are presented in Figure 4.5.

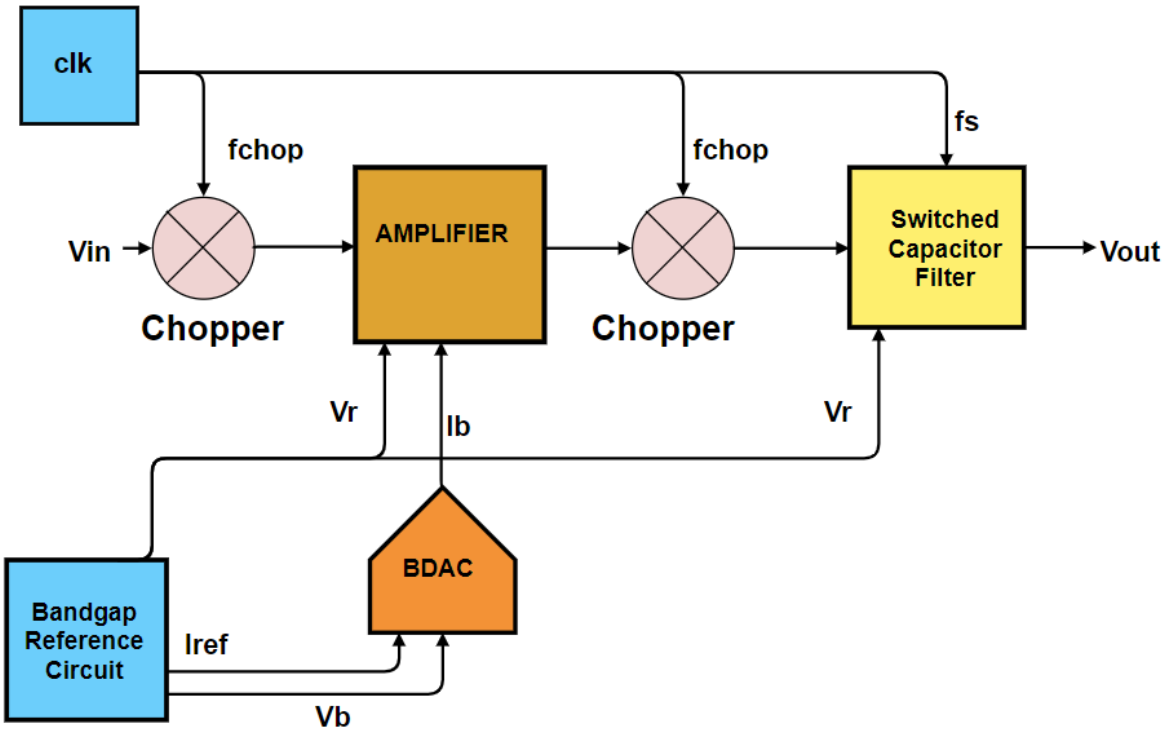


Figure 4.4. Chopping topology with tunable switched capacitor filter

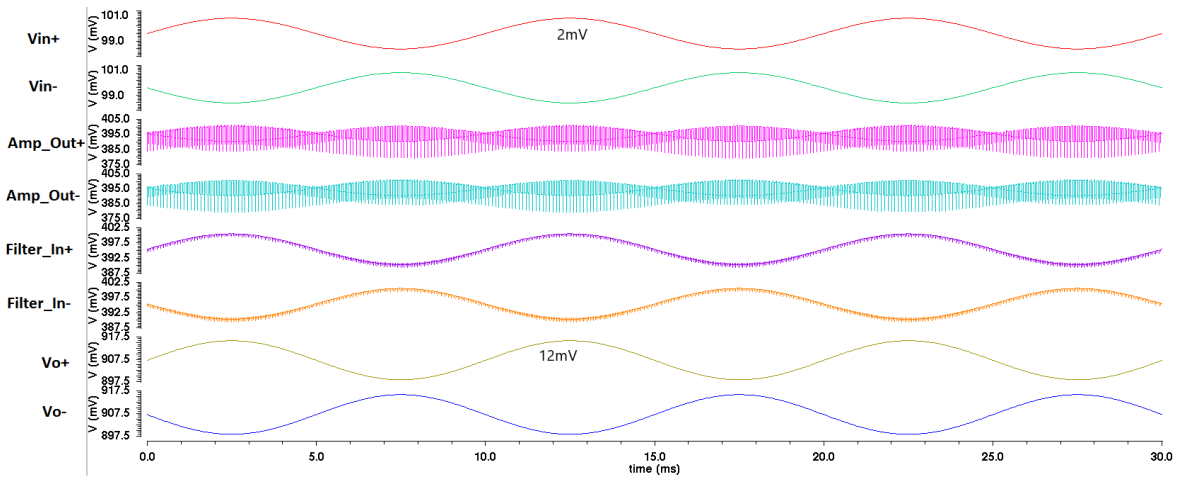


Figure 4.5. Simulation result of chopping topology with tunable switched capacitor filter

The final and the best topology uses G_m-C filter as illustrated in Figure 4.6. Filter characteristics are linear with ideal inputs, and this can be easily observed after the filter is connected to the chopping topology. In Figure 4.6, the chopping topology

and the G_m-C filter is at the center, at the left there is a clock signal generator for choppers. Bandgap reference circuit is at the bottom left to supply biasing voltages and current to the entire design. The BDAC below the amplifier generates biasing current for the amplifier, while the remaining 10 BDACs are for the OTAs in the G_m-C filter. Simulation results are displayed in Figure 4.7, where the differential input signals

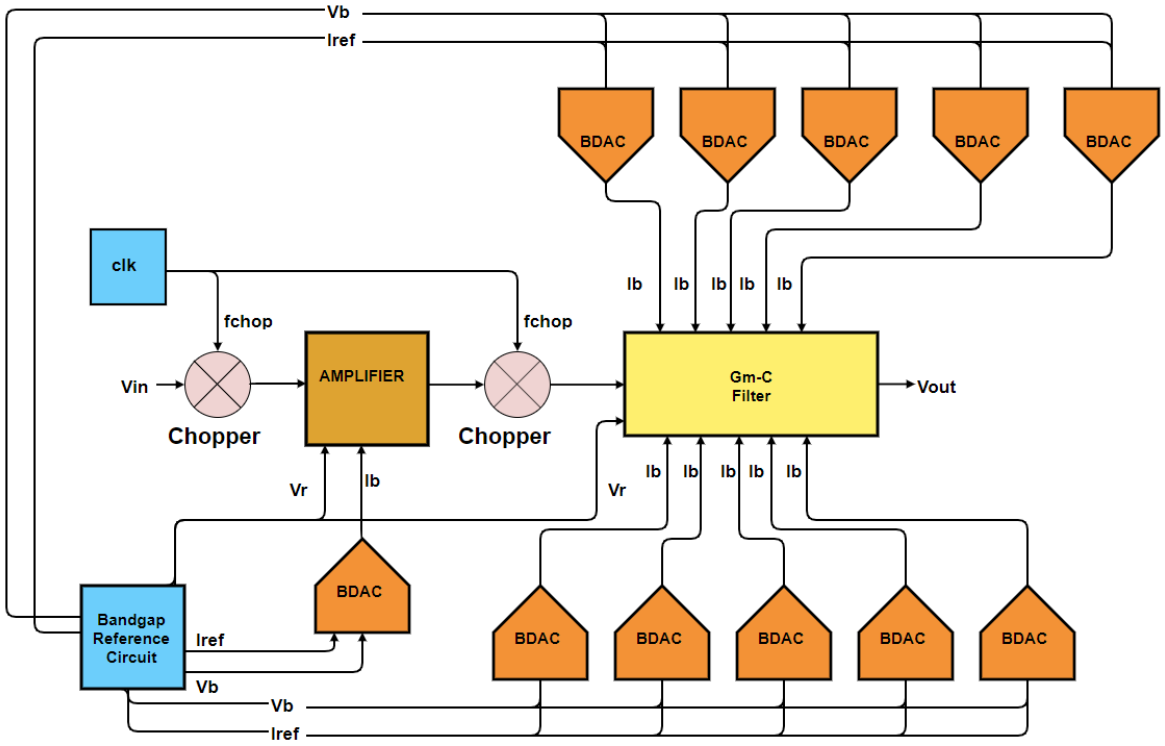


Figure 4.6. Chopping topology with tunable G_m-C filter

are at the top, and below them are the chopped, the demodulated and filtered signal pairs, respectively. The 10mV offset that was added to the input of the amplifier is eliminated in this configuration as well. Figure 4.7 depicts the simulation results.

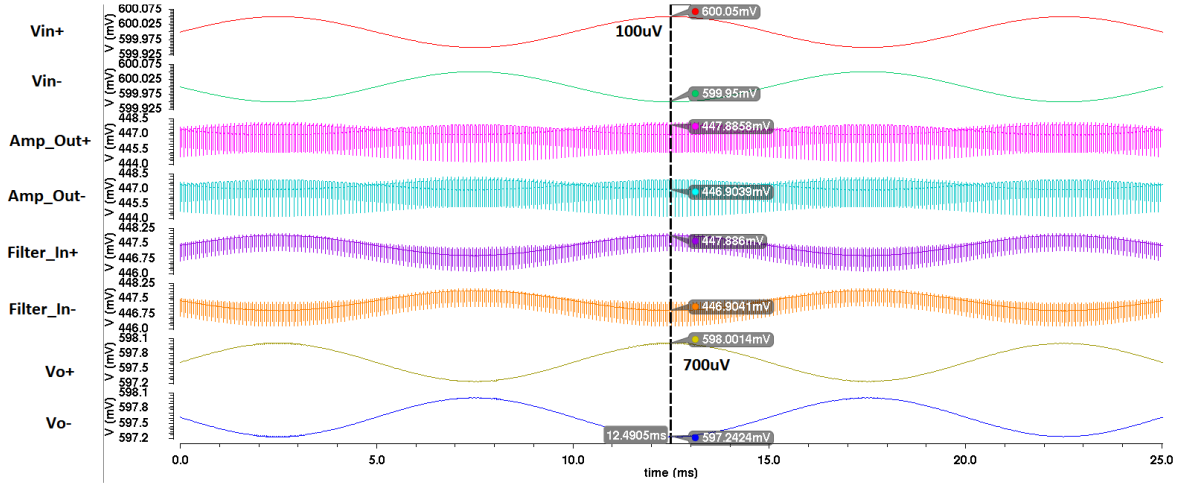


Figure 4.7. Simulation result of chopping topology with tunable G_m-C filter

After these simulations, layouts of the designed components were drawn in Cadence. Design Rule Check (DRC), Layout Versus Schematic (LVS), and Parasitic Extraction (PEX) analyses were run followed by post layout simulations. Except BDAC and Bandgap Reference Circuit, other post-layout simulation results are identical to pre-layout simulation results. However, post-layout simulation of the entire system does not perform as good as the pre-layout simulation.

Figure 4.8 illustrates the layout of the chopper circuit. Post layout simulation of the chopper circuit is shown in Figure 4.9. Results are identical to the pre-layout simulation.

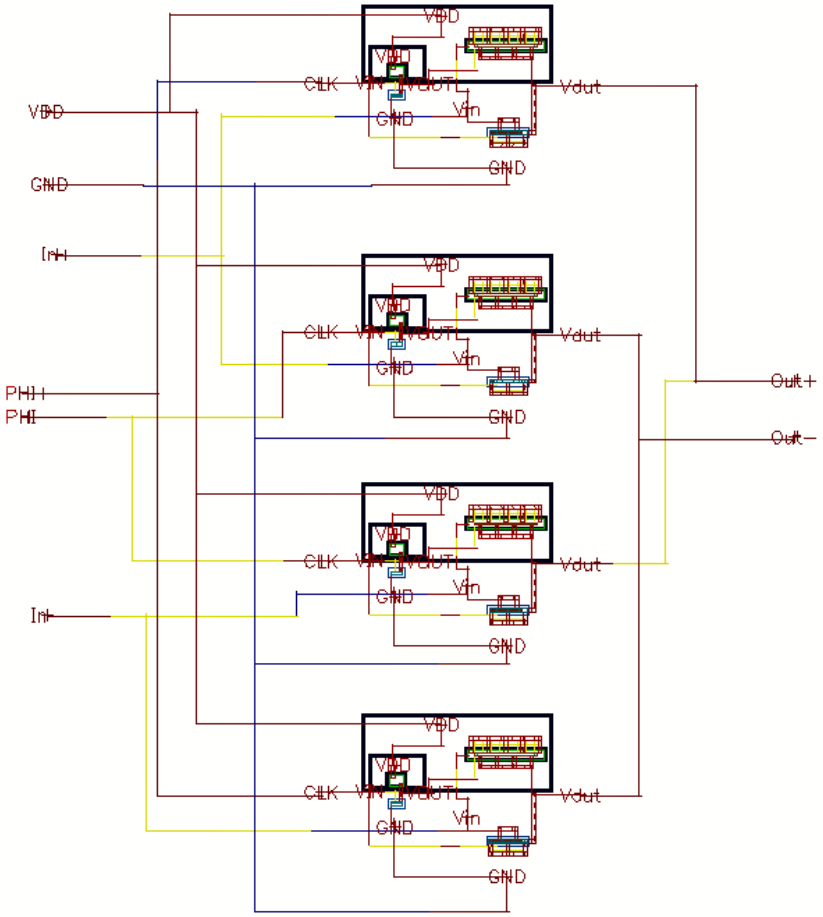


Figure 4.8. Layout of chopper

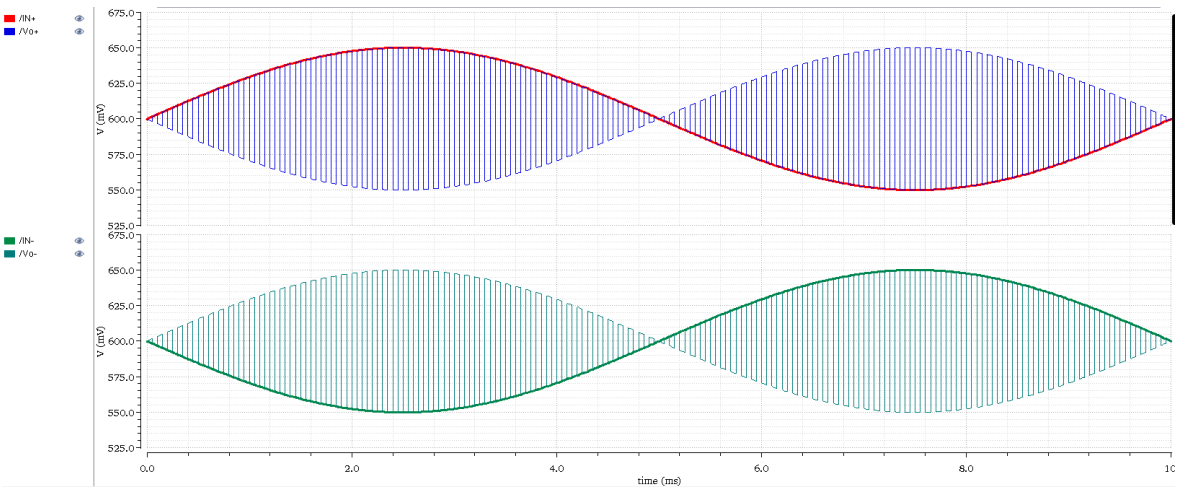


Figure 4.9. Post-layout simulation of chopper circuit

Similarly, post-layout simulation of the folded cascode OTA of the system was run. Results match pre-layout simulation for this circuit as well. Figures 4.10 and 4.11 depict the layout and post-layout simulation results, respectively.

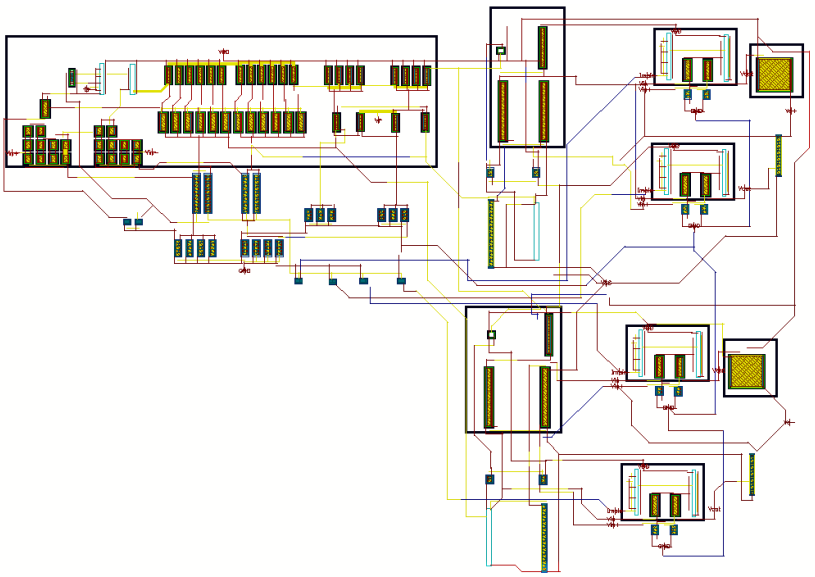


Figure 4.10. Layout of folded cascode OTA with CMFB and class ab output stage

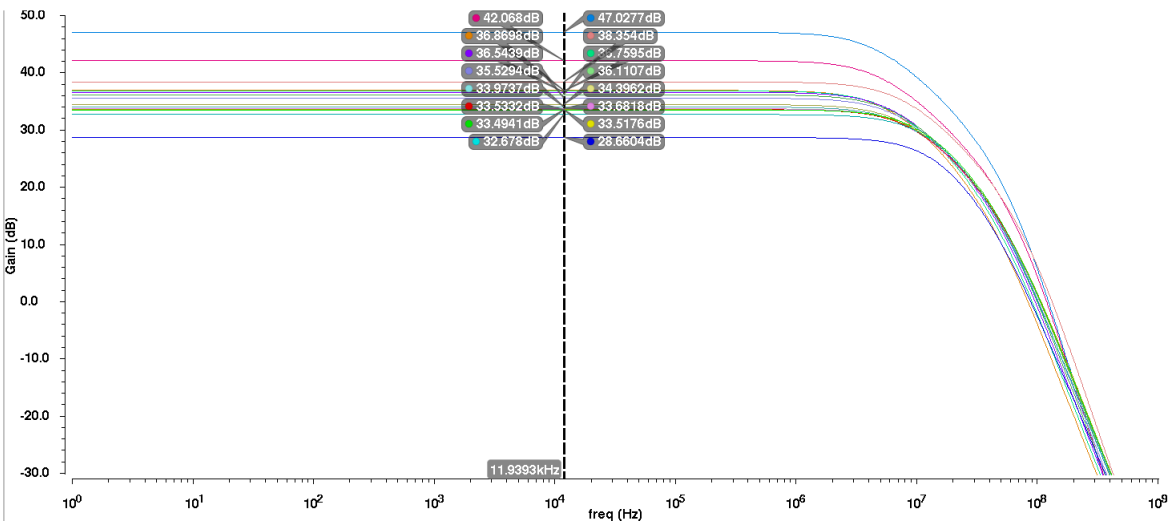


Figure 4.11. Post-layout simulation of folded cascode OTA with CMFB and class ab output stage

Figure 4.12 depicts the layout of the linearized OTA circuit. Post-layout simulations of the linearized OTA and the G_m-C filter were run, as well. Since the results of post-layout simulation of the OTA are identical to pre-layout simulation results, it is also valid for the G_m-C filter. Post-layout simulations transconductance (G_m) and output current (I_{out}) characteristics of the OTA are shown in Figures 4.13, 4.14, 4.15.

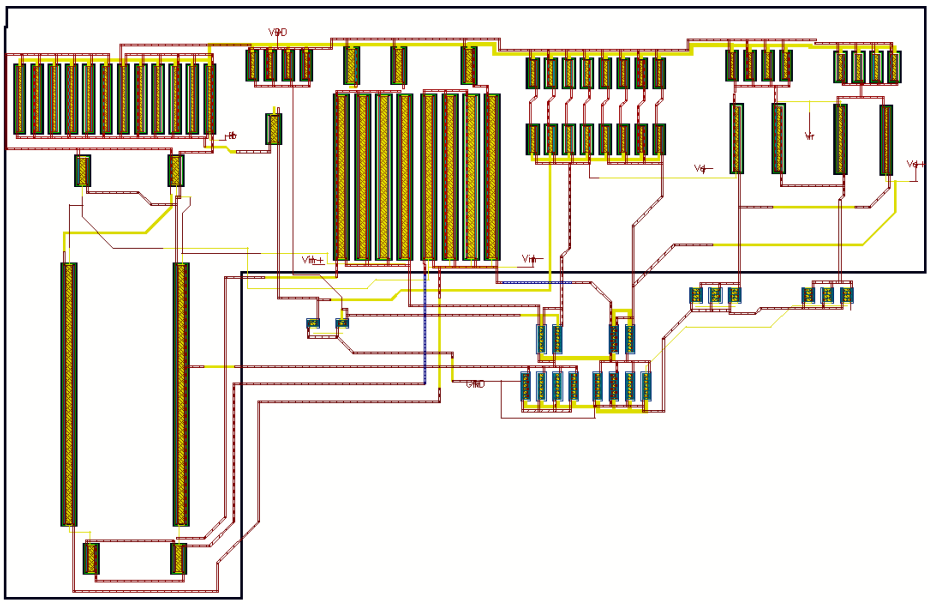


Figure 4.12. Layout of linearized OTA

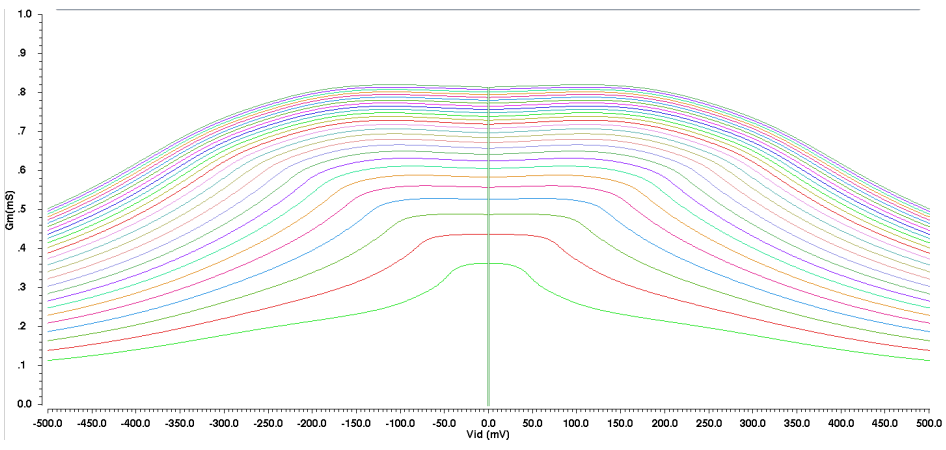


Figure 4.13. Transconductance of linearized OTA after post-layout simulation

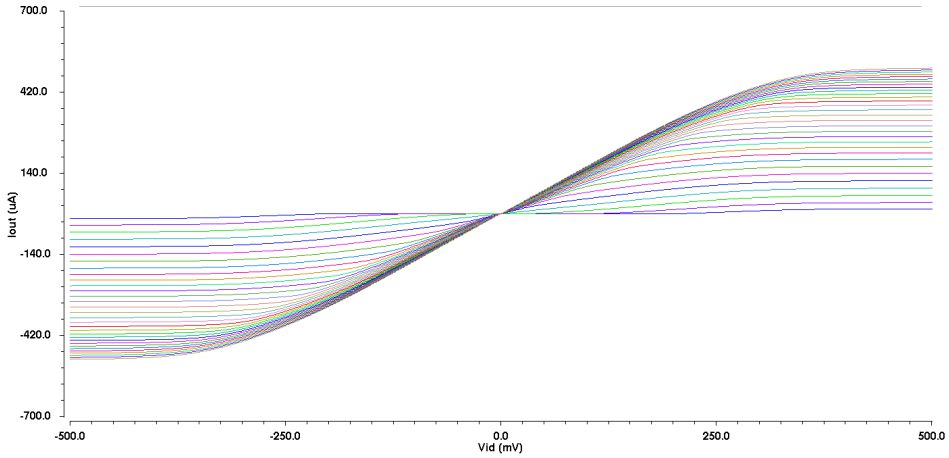


Figure 4.14. Output current I_{out} of linearized OTA after post-layout simulation

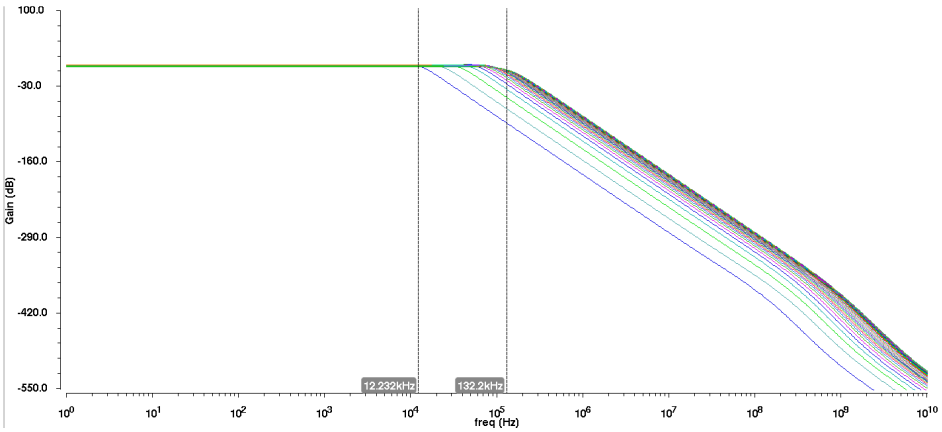


Figure 4.15. Post-layout simulation of G_m-C filter

Post-layout simulation of bandgap reference circuit was also run. Results differ with the pre-layout simulations. Reference current decreased from 1μA to 744nA, V_R decreased from 623mV to 451XmV which affect common-mode level of amplifiers and OTAs, and V_B decreased from 903mV to 788mV that affects biasing of BDAC. Layout of the bandgap reference circuit and its post-layout simulations are shown in Figures 4.16 and 4.17, respectively.

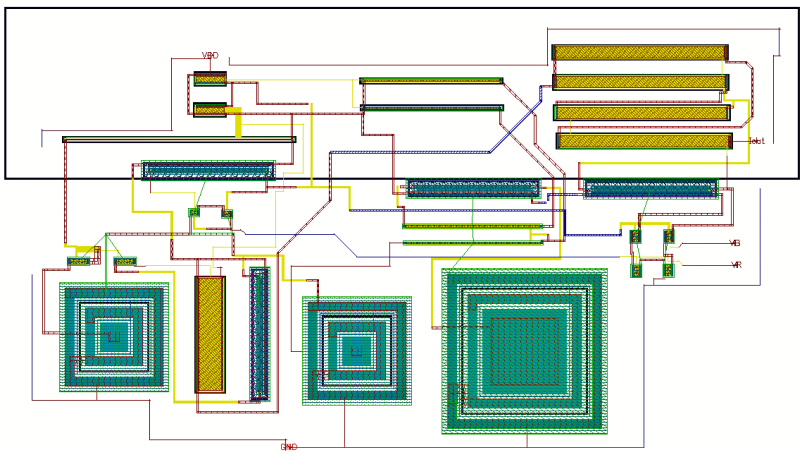


Figure 4.16. Layout of bandgap reference circuit

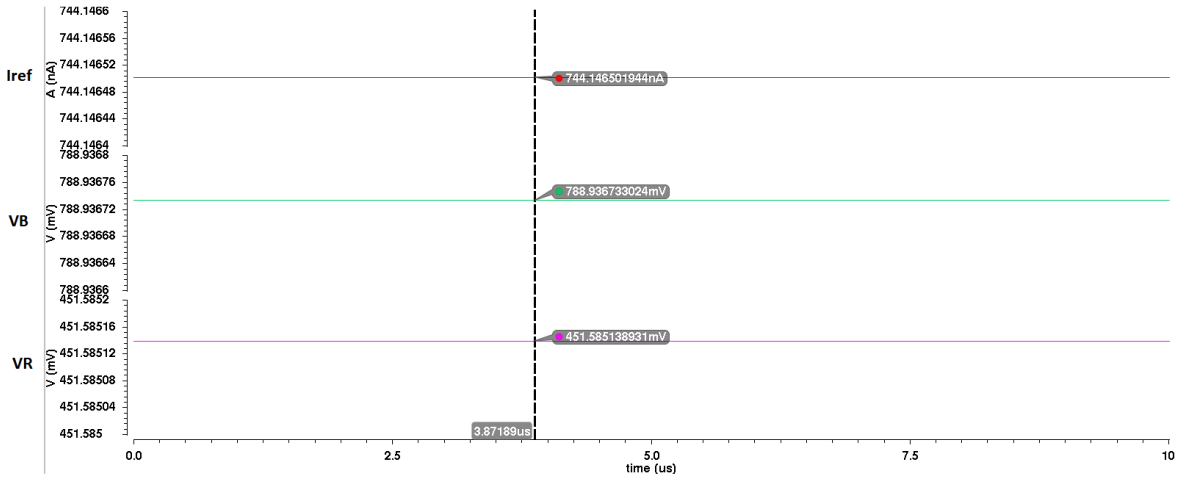


Figure 4.17. Post-Layout simulation of bandgap reference circuit

Since the BDAC is a very large circuit, its layout involves many blocks and interconnect wires. Thus, it is more difficult to draw the layout of the BDAC. A problem that could not be solved occurred in the layout stage. Therefore, post-layout simulation of the BDAC does not give reasonable results to present here, only the drawn layout is presented in Figure 4.18.

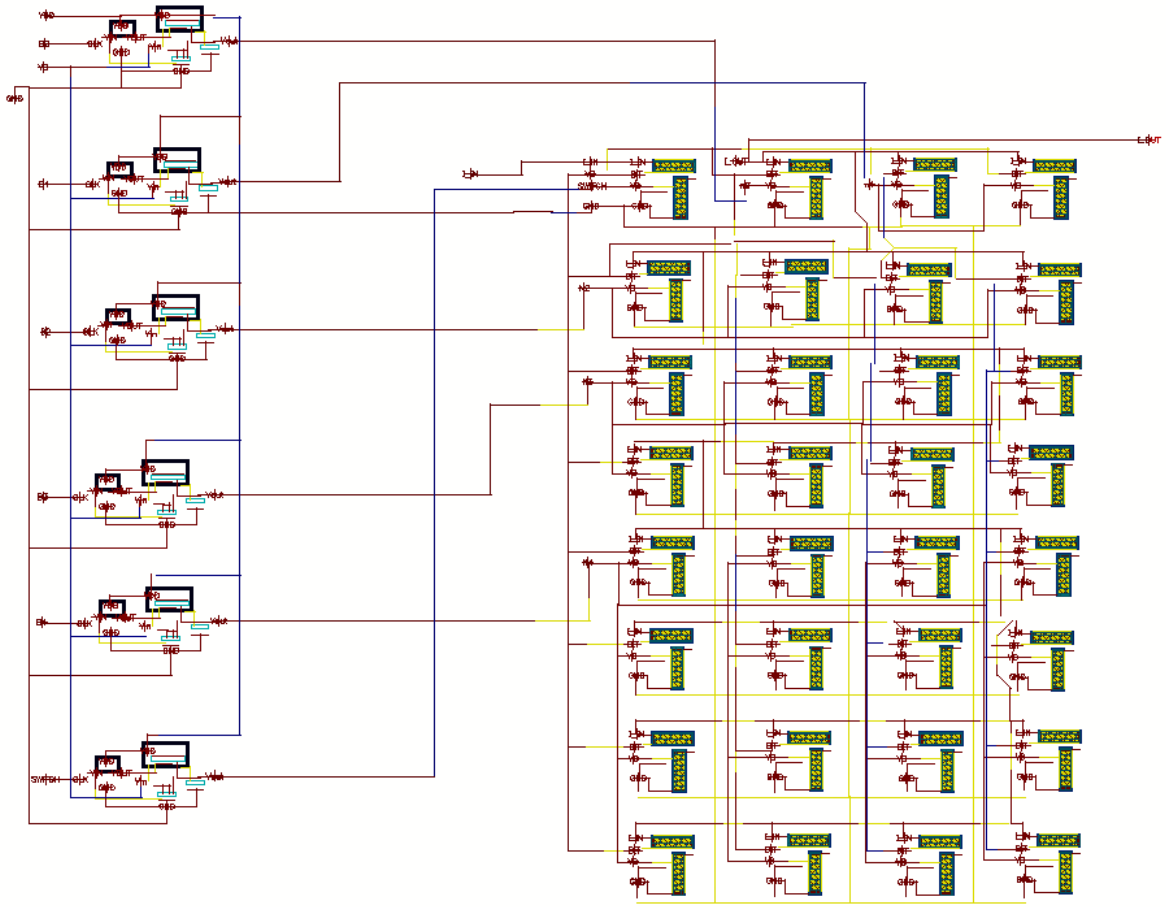


Figure 4.18. Layout of BDAC circuit

5. CONCLUSION AND FUTURE WORK

As a conclusion, a configurable interface for analog sensor outputs has been designed in UMC 130nm technology. Chopping topology has been used to remove low frequency offset and noise. Three types of fully differential filters have been designed and connected to the output of the chopping amplifier to obtain a clean signal. Filters and amplifiers are tuned by biasing current supplied from biasing digital to analog converter. The proposed design is self biased so that all biasing voltages and currents are generated by a bandgap reference circuit. Operating frequency range is up to 15kHz while designed filters can operate in a wider range. 1/f noise, drift and offset voltage up to 10mV can be removed by proposed design.

To remove offset more than the proposed design is capable of, there are advanced and nested chopping topologies and topologies that combine chopping and autozeroing. Using advanced topologies may give better results. Moreover, tunability of filters can be increased by matching them perfectly and using different linearization techniques. Moreover, f_{chop} can be tunable. Resolution of BDAC has a trade off. Increasing the number of digital input gives more resolution. However, increasing resolution will generate small current values which will be under the noise floor and will not give reliable results.

Digital signal processing is an important method to read and evaluate analog sensor outputs. A configurable analog sensor interface circuit with analog to digital converter can transform the design into a analog input - digital output topology. To process signals obtained from analog sensors, an ADC is required for DSP applications in FPGA or other environments.

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