WATER-GATED FIELD EFFECT TRANSISTOR WITH INTEGRATED MICROFLUIDIC CHANNEL

by

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ABSTRACT

WATER-GATED FIELD EFFECT TRANSISTOR WITH INTEGRATED MICROFLUIDIC CHANNEL

This thesis establishes a novel fabrication method to integrate water-gated transistors with microfluidic channels using surface micromachining techniques. Transistors are designed and fabricated on 16 nm thick single crystalline silicon films of silicon on insulator (SOI) wafers. After fabrication, I_D vs V_{DS} characteristic is tested to prove that device is operational. To fabricate the device, thin film silicon is patterned to create channel region of the transistor. Then, 200 nm thick aluminum is evaporated to form source and drain contacts. Thermal annealing is applied to establish ohmic contacts between silicon and aluminum of the source and drain electrodes. To create microfluidic channel, device is covered with sacrificial photo-resist with standard lithography. To form the gate electrode, aluminum is thermally evaporated on top of sacrificial photoresist which is on channel region using shadow mask technique. After the device's surface is activated with oxygen plasma, 5 mm thick PDMS is casted and cured. Reservoir holes and contacts are obtained by punching holes in those regions through PDMS layer. Finally, microfluidic channel is released by acetone injected inside reservoirs to remove photoresist. Device is tested after the microfluidic channel is filled with DI-water, which forms the electrical double layer on surface of the channel region to create gate capacitance which is necessary to operate the transistor. Transistor's characterization is made between 0 and -0.8 V which is the region water operates without any ionization. Maximum output current obtained is 900 μA with 60 W/L ratio and ON/OFF ratio of 22 with threshold voltage of -0.4 V.

ÖZET

SU KAPILI TRANSİZTÖRLERİN MİKRO-AKIŞKAN KANALLAR İLE TÜMLEŞTİRİLMESİ

Bu tezde su kapılı transiztörlerin mikroakışkan kanallar ile tümleştirilmesi için yenilikçi üretim metodları anlatılmaktadır. Transiztörler yalıtkan üzeri silisyum pullar üzerinde 16 nm kalınlığındaki tek kristal silisyum filmler şekillendirilerek üretilmiştir. Üretimden sonra savak akımları savak-kaynak gerilimine göre ölçülerek üretilen cihazın çalıştığı kanıtlanmıştır. Cihazın üretiminde, ince film silisyum transiztörün kanalını oluşturması için şekillendirilmiştir. Sonrasında, 200 nm aluminyum kaynak ve savak elektrodlarını oluşturması için buharlaştırılmıştır. Tavlama yöntemiyle aluminyum ile silisyumun ohmik kontakt oluşturması sağlanmıştır. Mikroakışkan kanalın oluşturulması için, geçici katman olarak fotorezist şekillendirilmiştir. Kapı elektrodunun oluşturulması için, aluminyum gölge maskesi tekniği ile geçici fotorezist katman üzerine buharlaştırılmıştır. Cihazın yüzeyi oksijen plazma ile aktifleştirildikten sonra 5 mm kalınlığındaki PDMS kaplanarak sertleştirilmiştir. Rezervuar boşlukları PDMS üzerinden delinerek oluşturulmuştur ve geçici fotorezist katmanı aseton ile temizlenmiştir. Test edilmesi için cihaz kanallarına deiyonize su enjekte edilmiştir, bu şekilde transiztör kanal yüzeyinde elektriksel çift katman oluşturulmuştur. Elektriksel çift katman transiztörün çalıştırılması için gereken kapasitenin oluşmasını sağlamıştır. Transiztör 0 ve -0.8 V arasında karakterize edilmiştir. W/L oranı 60, eşik voltajı -0.4 V olan transiztörün maksimum çıkış akımı 900 μA, açma kapama oranı 22 olarak ölçülmüştür.

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LIST OF SYMBOLS

Al	Aluminum
C_d	Diffuse layer capacitance
C_{dl}	Electrical double layer capacitance
C_h	Helmholtz layer capacitance
H_2O	Water
HNO_3	Nitric acid
I_D	Drain current
k	Boltzmann constant
L	Length of the transistor channel
L	Characteristic Length
n^0	Ion concentration
q	Electron charge
Re	Reynolds number
Si	Silicon
SiO_2	Silicon dioxide
T	Absolute temperature
u	Fluid velocity
V_{DS}	Drain-source voltage
V_{GSeff}	Effective gate-source voltage
V_T	Threshold voltage
W	Width of the transistor channel
z	Signed charge
ε	Dielectric constant
ε_0	Dielectric constant of air
μ	Dynamic velocity
μ_p	Hole mobility
ν	Kinematic viscosity

ρ	Fluid density
σ^M	Charge density
ϕ_0	Surface potential

LIST OF ACRONYMS/ABBREVIATIONS

3D	Three dimensional
BioFED	Bio-field effect device
CMOS	Complementary metal oxide semiconductor
CVD	Chemical vapor deposition
DI	Deionized
EG-FET	Electrolyte-gated field effect transistor
IC	Integrated circuit
IPA	Isopropyl alcohol
LAPS	Light-addressable potentiometric sensor
MAGFET	Magnetic field effect transistor
MEMS	Microelectromechanical systems
MOSFET	Metal-oxide-semiconductor field effect transistor
PDMS	Polydimethylsiloxane
PR	Photoresist
RPM	Rounds per minute
RTP	Rapid thermal processing system
SOI	Silicon on insulator
SMU	Source measurement unit
UV	Ultra violet
WG-FET	Water-gated field effect transistor

1. INTRODUCTION

Microfabrication technologies revolutionized the electrical engineering and computer science. Millions transistors are compressed and wired into very small chips which are used for incredibly fast computation and communication, requiring very little power to operate. This industrial revolution enabled production of complex systems in very small devices, which can be used by billions of people, everyday.

Advancements in microfabrication technologies also caused other sciences to emerge. One of these sciences is Micro-electro-mechanical systems (MEMS). Utilizing microfabrication techniques, MEMS builds structures which can be used to create sensors and actuators in very small scales. Being an interdisciplinary profession, MEMS techniques require the knowledge of electrical engineering, mechanical engineering and great knowledge in material science. This enables the integration of 3D structures integrated with analog and digital systems in very small scale.

Techniques established by MEMS fabrication lead to experimentations with different materials, different transistor structures, layers of different chemical properties, also integration with different physical blocks. One of these experiments are conducted on the interface between electrodes and electrolytes. By modifying the traditional metal-oxide semiconductor (MOSFET), new field effect devices are emerged, like ion sensitive field effect transistors (ISFETs) [1], electrolyte gated field effect transistors (EG-FETs) or bio-field effect devices (BioFEDs). These devices build upon the interactions between ions near material surface.

Water-gated field effect transistor (WG-FET) is a concept emerged from the idea of utilizing electrolytes as the gate electrode. Main working principle of the field effect transistor builds on electrical double layer, which is formed when a substrate contacts with water and draws ions on its surface. This double layer produces a capacitance, which can be used for inducing channel with electrical field. This field accumulates holes or electrons, depending type of the semiconductor and allows current to be modulated

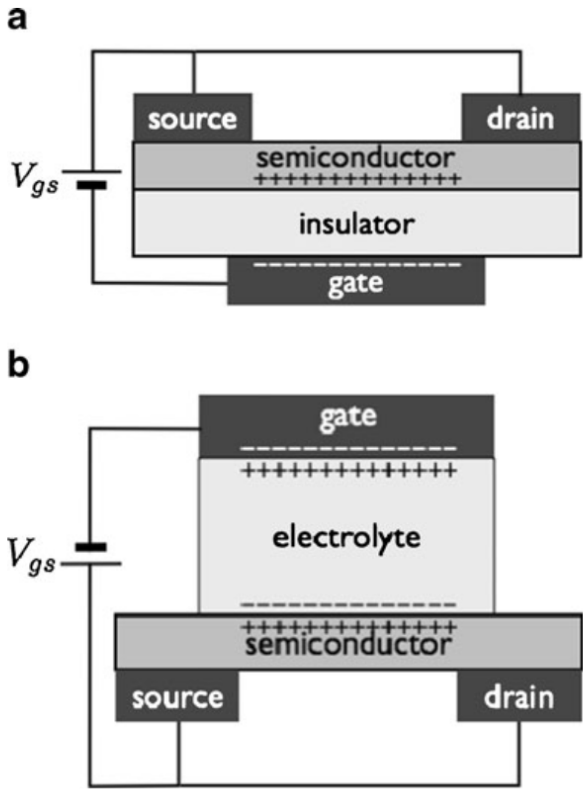

Figure 1.1. a) MOSFET vs b) EG-FET [2]

with changing gate voltages. With working by utilizing liquids, it is rational to think that creating a container environment for those liquids has importance to create reliable devices.

Microfluidics are the techniques which produces systems in order to manipulate liquids, guiding them or small molecules inside liquids, mixing or pumping them in the microfluidic channels which are micrometer in size [3]. Most of the science which is built on chemistry, is useful in biological analysis. It is also a very powerful tool to apply chemical synthesis, very small amounts of liquids which can be controlled by volume increases the accuracy of obtaining products [4]. To achieve chemical reactors, there are several techniques introduced, like electro-osmotic pumping or hydrodynamics [5]. Accurate manipulation of liquids also opened the path to fields which utilize electrical contacts with liquids, like Digital Microfluidics(DMF) [6].

Microfluidic integration of transistors have been achieved by several methods before. A fabrication method includes building microfluidic channel structure by chemical etching of silicon with KOH [7]. Another unconventional method is to form electrodes with liquid mercury that is transported with PDMS microfluidic channels on organic semiconductor with control, which aims to adjust channel length by adjusting volume of the pumped mercury contacting semiconductor [8]. Also a IC/Fludic channel hybrid system is studied, which integrated coils are embedded inside microfluidic channel to trap cells [9]. Embedding a CMOS chip for PDMS microfluidic packaging is studied by bonding glass cover for Lab on a chip devices [10]. One of the applications of microfluidic integration of integrated circuits (IC)s is to measure nanoparticles with magnetic field effect transistors (MAGFET) combined with CMOS IC. This study also shows that liquid mercury can be used to obtain electrical contacts in the package and have a flexible package with PDMS package [11].

Moreover, Bio FEDs(Field Effect Devices) which are used to analyze different types of biological structures. LAPS, En-FETs (light-addressable potentiometric sensor) are some of the devices which forms an example of BioFEDs [12]. They mostly work to have analyte inside electrolyte, which forms chemical reactions deposited on channel region of the proposed device. Electrical characteristics indicate the existence of those analytes.

One of the most popular materials used in microfluidic applications is Polydimethysiloxane (PDMS). PDMS has a lot of properties to be used in microfluidic channel applications. Its flexible structure can be utilized to build microfluic valves or pumps, which cannot be possible with rigid materials like glass or silicon. Also it is transparent, which is beneficial for optic applications, and eases observation of fluids. PDMS is permeable to gases and non-toxic, therefore it is compatible for biomedical research. Also its fluidic nature allows it to form complex structures on molds with high resolution, which does not require any chemical or physical etching processes. Its surface is naturally hydrophobic, but can be changed to hydrophilic with modifying with plasma treatment [13].

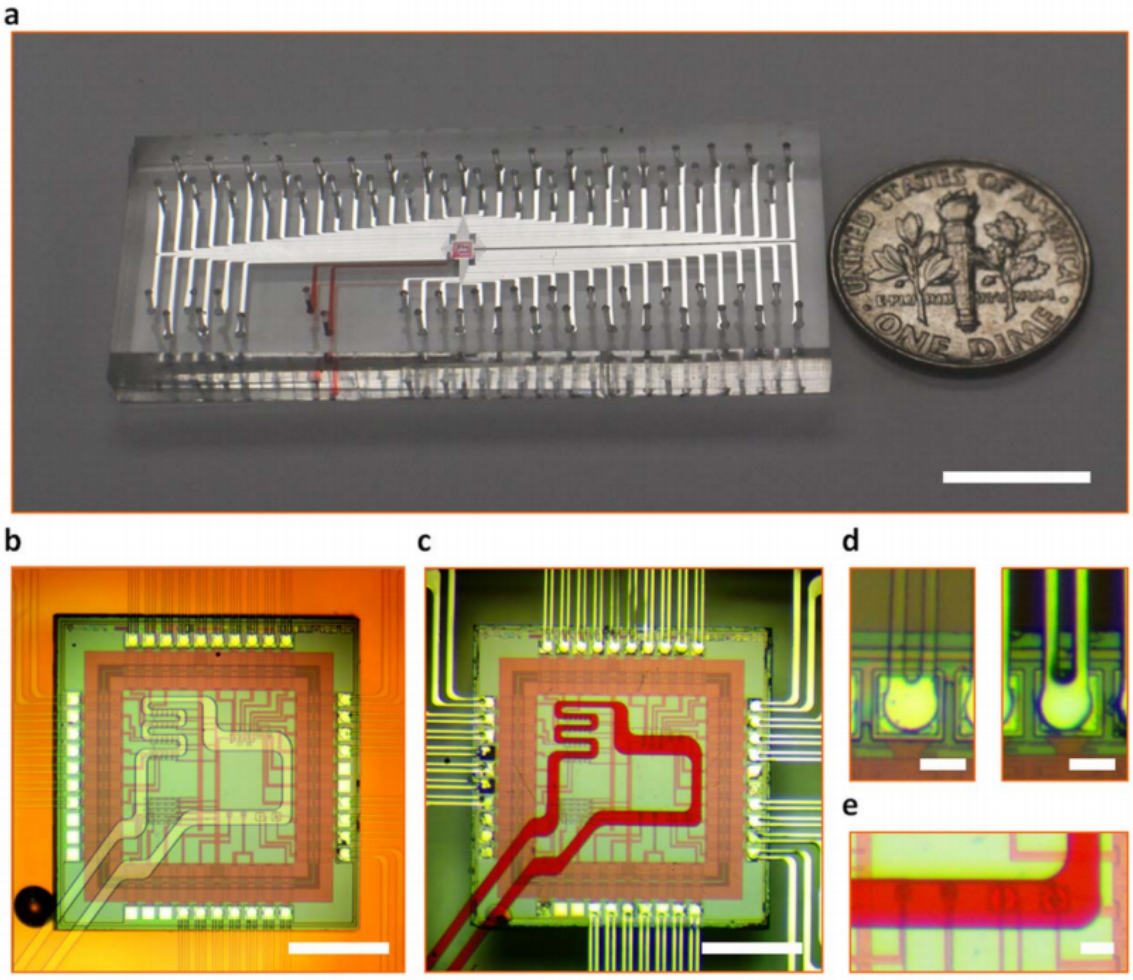

Figure 1.2. Microfluidic integrated CMOS hybrid chip with liquid interconnects. [11]

To be able to integrate multiple WG-FETs in a single chip, it is necessary to have a containable liquid. Most of the work done with Water-Gated Field Effect Transistors are conducted on water droplets [14–16]. Although multiple water droplets can be used to build multiple transistor circuits, liquid containment is also necessary for further scaling because of accurate control of water droplets and prevention of evaporation. Microfluidic channel integration lays foundation of IC chips in water gated transistors, which also makes able to design more accurate chips with the knowledge of volume of liquids and accurately controlled gate structure.

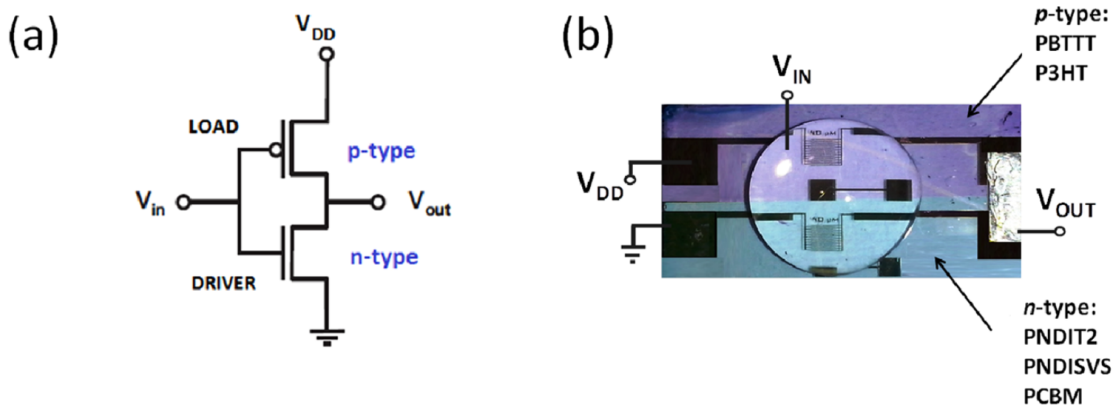

Figure 1.3. Integrated inverter with organic WG-FETs [17].

1.1. Motivation and Novelty

WG-FET devices which utilize 16 nm thick single crystalline silicon film as active layer was reported before [16]. So far, these devices are fabricated and tested by manually placing a droplet of water onto its active region. Furthermore, it is shown that these devices perform best when a top probe gate is inserted to the water droplet, vertically above its active region. These present fabrication challenges, which must be overcome to achieve their large scale integration since they are to be used as both sensors and read-out circuits on a lab-on-a-chip platform. Hence, this work presents for the first time a WG-FET device integrated to a microfluidic channel and surface micromachined top gate electrode. PDMS microfluidic channels and hanging top gate electrode are formed using surface micro machining methods. Microfluidic channels are fabricated without any bonding procedure. This allows to use high accuracy alignment with PDMS channels without any high-tech alignment system for bonding. This work forms the top gate electrode by using an aligned shadow mask on top of the sacrificial photoresist layer while evaporating thin aluminum film, unlike other works where gate electrode is formed on another substrate first and then bonded [18].

1.2. Outline of the Thesis

In the first chapter, the concepts of water-gated transistors and microfluidics are introduced, and importance of microfluic channel integration is indicated. Previous work about microfluidic channels, usage of PDMS, and electronic integration with microfluidic channels are mentioned related to this thesis.

In the second chapter, the theory and mechanics in the microfluidics and water gated transistors will be described extensively. Electrical double layer will be explained, and transistor model will be described.

In the third chapter, structure of the fabricated device will be presented. Fabrication of the microfluidic integrated WG-FET will be described step by step.

In the fourth chapter, methods on building test setup will be described and experimental results of the fabricated device will be discussed.

In the fifth chapter, conclusions and possible future work will be investigated.

2. FUNDAMENTAL THEORIES

2.1. Electrical Double Layer

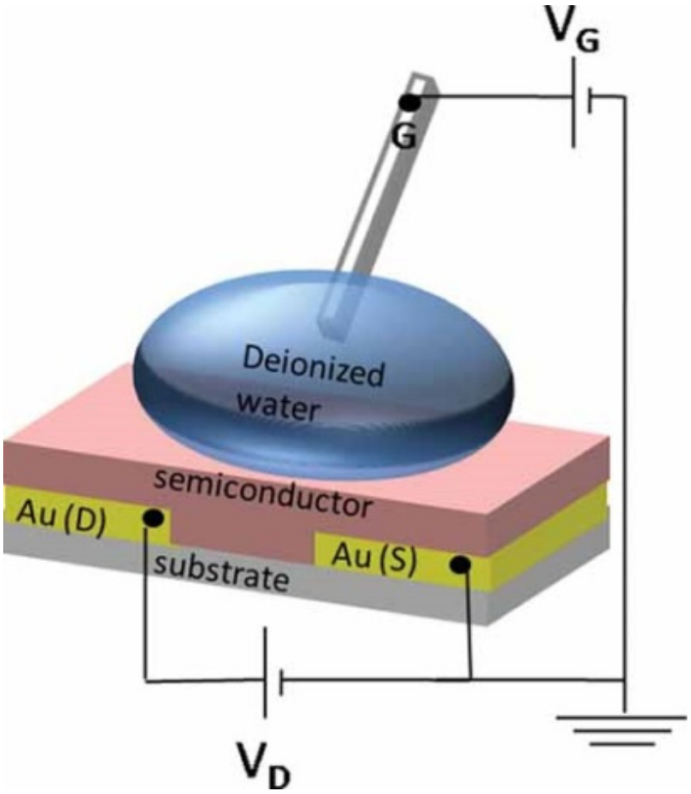

Figure 2.1. WG-FET with probe gate [15].

To understand WG-FET, we should understand the physical phenomena causing the field effect which is used to accumulate charge for altering the current of the transistor. Electrical double layer is a structure which occurs because of attraction of ions when a material has contact with a liquid. If a potential is applied to material, (in this case, it is Al and Si) charged surface draw the opposite charged ions inside liquid, which forms a layer. This layer is anchored to the surface of material, by chemical interactions. A second layer also forms because of coulomb forces which forms a high

density of those ions. This second layer's ions are not bonded to surface of material, which means they can move in presence of an electric field. Also the charge density of those ions exponentially drop until the end of this second "diffuse" layer.

This model is developed with the foundation of Helmholtz, which present the attraction of those liquid electrolyte ions to surface of materials in his article in 1853 [19]. This model includes the effect of potential applied to material, but does not take into account of ion concentration inside liquid. Stern's approach explains this phenomena in more detail, adding a second layer to next of Helmholtz to explain charge density at the surface [20]. This model is further improved by Grahame, which includes multiple Helmholtz layers because of the opposite charges solvated inside the diffuse layer, which alters the potential characteristic [21].

Apart from Helmholtz model, every other theory indicates ion concentration's effect on the electrical double layer. This is reasonable, as diffuse layer is consisted of free moving ions, having more ions indicate thick layers. Thick layer points out larger electrical double layer capacitance. As this capacitance is an analogy to the oxide capacitance in MOSFETs, having larger capacitance creates larger currents, because more charge can be accumulated near surface of the channel. Electrical double layer has other dependencies, like temperature and electrostatic potential of the surface.

The relationship between electrical double layer capacitance and ion concentration is shown in Equation 2.1 [22]. σ^M is charge density, z is signed charge, q is electron charge, ε is dielectric constant of electrolyte, ε_0 is dielectric constant of air, k is Boltzmann constant, T is absolute temperature, ϕ_0 is surface potential, n^0 is ion concentration.

$$C_d = \frac{d\sigma^M}{d\phi_0} = \sqrt{\frac{2z^2q^2\varepsilon\varepsilon_0 n^0}{kT}} cosh \frac{zq\phi_0}{2kT} \tag{2.1}$$

This equation is derived from Gouy-Chapman model, which focuses on diffuse layer instead of Helmholtz layer. This approach fits for WG-FETs, because electrical

double layer consists of two capacitances: C_h and C_d, Helmholtz layer capacitance and diffuse layer capacitance. This capacitances are connected in series, which means larger capacitance can be neglected. Since the charge accumulated on the surface of the material at the Helmholtz plane is much larger than the diffuse layer, Helmholtz capacitance can be neglected in this model.

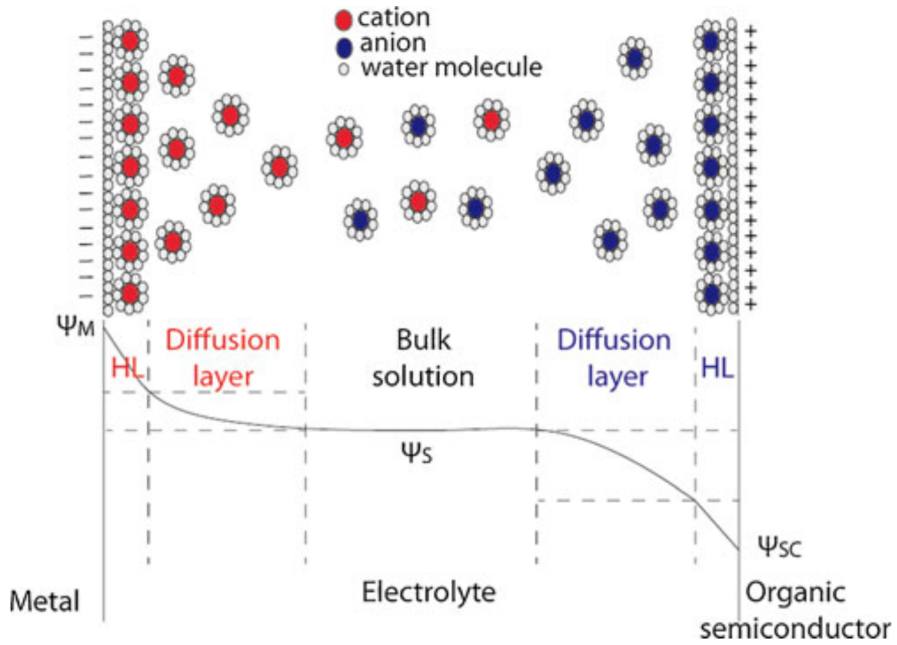

Figure 2.2. Representation of electrical double layer at the interfaces of semiconductor and gate electrode. [2]

2.1.1. WG-FET

A WG-FET device schematic can be seen in Figure 2.1 [15]. Although WG-FET device operates like MOSFET. It has a linear, saturation and cut-off regions. This thesis focuses to build transistor without doping processes. Without doping, junctions at the source and drain electrodes won't exist. This means that inversion is not a possible working scenario for the transistor. Therefore, WG-FET presented in this thesis operates with accumulation instead of inversion. This has few drawbacks. Since there are no p-n junctions, there is a high possibility to have high off currents between

source and drain electrodes. Moreover, from integration perspective, it is susceptible to current leakage if devices are positioned closely.

Current between source and drain electrodes can be calculated with Equation 2.2, which is similar to MOSFET version. I_{DS} is the drain current, μ_p is the hole mobility inside thin film silicon, C_{dl} is the electrical double layer capacitance. V_{GSeff} denotes the potential difference between gate and source electrode effecting the channel. Since there are multiple double layers connected in series inside the model, V_{GS} voltage cannot be directly included in the equation like MOSFET counterpart. V_T denotes the threshold voltage, which indicates the voltage the transistor starts to work with accumulation.

$$I_D = \frac{1}{2}\mu_p C_{dl}\frac{W}{L}(V_{GSeff} - V_T)^2 \tag{2.2}$$

2.1.2. Microfluidic Channels

Microfluidic science is somehow projected from the microfabrication of integrated circuit technology. Being able to integrate multiple mixing, synthesizing features in a small chip with very small amount of liquid, like being able to integrate too many transistors which can operate at the same time makes this part of science very popular. As fabrication technologies are borrowed from micro-fabrication like lithography, modeling of the devices also became similar. All these applications are possible because when the dimensions of the channels get smaller, physics of the transportation of liquids change. Different flow regimes starts to occur, which we don't notice in our everyday lives.

One of those regimes is called as laminar flow. This flow regime indicates that fluids inside microfluidic channel moves straight-forward. This means liquid won't mix with other liquids during the flow. To understand if the flow of the corresponding liquid is laminar, one important parameter, Reynold's number should be calculated. Reynold's number is a parameter which shows the dominating force inside a channel comparing between inertial or viscous forces.

Reynolds number can be calculated with Equation 2.3. ρ denotes fluid density, u denotes velocity of the fluid, L denotes characteristic length, which can be interpreted as the smallest dimension that fluid travels. μ denotes dynamic viscosity.ν denotes kinematic viscosity of the fluid which is equal to μ/ρ. If Reynolds number is smaller than 2000, it can be assumed that viscous forces dominate and flow becomes laminar [23]. On the other hand, if it is larger than 2000, it can be interpreted as inertial forces have considerable effect, which means flow starts to become turbulent, and it is susceptible to mixing.

$$\mathrm{Re} = \frac{\rho u L}{\mu} = \frac{u L}{\nu} \tag{2.3}$$

For this thesis, fluid dynamics are not relevant because transistor utilizes static DI water inside the channel. However, because of electrical double layer, movement of ions can be observed if electrical field is applied through microfluidic channel. This allows the usage of electro-osmatic pumping, which can be an effective mechanic if multiple transistors are placed inside a single chip. Therefore, it is important to design microfluidic channels with low Reynold's numbers, to create a straight path for flow.

3. FABRICATION OF THE DEVICE

3.1. Structure of The Fabricated Device

This thesis is an extension of the work presented in [16]. Their study revealed the performance of WG-FETs built with 16 nm thick single crystalline silicon film, in two types of designs, top gate electrode and planar gate electrode. Their top gate structure is established by placing a probe. Alternatively, they placed a planar gate electrode near active area of transistor. These two designs both work with water droplets. Although planar gate transistor can be used for microfluidic channel integration, output currents of the device is relatively low compared to top gate structure. Also planar structure complicates the microfluidic channel integration process, with increasing the width of the channel which makes it susceptible to collapsing.

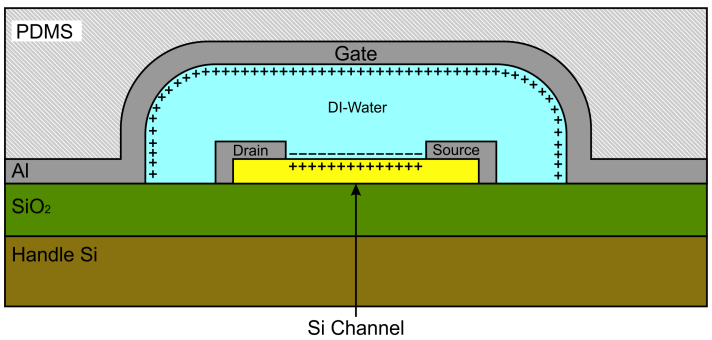

Figure 3.1. Cross-section sketch of the fabricated device.

Sketches of the cross-section of proposed devices shown in Figure 3.1. Device is built on silicon on insulator wafer, which allows us to utilize 16 nm silicon film. By etching the silicon, active area of the transistor can be patterned. Channel length obtained by this procedure is 50 μm. SiO_2 of the wafer creates insulation between source, drain electrodes and other transistors which can be fabricated in the same chip. On top of active layer, 200nm thick, 40 μm wide Al contacts are placed to obtain source and drain electrodes. Microfluidic channel is 200 μm in width, 15 μm in height. Top gate electrodes cover the microfluidic channel in transistor channel region, which

is 200 μm in thickness. PDMS casted on device is 5 mm thick, which allows support for microfluidic channel and contact wires.

With 3000 μm width and 50 μm length, W/L ratio of the WG-FET is calculated as 60. This transistor has smaller features from the previous work, which is preferred for microfluidic channel integration.

It is described in [24] that insulator layer increases reusability of the transistor . Although insulator layers could not be applied to source and drain electrodes due to already used photoresist in sacrificial layer for the microfluidic channel, other regions are covered with PDMS which provides insulation.

3.2. SOI Dicing

12 Inch SOI wafers are diced to create samples for prototyping. SOI wafers used in this thesis is obtained from Soitec. Their smart-cut technology makes thin-film silicon available. To obtain SOI wafers, a doped silicon is thermally oxidized to grow buried oxide layer. Then hydrogen implantation is applied to wafer, creating a weak line to cut silicon. After this procedure, another silicon wafer bonded to this structure. The first wafer is split from the thin film line, leaving with a silicon-on-insulator wafer. Wafer has a 16 nm thin film silicon layer, with a 145 nm buried oxide layer, and 775 μm handle silicon.

In traditional CMOS process, multiple chips are fabricated into a wafer and diced after the fabrication. This allows a robust fabrication and enables mass production in semiconductor industry. In this case, SOI wafers are diced before fabrication to test instances without wasting a wafer for a single trial. Dimensions for each produced sample is 2.5 cm to 2 cm.

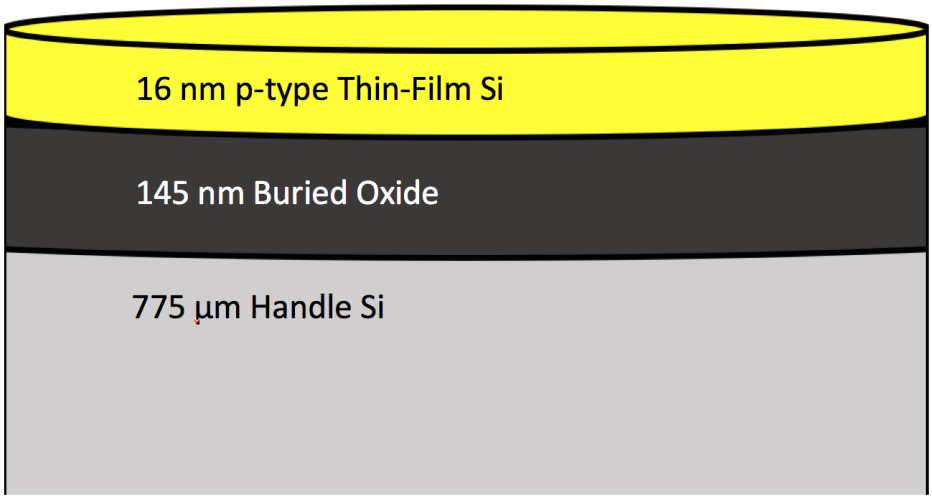

Figure 3.2. Sketch of SOI wafer.

3.3. Photolithography

For applying thin film photoresist to each sample, spin coating technique is used. Spin coating is a practice seen in microelectronics industry to pattern each layer to fabricate chips [25]. Microposit PR 1828 is used for SOI and Aluminum etching processes, AZ9260 is used for creating sacrificial layer for microfluidic channel. Alignment resolution is set to 20 μm, and with aluminum contacts and channel length which is 50 μm, which makes the possible largest active length to 150 μm. For compensating any alignment errors, 200 μm active length is sufficient for channel and a working transistor.

After thin film photoresist is applied on the surface of substrate, litography is initiated to achieve desired pattern on thin film silicon. Positive photoresist is used for this work, which means the masking pattern is transferred to produce the photoresist pattern. After UV is applied, obtained pattern is developed and hard baked to remove any remained solvents inside photoresist to prevent etching of masking film by the etchants of Si. Then the thin film silicon is patterned with "Trilogy Etch" ($126HNO_3$:$60H_2O$:$5NH_4F$) [26]. Masking photoresist film is then removed with ace-

tone and sample is cleaned for further processing.

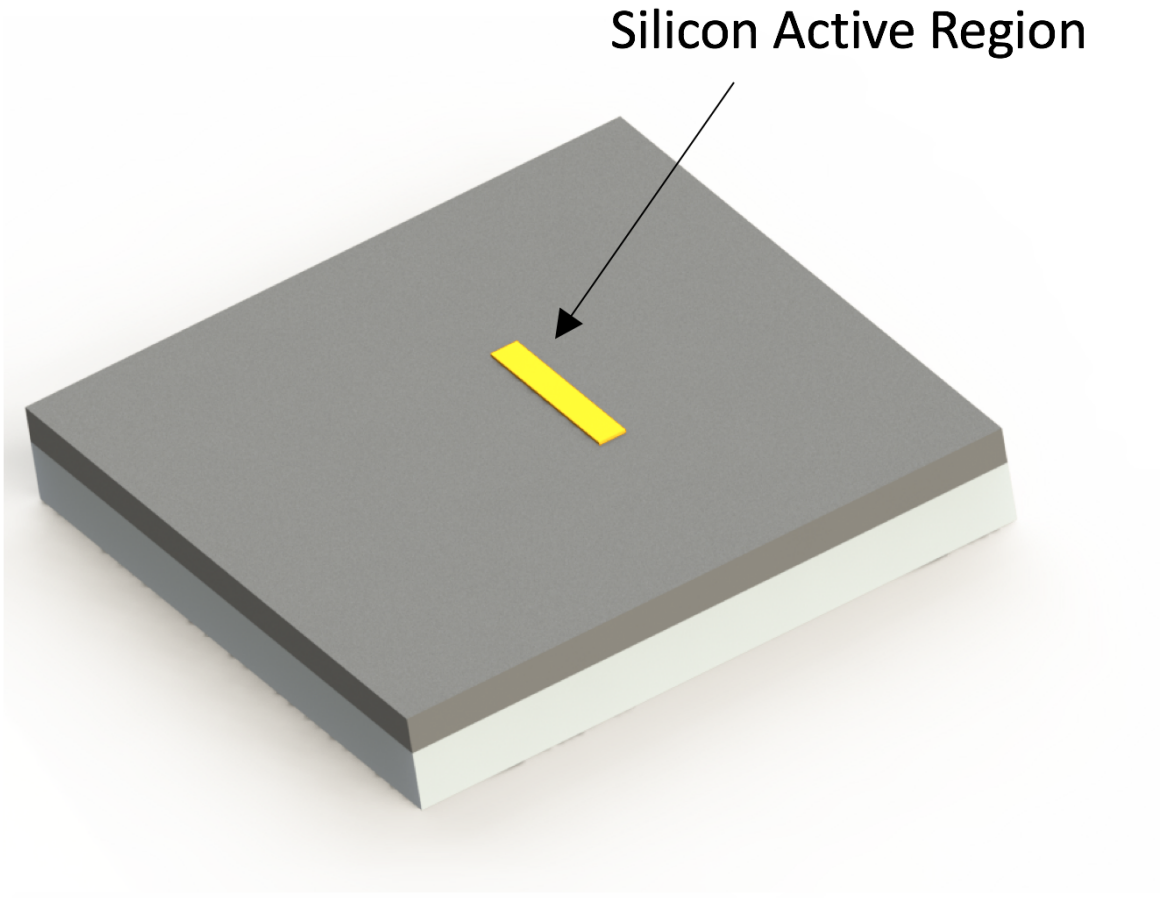

Figure 3.3. Device after patterning of 16 nm thick Si.

3.4. Thermal Evaporation of Al

Thermal evaporation is a procedure to increase the temperature of the coating material and guide it to the surface of substrate. It is necessary to obtain a vacuum environment to increase mean-free path of metal particles to be coated, which decreases the chance to have a chemical reaction before reaching the target, thus achieving contaminant-free coating. Procedure is conducted by applying high currents to a electrically conductive basket, which heats the metal inside this basket to the point of evaporation.

With 5 x 10^{-6} Torr vacuum pressure, 200 nm Al is coated on the device with a 0.5 g Al slug inside a tungsten basket.

3.5. Patterning Source and Drain Electrodes

After thin film Al is coated, photoresist is applied on the surface of substrate. Photoresist is patterned to cover aluminum electrode regions. Usual development time of photoresist takes 1 minute but the developer which is used to pattern photoresist is an etchant for Al. This allows patterning Al with increasing development time. Development approximately takes 15 minutes.

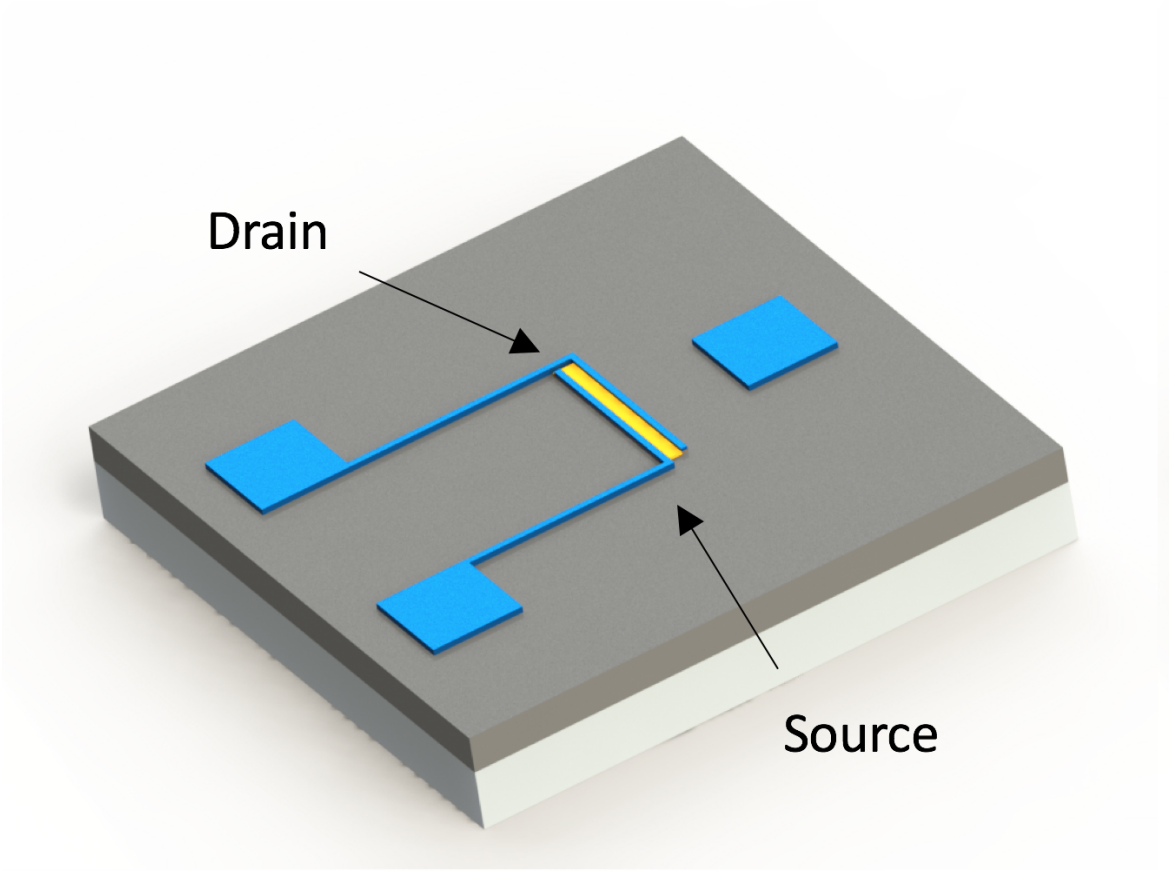

Figure 3.4. Device after patterning of 200 nm thick Al.

Micrograph of the structure can be seen in Figure 3.5. Since dimensions of the lengths are crucial to obtain a stable microfluidic channel, alignment of the electrodes

and thin film Si becomes a challenge with smaller dimensions.

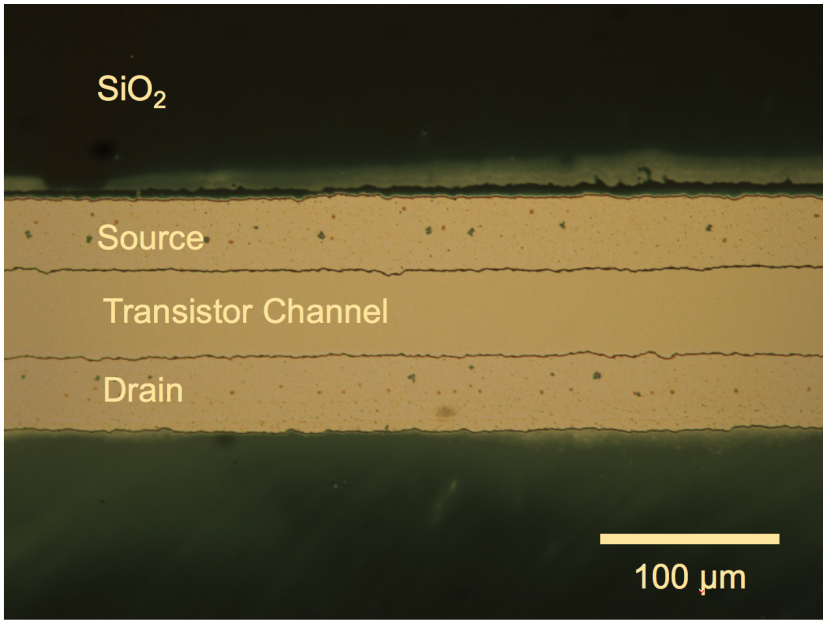

Figure 3.5. Micrograph of the device after Al patterning.

3.6. Thermal Annealing

When aluminum is applied to surface of Si, it is necessary for an annealing step to achieve ohmic contact. For this process, rapid thermal processing (RTP) system is used for the produce necessary conditions. For thermal annealing, substrate is heated in a controlled environment to diffuse Al atoms into silicon. The heat treatment is made with halogen lamps in a vacuum environment with a root gas presence in order to prevent any oxidation on Al during the process.

Root gas used in our procedure is Argon. In the process of thermal annealing, temperature is increased to 500 ^{0}C for 15 minutes with halogen lamps. After the procedure, chamber is slowly cooled down to room temperature.

After thermal annealing, device electrodes are tested if they have ohmic contact. Source and drain regions are connected to Kietley characterization system and resistive measurement is made between those electrodes. If current values show linear charac-

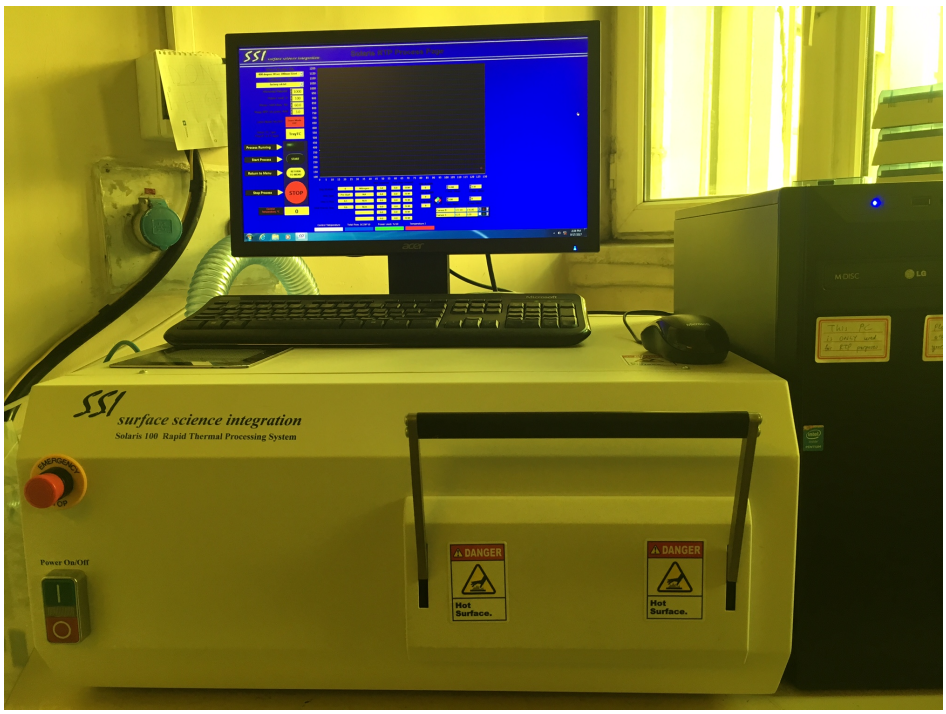

Figure 3.6. RTP system.

teristic in the regions -1-1 V, it is accepted to have ohmic contact. If measurement shows diode characteristic, device is re-annealed until ohmic contact is formed.

At the end of this fabrication step, the transistor can be tested with, a probe gate and a water droplet.

3.7. Fabrication of Microfluidic Channel

Traditional PDMS microfluidic structures is built bonding PDMS to substrate. To achieve this, a mold is prepared on a silicon wafer by patterning SU-8 on top of it. Then PDMS elastomer is mixed with curing agent which is casted on the mold, either by pouring, or spin coating if an accurate thickness is desired in PDMS layer. PDMS is then cured with temperature around 70 ^{0}C, which allow it to form an elastic solid patterned by the mold. PDMS is then separated from the mold and reservoirs are opened by punching through PDMS. Obtained PDMS piece is plasma treated later, which activates the surface of PDMS and make it hydrophilic. This allows it to be

bonded to other materials, glass being the most common one. PDMS can be easily bonded by applying pressure, which makes it very easy for prototyping. This bond formed between PDMS and bulk substrate is permanent.

3.8. Sacrificial Photoresist Layer

In this work, the method established by Subramani will be used, which uses sacrificial photoresist layer to fabricate microfluidic channels. [27]. Since it is not easy to align PDMS structures for bonding, self alignment is preferable for controlling microfludic channel structure. Also it decreases the chance of leaking any liquid at the interface of source and drain electrodes because of the gaps which may form. Method prefers building a sacrificial photoresist layer to form fluidic channel region.

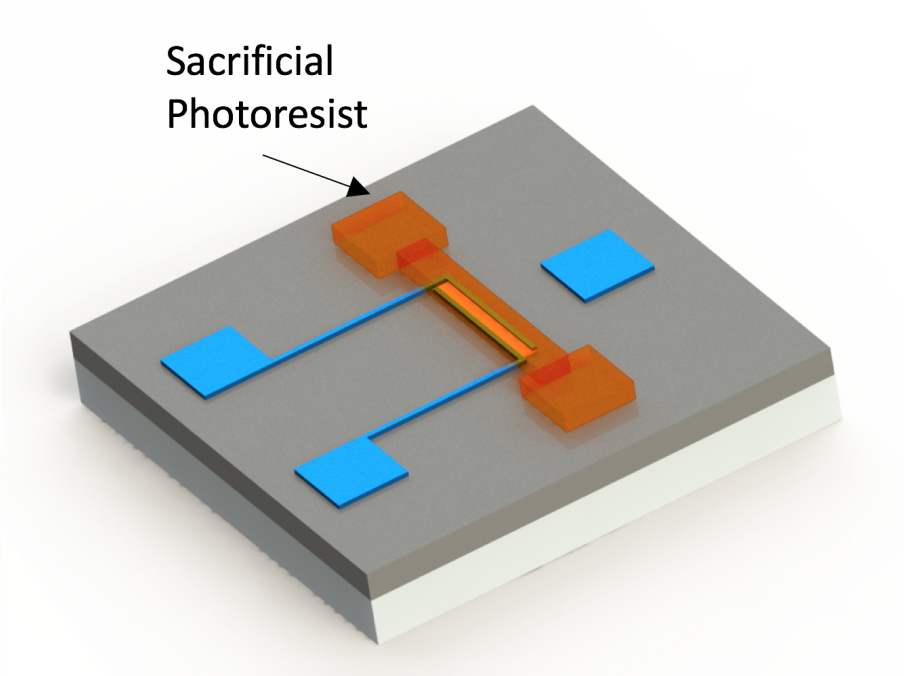

Figure 3.7. Device after patterning of 15 μm thick sacrificial photoresist.

This sacrificial layer is patterned with AZ 9260 photoresist, which is used for applications with thick structures. Multiple trials were made to obtain optimal channel thickness, aiming uniformity and larger thickness. With 500 RPM 1st coating step and 1200 RPM second coating step, a 15 μm thick photoresist is obtained. This structure

has larger soft-baking time with 20 minutes, which allows photoresist to spread uniformly on the surface of substrate. Spin-coated photoresist is then UV treated for 6 minutes 25 seconds under the pattern of microfluic-channel, then developed for 3 minutes. Obtained pattern is hard baked for 1 hours with 110 °C to remove any solvents before entering thermal evaporation to prevent contamination.

Micrograph of the device after patterning sacrificial photoresist can be seen in Figure 3.8. While in this fabrication section, it is important to cover all the active area and electrodes of the transistor. The next step includes evaporating Al on top of this layer. If there is a misalignment during patterning photoresist, evaporated Al may have contact with drain or source electrodes, which destroys the operation of device.

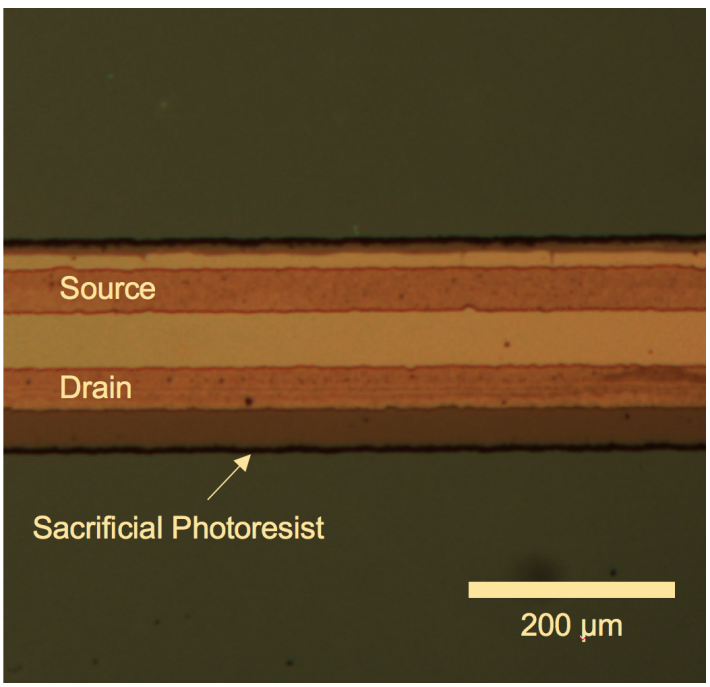

Figure 3.8. Micrograph of the device after patterning of 15 μm thick sacrificial photoresist.

3.9. Top Gate Aluminum Evaporation

A second Al evaporation is applied to surface of device, which form the top gate electrode of the transistor. To have a characteristic similar to top probe gate, a

suspending gate is necessary to form an even electric field on the channel. However, coating Aluminum is not possible without any masking, because evaporated Al would have contact with the previously evaporated aluminum, which is not desirable. Since photoresist is used as the sacrificial layer, it cannot be used as sacrificial layer to pattern aluminum again.

To overcome these fabrication challenges, shadow mask technique is used. To achieve shadow masking, substrate is covered with a masking layer without using a deposition technique. This mask can be made from aluminum or stainless steel films. For alignment and patterning, this mask can be patterned with lithography and electrochemically etched [28].

For prototyping, shadow masks are produced by hand cutting. Several length gates are produced, ranging from 200 μm to 1500 μm. Effects of gate lengths will be discussed later.

Aluminum film shadow masks are placed on top of each sample and fixed. 200 nm Al is thermally evaporated with a vacuum pressure of 5 x 10^{-6} Torr. Finally, mask is removed to obtain a gate line covering the sacrificial photoresist. This line is also used for having electrical contact.

Before testing with microfluic channels, it is investigated if this structure can suspend without having to attach another bulk material. Sacrificial layer is etched with acetone, releasing the top gate aluminum. However, the aluminum film is collapsed, proving to be structurally unstable because of being very thin.

3.10. Construction of Microfluidic Channel

There are several different materials which can be used in constructing microfluidic channels. PDMS being one of the popular options, stainless steel, silicon, glass, other polymers or even ceramics can be used to produce microfluidic channels [29].

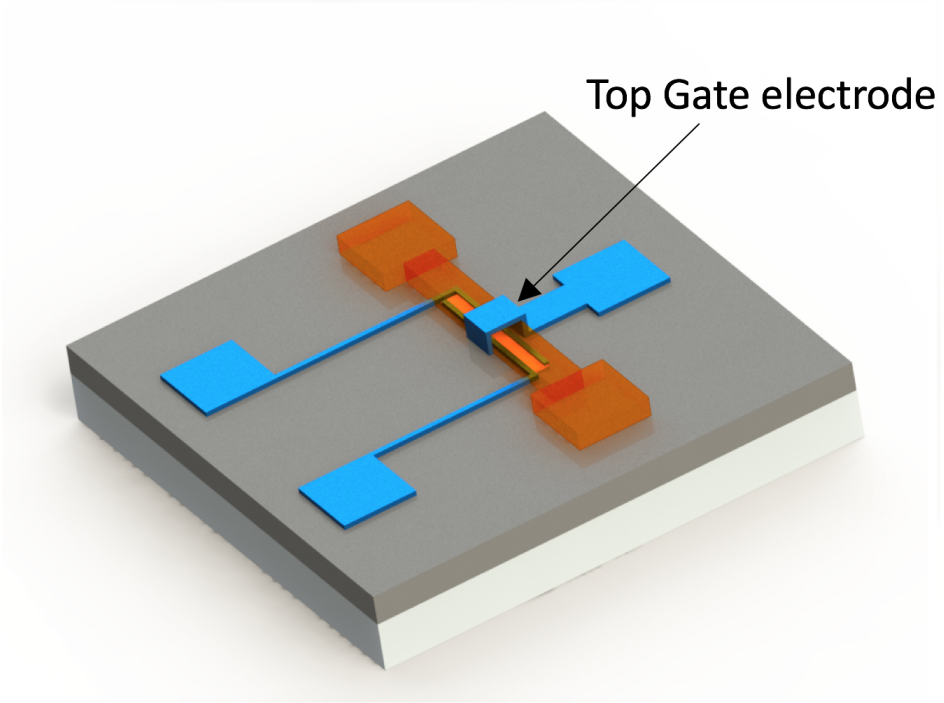

Figure 3.9. Device after 200 nm top gate Al is evaporated by shadow mask technique.

Parylene-C is also tested for producing microfluidic channels in this project. It is coated with chemical vapor deposition (CVD) [30], which is a popular method to achieve uniform coating in MEMS processes. Coating thickness was chosen 5 μm. Normally reservoirs can be opened by physically etching parylene with oxygen plasma, after masking it with a photoresist layer. For prototyping purposes, the reservoirs are opened with forcing needles. Microfluidic channels are formed after releasing the structure in acetone bath after a day, etching the sacrificial photoresist.

Micrograph of the final structure can be observed in figure. Although the structure could be released, it collapsed after acetone is evaporated. It is related to the aspect ratio of the microfluidic structure, which is approximately 10:1. Mechanical stress is too high for it to be stable, and since it is not an elastic material as PDMS, it cannot allow liquid forced inside. Microfluidic channel with smaller widths cannot be used because of the limitations on the alignment and photolitography processes. Smallest feature is chosen to be 40 μm, which is the width of aluminum electrodes.

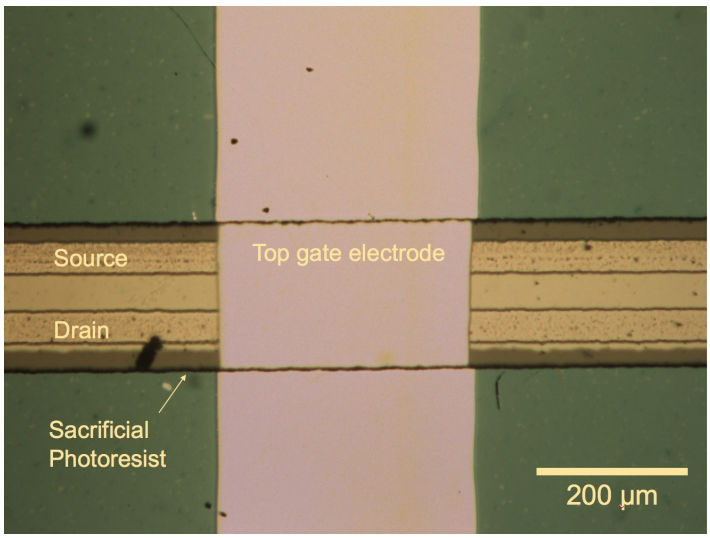

Figure 3.10. Micrograph of the device after 200 nm top gate Al is evaporated by shadow mask technique.

After testing parylene-C, PDMS microchannels are constructed. PDMS base is mixed with curing agent and blended. In Subramani's work, it is tested that higher cross-linker:base ratio achieves higher bonding strength on surfaces. 1:3 ratio gives the highest bond strength. Comparison of different mixing ratios can be seen in Figure 3.13 [27]. For the first trials, 1:10 cross-linker:base ratio is used, but because of poor adhesion, PDMS is easily separated from substrate surface, indicating permanent bonding is not achieved. This can be understood with looking into air gaps at the substrate-PDMS interface.

Substrate is oxygen plasma treated for 1 minute to activate its surface. Then, 1:3 cross-linker:base mixed PDMS is casted on the substrate with the thickness of 5 mm. Since PDMS is a liquid before curing which can penetrate inside smallest gaps as 10 nm [31], it is necessary to encapsulate the borders of the container the sample is placed. Petri dish is a sufficient choice, which also can be used to spin coat PDMS in traditional PDMS processing. After casting, gas bubbles are cleared with vacuum environment for 20 minutes. Normally, PDMS can be cured itself in 48 hours, but it is common practice to increase temperature to decrease curing time. PDMS is cured for 1 hours at 65 C inside a petri dish. After curing, sample is separated from the dish by

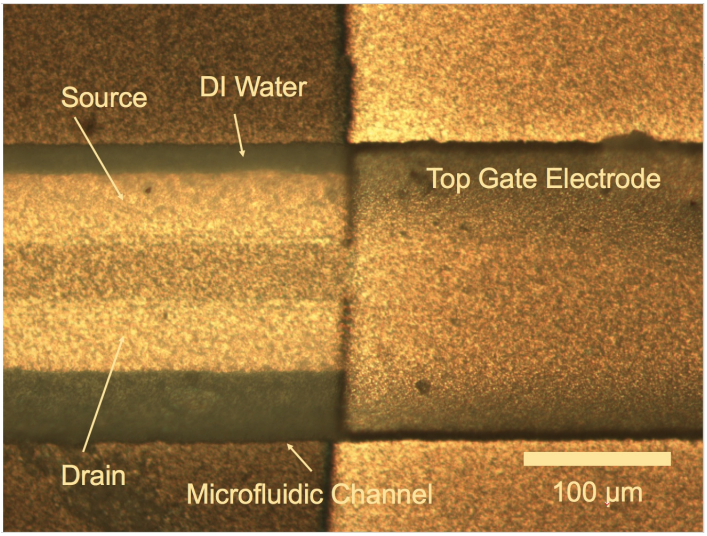

Figure 3.11. Micrograph of the device after 5 μm parylene is deposited and microfluidic channel is released.

cutting PDMS with razor blades from the edges of sample.

Reservoir holes are opened with flat gauge needles, with its tip is sanded to achieve clean cut penetration without tearing PDMS. Acetone is injected into the reservoirs, etching the photoresist sacrificial layer, thus releasing the microfluidic channel. After cleaning the sample with IPA and removing dust from the surface of PDMS with scotch-tape, sample is prepared for testing.

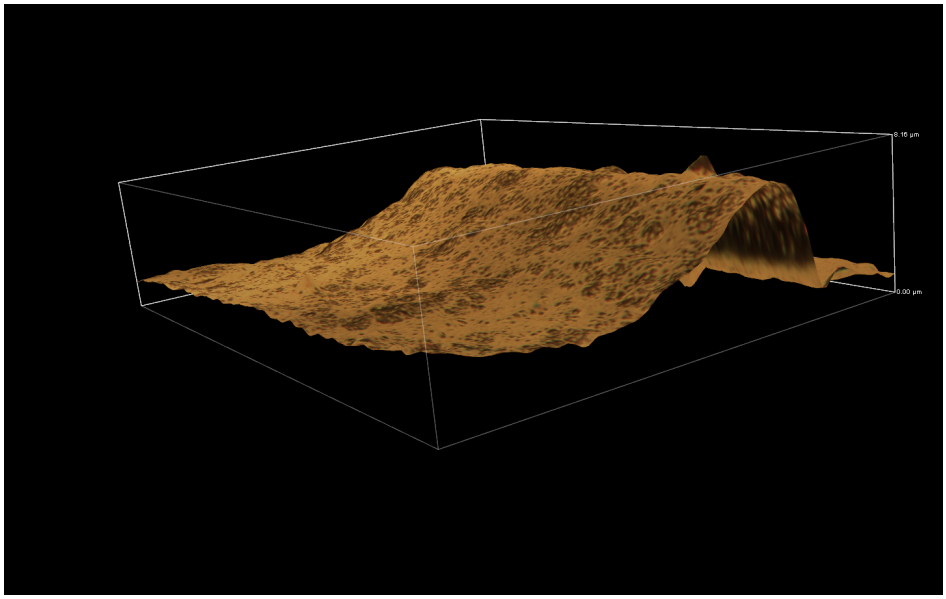

Figure 3.12. 3D micrograph of collapsed Al top gate.

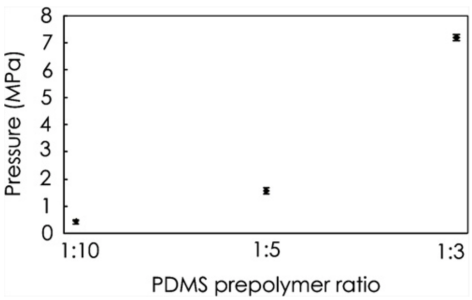

Figure 3.13. Comparison of bonding strengths of PDMS with respect to mixing ratios [27].

Figure 3.14. Oxygen plasma equipment.

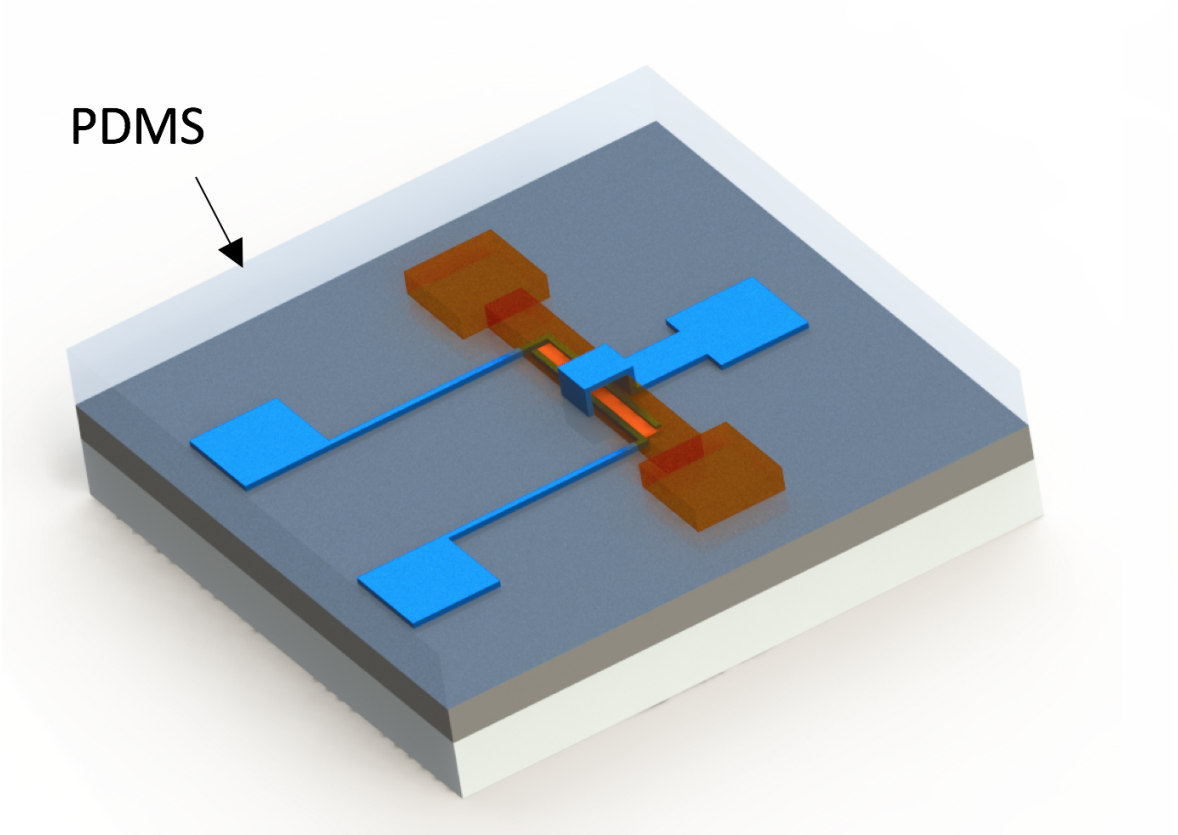

Figure 3.15. Device after 5 mm thick PDMS is casted.

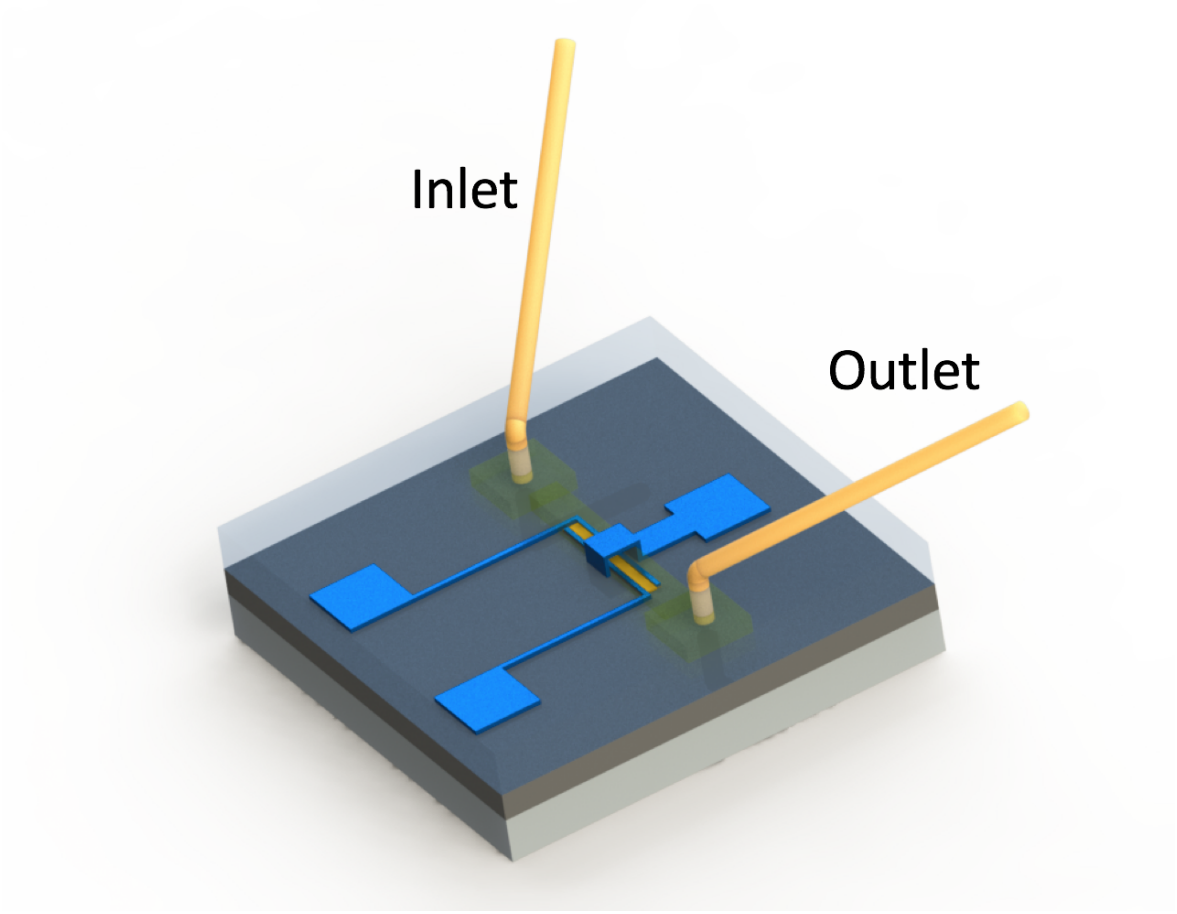

Figure 3.16. Device after reservoirs are opened and sacrificial photoresist is removed.

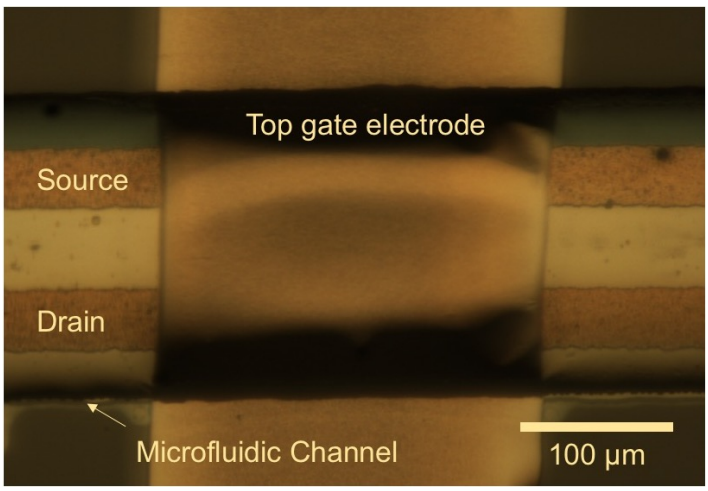

Figure 3.17. Micrograph of the device after PDMS microfluidic channel is released.

4. EXPERIMENTS AND RESULTS

4.1. Preparation of Test Setup

Since surface of the device is covered with PDMS, it is necessary to drill PDMS to reach source, drain and gate contact regions. With oxygen plasma applied to those surfaces, punching PDMS will be a hard task because PDMS would be bonded to those surfaces, requiring high amounts of pressure, which can damage contact aluminum, or the sample. To avoid this, photoresist bumps are placed on contact regions and baked for 1 hours at 110 °C before applying oxygen plasma to device. PDMS does not adhere photoresist, so it is trivial to remove PDMS in line with photoresist bumps. Using this method, after cutting carefully, PDMS is extracted from contact regions and photoresist is removed with acetone.

After contacts are opened on the device, experimental setup is prepared by placing sample to a circuit board. Source, drain, gate and bulk contacts are connected to peripheral inputs of the test setup with silver epoxy. Silver epoxy is used instead of soldering because solder does not adhere well to the substrate. Silver epoxy is applied between the wires and contacts of the substrate, and left for baking for 2 hours at 110 °C to remove solvents to solidify epoxy for permanent contact. PDMS also increased mechanical stability of the test setup because of mechanically supporting wires inserted through it, increasing durability to stress. This is important because silver epoxy contacts can be disintegrated with small amount of stresses applied to them, which can easily occur with little force to wires.

When the test setup is prepared, DI-Water is injected through inlet with syringe pumps until water is observed at the outlet of microfluidic channel. With dimensions of 4000 μm $\times$ 200 μm $\times$ 15 μm, 0.012 μL of DI water is injected inside the channel region of microfluidic channel. Water volume inside channel also gives insight about the potential of integrating microfluidics, which indicates that 100 transistors integrated to channel with this design can work with fluids with a volume about 1.2 mL.

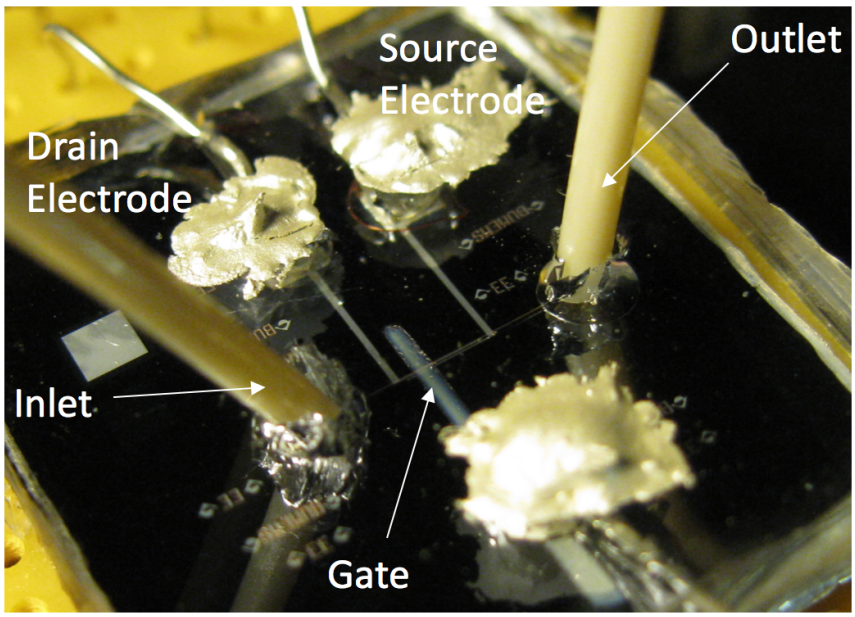

Figure 4.1. Test setup of the fabricated WG-FET device with external fluidic and electrical connections.

4.2. Testing Instrument

Keithley 4200 semiconductor characterization system is used for obtaining transistor characteristics of the fabricated device. With built-in source measure units (SMUs), this system can accurately measure I-V and C-V characteristics of semiconductor devices with measuring currents up to 1 A.

4.3. Measurements

I_D vs V_{DS} curves of the WG-FET device with W/L ratio of 3000 μm/ 50 μm and gate width of 300 μm is shown in Figure 4.3. Although it is clear that this transistor's drain current is affected from V_{GS}, transistor does not enter in a saturation region. This means that gate voltage cannot dominate drain-source voltage.

I_D vs V_{DS} curves of the WG-FET device with W/L ratio of 3000 μm/ 50 μm with gate width of 1500 μm is shown in Figure 4.4. This transistor has much greater

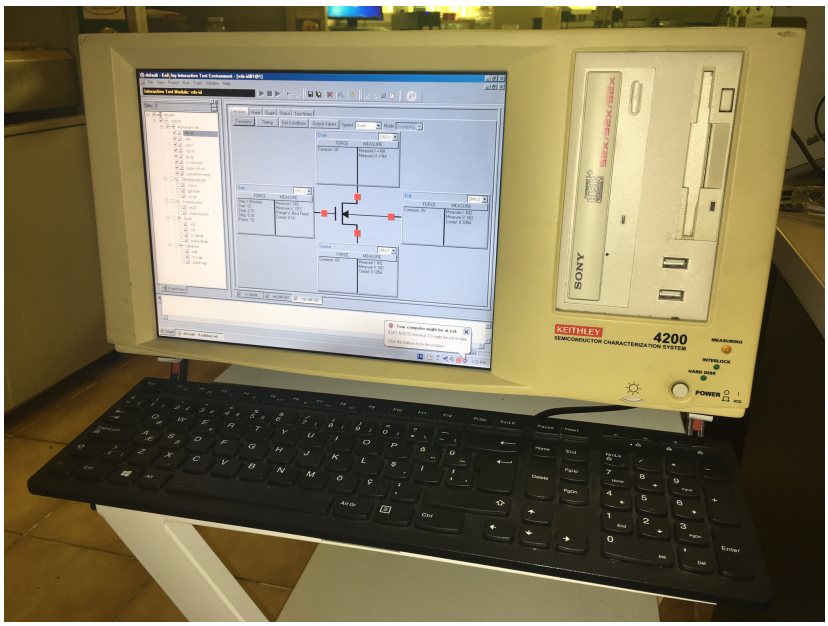

Figure 4.2. Keithley semiconductor characterization system.

output currents, and the characteristic indicates there is a saturation region.

Experimental results show ON/OFF current ratio of 22 A/A at V_{DS} = -0.5 V with a threshold voltage of -0.4 V. ON/OFF ratios are very small compared to previous work [16] but maximum drain current is much larger than planar gate study. This is attributed to have closer electric fields to channel, also it more acts like a parallel plate capacitor.

Comparison with previous work [16] is shown in the Table 4.1.

Table 4.1. Comparison of microfluidic integrated suspended top gate WG-FET with probe and planar structures.

	Probe-gate	**Planar-gate**	**This work**
Maximum drain current	8 μA	0.4 μA	900 μA
ON/OFF ratio	14000	250	22

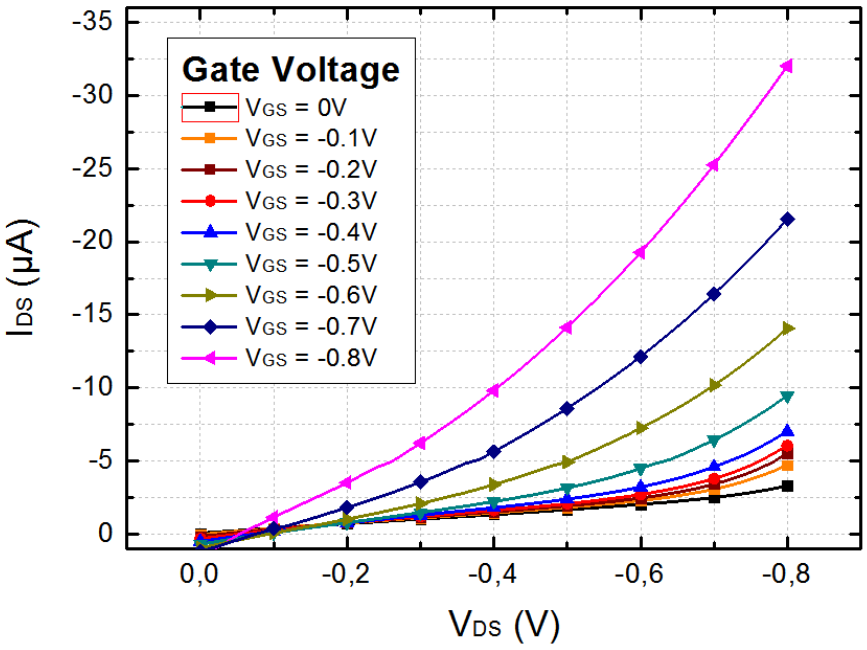

Figure 4.3. I_D vs V_{DS} characteristic of the device when gate width is 300 μm.

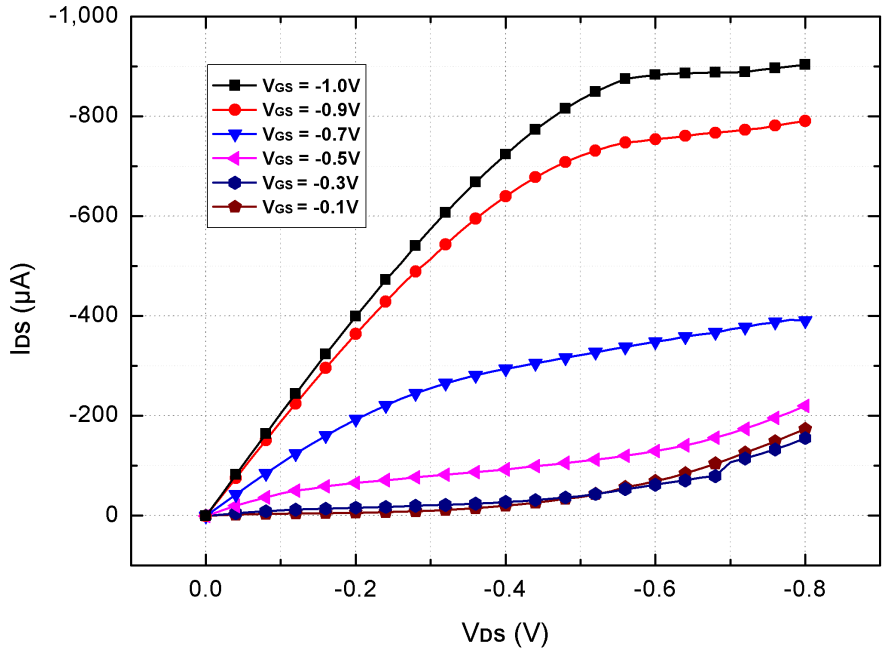

Figure 4.4. I_D vs V_{DS} characteristic of the device when gate width is 1500 μm.

5. CONCLUSION

This thesis established fabrication steps to integrate microfluidic channels to the Water-Gate Field effect transistor. New methods are introduced to fabricate gate electrode attached to microfluidic channel. This allowed to include multiple transistors in a single chip, without using water droplets. While fabricating microfluidic channel, surface micromachining is used instead of traditional soft-lithography and bonding processes.

Since these transistors utilize electrical double layer to operate, it should be investigated to manifest ion effects to transistor characteristics. Also transistor model should be improved by taking gate electrodes into account. Transistor can be made more reliable by insulating drain and source electrodes, which can be achieved by chemical vapor depositing an insulator material, like silicon oxide, or parylene. Photoresist cannot be utilized since being used as a sacrificial layer.

For future work, multiple transistor effects should be investigated. Even multiple inlet outlet systems are achievable with fabrication methods presented in this thesis, multiple inlet-outlets are mostly used for different kinds of liquid injection. While operating in the same microfluidic channel, electric field of one of the top gates can affect the other transistors, or applied voltages can cause electro-osmotic pumping. These effects can be investigated or utilized to create more complex devices. Also some features can be added to microfluidic channel, like valves and pumps.

Creating a sensory device will be studied in the near future of this project. Chemical interactions inside the microfluidic channel can be investigated which can be used for biological research. Also integration of a read-out circuit is a challenge which should be addressed to create a lab-on-a chip system.

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APPENDIX A: MASKS USED IN FABRICATION

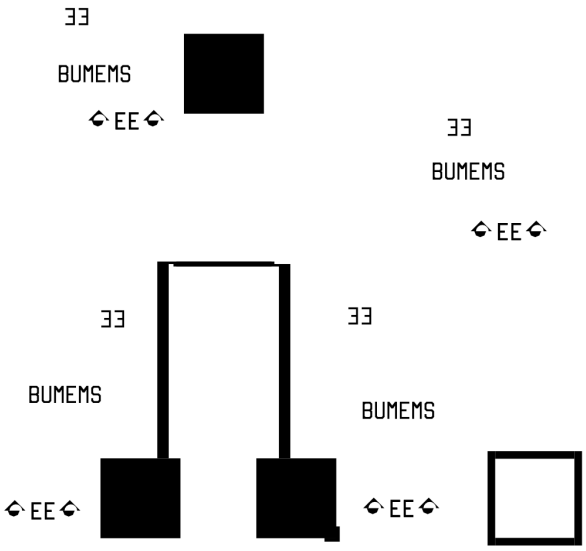

Figure A.1. Si mask.

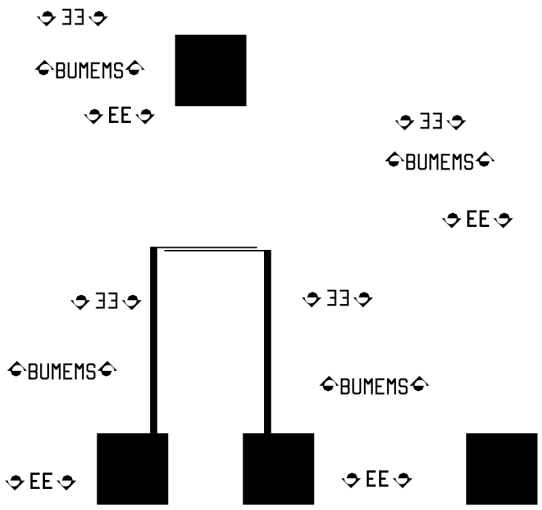

Figure A.2. Al mask.

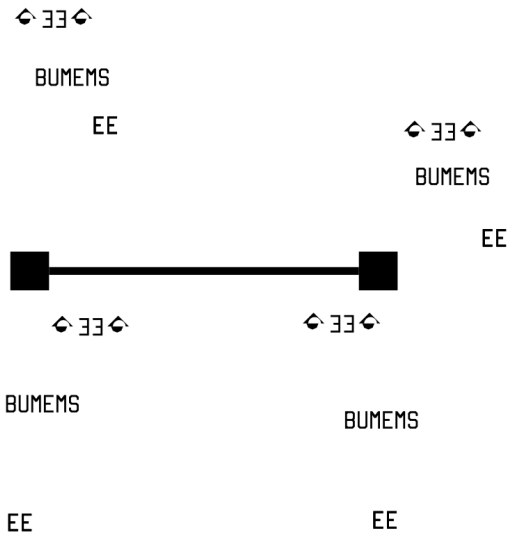

Figure A.3. Microfluidic channel mask.

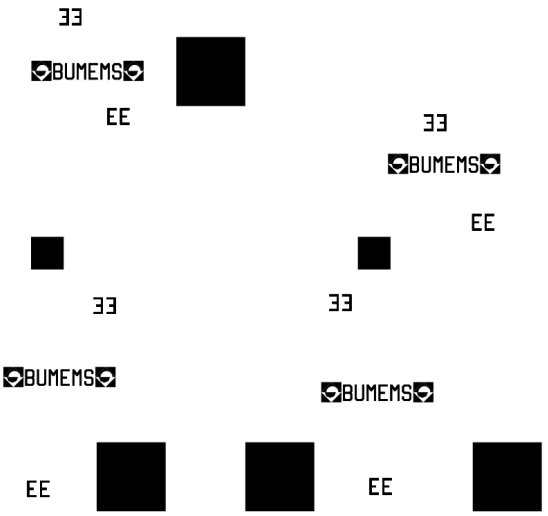

Figure A.4. Via mask.