Design of Low Power Continuous Time $\Sigma - \Delta$ Analog to Digital Converters.

by

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I dedicate this thesis to my family and friends. To my little nieces Anil, Sevilay and Lara. Baba, Mama, Rahil, Shirin, Bahram and Reza, I would not have been here if it was not for your endless sacrifices. My love for you is bound to no limits. I thank my dearest friends, Ata, Mahta, Kaveh and Ulduz for their selfless support through my darkest days and their company through the most beautiful days of my life.

When all are one and one is all, to be a rock and not to roll.

And you've shown me a stairway to heaven ...

ABSTRACT

Design of Low Power Continuous Time $\Sigma - \Delta$ Analog to Digital Converters.

A second order CT $\Sigma\Delta$ modulator for audio frequency sensory systems in 180nm TSMC CMOS process is presented. The design incorporates a C-gm based current mode structure with 2nd order noise shaping, a 25 kHz bandwidth, a sampling frequency of 12.8 MHz marking an OSR of 256 and a total power consumption of 5.9μW. Consequently the proposed loop achieves a FOM of 2.8fJ/conv. The overall power consumption is distributed evenly among segments of the loop to attain adequate number of bits without the need to sacrifice power. Two representations of overall design, a robust Voltage input circuit and a high precision current input modulator, are introduced.

ÖZET

Düşük Güçlü ve Gerçek Zamanlı Analog-Sayısal $\Sigma - \Delta$ Dönüştürücü Tasarımı

Ses frekanslarında çalışan sensör sistemleri için tasarlanan, 180 nm TSMC CMOS teknolojisiyle gerçeklenmiş, ikinci dereceden sürekli zamanda Sigma Delta modülatörü sunulmuştur. Tasarımda, ikinci derece gürültü şekillendirmesine, 25 kHz bant genişliğine, 256 aşırı örnekleme miktarı ile 12.8 MHz örnekleme frekansına ve 5.9μW güç tüketimine sahip C-gm temelli akım modlu yapı kullanılmıştır. Sonuç olarak, önerilen döngü 2.8 fJ/con FOM değerini sağlamaktadır. Yeterli sayıda biti güçten feragat etmeden elde edebilmek için, toplam güç tüketimi tüm segmentler üzerinde eşit seviyelerde dağılmıştır. Gürbüz voltaj girişli ve yüksek çözünürlüklü akım girişli modülator olmak üzere iki farklı tasarım anlatılmıştır.

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LIST OF SYMBOLS

C	Capacitance
F_s	Sampling frequency
F_b	Signal frequency
K	Integrator gain degradation coefficient
L_{vt}	Low threshold device
G_m	Transconductance of an inverter Cell
g_m	Transconductance of a single transistor device
g_0	Transconductance seen at input and second integration node
L	Channel length of a transistor
N	Number of bits in a data converter
R_e	Enhancement Resistance
V_{gs}	Gate to source voltage
V_{th}	Threshold voltage
V_{in}	Input node voltage
W	Channel width of a transistor

LIST OF ACRONYMS/ABBREVIATIONS

ADC	Analog to Digital Converter
CT	Continuous Time
DAC	Digital to Analog Converter
DT	Discrete Time
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
IC	Integrated Circuit
MOS	Metal Oxide Semiconductor
NMOS	Negative Channel Metal Oxide Semiconductor
NTF	Noise Transfer Function
OPAMP	Operational Amplifiers
OSR	Over Sampling Ratio
PMOS	Positive Channel Metal Oxide Semiconductor
SNR	Signal to Noise Ratio
STF	Signal Transfer Function
SQNR	Signal to Quantization Noise Ratio
$\Sigma\Delta$	Sigma Delta data converter

1. INTRODUCTION AND BACKGROUND

New research paradigms in battery powered biomedical monitoring and implant systems have emerged with the dawn pf post PC computation. There is a growing demand for mobile sensing in biomedical systems, lab on a chip devices, self powered structure health monitoring, etc. To increase the limited battery life and avoid inflicting damage to the environment, the system needs to be designed for low supply voltages and low power consumption while establishing a minimum precision especially in the case of sensor systems. Moreover, new applications such as micro arrays are in need of high precision ADCs that require a minimal space for increasing the chip accuracy.

The presented work is a data converter block for audio frequency sensory systems. A continuous time $\Sigma\Delta$ modulator is an attractive choice for ADC implementation since it possesses an inherent anti aliasing filter and relaxed requirements on integrators, thus eliminating the need for difficult filtering and sampling circuitry and mitigating power consumption. It also does not require complex switching and clocking schemes, thus paving the way for very high OSR.

However, there are challenges such as loop design, low power consumption, area constraints and effective chip implementation to be addressed. The main focus of the presented work is to reach a tangible solution for such challenges. The main contributions of this thesis can be summarized as below:

- **A simple design method for CT loops:**
  A simple methodology for modulator design is presented.
- **C-gm integrators:**
  A new approach to C-gm integrators proposed by [1] is introduced. The new circuit addresses the low power, area and supply design paradigms.
- **DAC stage:**
  A new DAC circuit is proposed to address design issues of low frequency current

mode C-gm circuits.

- **Voltage and current input circuit:**

  Two final approaches are taken for the overall design. A voltage input circuit that is more robust in nature but less precise, and a high precision current mode circuit.

- **Chip Implementation:**

  All the introduced designs are implemented in an overall layout design taped out to fabrication. Issues concerning this process are discussed as well.

1.1. ADCs

Analog to digital converters play the prominent role of interfacing between the real world which demonstrates a continuous-time nature into the digital world where, only discrete time signals and discrete time amplitudes exist. Fig 1.1 depicts the major blocks of any data converter. The sample and hold block performs the operation of

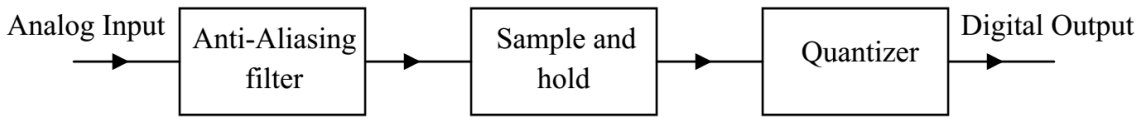

Figure 1.1. Signal processing chain.

converting a continuous time signal into a discrete time counterpart. Assuming inputs having useful data up to frequency of f_b, the Nyquist law dictates that the sampling frequency (f_S) is to satisfy the criterion shown below to avoid loosing essential data.

$$f_s \geq 2f_b \tag{1.1}$$

The anti-aliasing filter removes any signal in frequencies above f_b. The quantizer performs the process of converting input signal into discrete values. The quantization step is lossy and dependent on the accuracy of the ADC. For a system with a full scale

value of $\pm V_{ref}$ and N output digital bits, the step size of quantizer is given by,

$$\triangle = \frac{2V_{ref}}{2^N} \tag{1.2}$$

The quantization noise, ϵ, introduced into the process is bound to the range of $\pm\frac{\triangle}{2}$. The introduced quantization noise can be considered a white noise process demonstrating the probability density function depicted in Fig 1.2 [2]. The introduced quan-

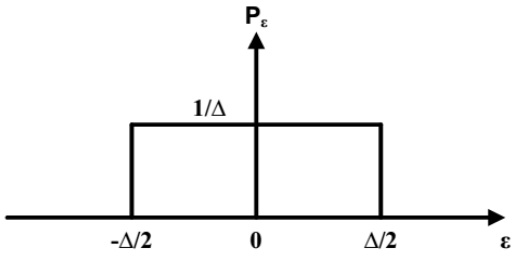

Figure 1.2. Quantization noise probability density function.

tization noise can be calculated as [2]:

$$\delta_\epsilon^2 = \int_{-\frac{\triangle}{2}}^{+\frac{\triangle}{2}} \epsilon^2 \frac{1}{\triangle} d\epsilon = \frac{\triangle^2}{12} \tag{1.3}$$

Having a sinusoidal input, total stimulus referred power is given by $\frac{V_{ref}^2}{2}$. Consequently, the signal to quantization noise can be expressed as:

$$SQNR = \frac{\frac{(2^{N-1}\triangle)^2}{2}}{\frac{\triangle^2}{12}} \tag{1.4}$$

Addressed in dB format, Equation 1.4 can be translated into:

$$SQNR(dB) = 6.02N + 1.76 \tag{1.5}$$

1.2. Oversampling ADC

As mentioned before, quantization noise is considered a white noise type and thus, it is spread evenly between DC and sampling frequencies. Consequently, it is possible to reduce the in band noise of a system by using a sampling rate much higher than that of the band of interest as shown in Fig 1.3. The improvement can be

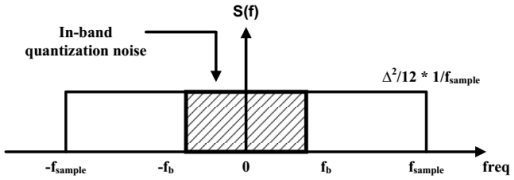

Figure 1.3. Quantization noise probability density function.

addressed through the following formula [3]:

$$SQNR(dB) = 6.02N + 1.76 + 10log_{10}OSR \tag{1.6}$$

where:

$$OSR = \frac{f_{sample}}{2f_b} \tag{1.7}$$

Based on the Equation 1.6 doubling the OSR would result in a 3dB improvement in total SNDR performance.

1.3. Sigma Delta Conversion

In a historical hindsight, oversampling was used for increasing the performance of pulse code modulation, rather than stretching quantization noise over a wide frequency range. The key to this process is to transmit the change (delta in this case) between successive samples of input instead of the actual data. The block diagram of a delta modulator is depicted in Fig 1.4. Thus, the estimate of the system stimulus can be obtained through the integration of the digital output of the delta modulator. It is

necessary to ensure that the quantization steps are adequately small in comparison to signal bandwidth for having an effective input tracking. Since the input DC signal

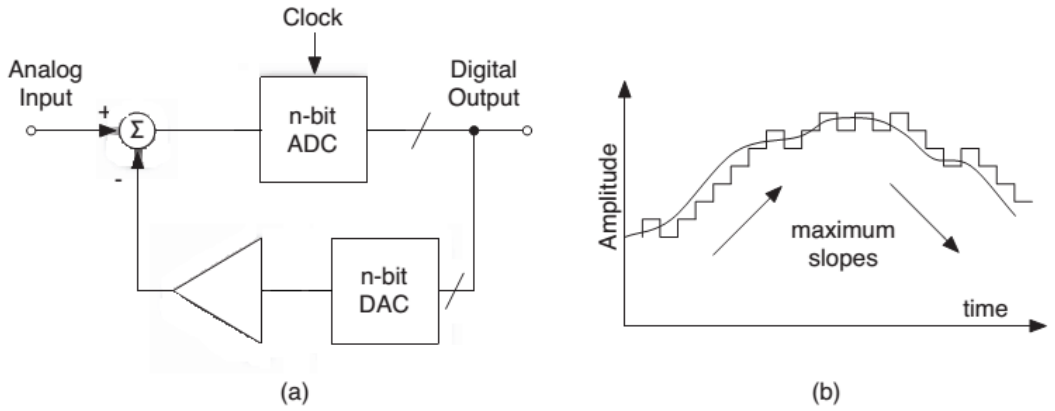

Figure 1.4. (a) Delta modulation. the difference between input and its estimate is quantized and sent away. (b) input tracking in delta modulators

does not produce any significant outputs, it is safe to assume the circuit has a high pass response [3]. Fig 1.5 (a) depicts the equivalent loop of a delta modulator. If the input derivative block is to be removed, 1.5 (b), the circuit is turned into a low pass block. What remains is an integrator operating upon the input error difference and not the estimation of the signal. Since the scheme of Fig 1.5 (b) is the integration (sigma) of the differences (delta), henceforth the loop is named a sigma-delta ($\Sigma\Delta$) modulator [3].

1.4. Sigma-delta ADC

The oversampling method of quantization noise reduction can become more effective if the noise spectrum is to be shaped out of the desired band of interest, therefore, changing white spectrum into a shaped spectrum. Such high frequency noise is not of concern since it can be removed through a digital filter. This is the basic principle of $\Sigma\Delta$ modulation. Fig 1.6 illustrates a basic discrete-time first order sigma-delta loop. Note that quantization noise is considered to be additive. The output can be written as follows:

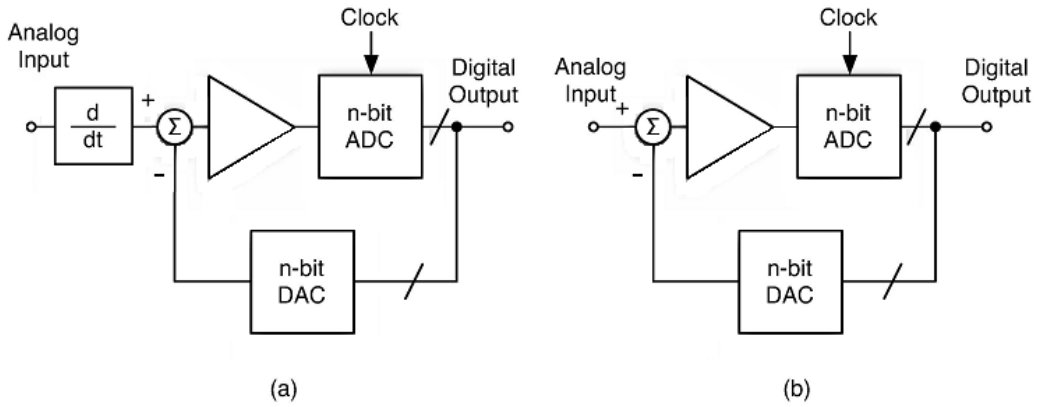

Figure 1.5. (a) Delta modulation Equivalent. (b) sigma delta modulation [3].

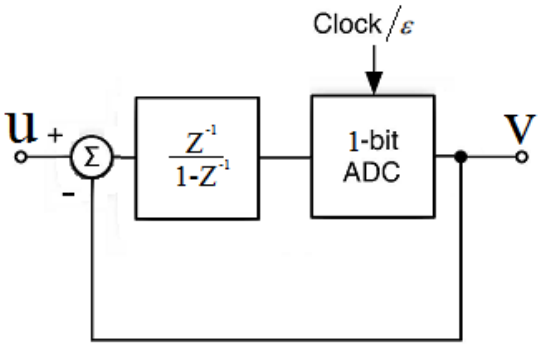

Figure 1.6. First Order Loop.

$$v(z) = STF.u(z) + NTF.\epsilon(z) \tag{1.8}$$

where u, v and ϵ represents circuit input and output and additive quantization noise respectively. Henceforth:

$$STF = \frac{v(z)}{u(z)} = z^{-1} \tag{1.9}$$

$$NTF = \frac{v(z)}{\epsilon(z)} = 1 - z^{-1} \tag{1.10}$$

Thus, the input arrives at the output with a delay. However, the quantization noise is filtered away through the $1 - z^{-1}$ function. Fig 1.7 depicts the noise shaping process of a first order system. Higher orders of shaping can be used to further improve the

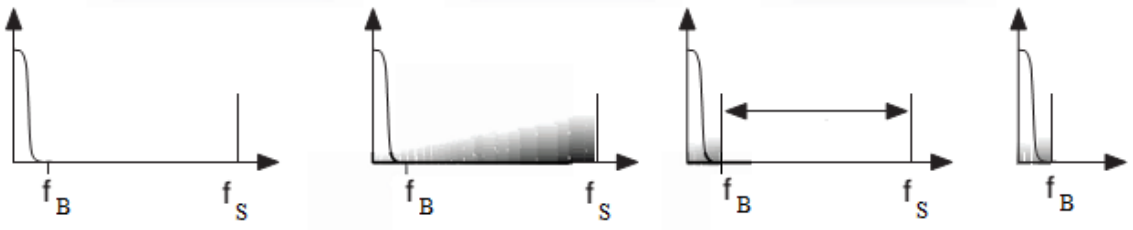

Figure 1.7. First order modulator noise shaping profile.

SQNR performance of a system. Using a loop with an order of L, NTF can be changed to the expression in Equation 1.11.

$$NTF = (1 - z^{-1})^L \tag{1.11}$$

The SQNR of such a system is [2]:

$$SQNR_{max}(dB) = 6.02N + 1.76 + (20L + 10)log_{10}OSR - 10log_{10}\frac{\pi^{2L}}{2L + 1} \tag{1.12}$$

Consequently, the SQNR improves by increasing the order of loop as well as the OSR.

1.5. Continuous-time versus Discrete-Time $\Sigma\Delta$ modulators

A Continuous-Time (CT) modulator alters the interface point between continuous time and sampled-data segments of a $\Delta\Sigma$ modulator, moving it inside the feedback loop as depicted in Fig. 1.8. The discrete-time implementation assumes that the sampling is performed before the modulator through a sample and hold circuit, giving rise to a process which is entirely in z domain and is implemented in switched-capacitor form. A continuous-time modulator, however, performs sampling after passing the

input signal through the loop filter which uses Laplace domain calculation system. [3].

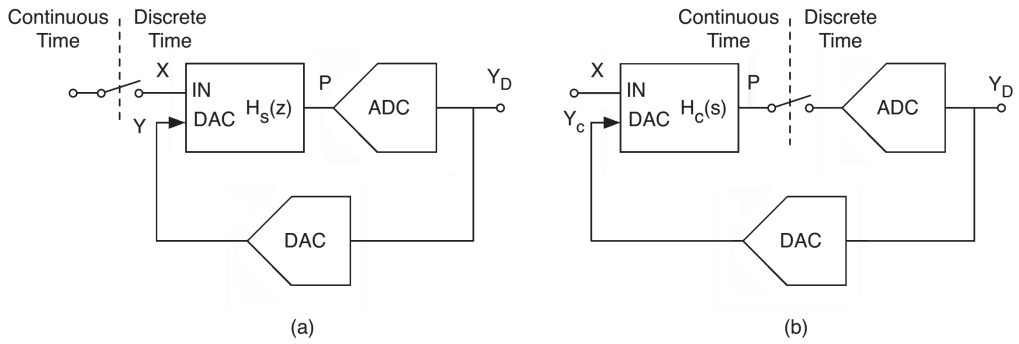

Figure 1.8. (a)Sampled-data $\Delta\Sigma$ modulator. (b) Continuous-time $\Delta\Sigma$ modulator.

The key differences between DT and CT modulators are as follows:

- **Low voltage operation:**

  The continuously decreasing supply voltage of recent CMOS technologies has lead to performance limitations for switched-capacitor circuits. In order to obtain a sufficiently low on resistance, methods such as Switch-bootstrapping or Switched-opamp are necessary. [1] [3]

- **Power consumption:**

  In swithced-capacitor circuits the unity gain frequency of operational amplifiers must be at least five times the sampling rate [1]. Thus, a high quiescent current is required to achieve the desired bandwidth. On the other hand, the unity gain frequency of integrators in the CT $\Delta\Sigma$ are usually lower than the sampling frequency.

- **Aliasing:**

  In a CT modulator, sampling occurs inside the loop. This attribute strongly reduces the out of band signals and acts as an anti aliasing filter. Thus, the need to have an additional anti-aliasing filter is nullified. Furthermore, this inherent

anti-aliasing reduces the thermal noise in the out of band frequencies. Also, CT $\Delta\Sigma$ modulators are less sensitive to asynchronous substrate interface from neighboring digital circuitry compared to DT $\Delta\Sigma$. Moreover, having the sampling circuit implemented inside the loop results in discarding any non idealistic of the sample and hold circuit in form of noise shaping. [3] [1]

- **Slew rate:**

  The step transitions at the input of integrators used in sampled-data modulators require large slew-rates since both feedback and input signals are step functions, filling capacitances through integrators. In contrast, the continuous-time input and feedback are distributed over the entire clock period in CT modulators. Such degree of freedom could be incorporated in optimizing integrator power consumption. [3]

- **Technology**

  Sampled-data circuits require the use of MOS switches that are not conveniently implemented in pure bipolar technologies. On the other hand, continuous time modulators can be integrated in any technology, including CMOS, BiCMOS and pure bipolar. [3]

- **Excess loop delay:**

  A huge portion of delay in feedback signals is due to comparator response time. Such delays alter the frequency characteristics of the modulator and are proven to degrade the SNR performance of the modulator [1]. Moreover, since the comparator response time is dependent on the differential input at its gates, the delay is input dependent. The signal imposed delay of the comparators has the same impairing effects as clock jitter [1]. Thus, using a Return-to-Zero (RZ) feedback signal gives the comparator enough time to settle and thus eliminates the effects of comparator delay on SNR.

- **Clock jitter:**

  Clock jitter in the feedback signal increases the noise in the signal band. Unlike the previous cases, clock jitter influence on CT modulators can not be mitigated by loop elements or using RZ feedback [1]. However, since the frequency of operation in this work is rather low, the jitter problem can be addressed by

Table 1.1. Main advantages of continuous-time $\Delta\Sigma$ over their discrete-time counterparts.

	Discrete-Time $\Delta\Sigma$	Continuous-Time $\Delta\Sigma$
Sampling Errors	Critical	Shaped out of band
Required supply voltage	high	low
Unity gain frequency	$f_T = 5 \times f_s$	$f_T \leq f_s$
Thermal noise aliasing	Increases noise level	Highly attenuated
Anti-aliasing filter	Essential	Not critical
Slew rate	Sensitive	Not critical
Technology	Especial considerations required	implementable with most technologies

careful circuit design and using external latch and crystals.

Tables 1.1 and 1.2 point out the main advantages and disadvantages of these circuits. The presented series of comparisons point out to the fact that CT time modulators are best used in low power applications with limited bandwidth. The relaxed slew rate constrains imposed on integrators and the possibility of reducing supply voltage to a great extent make it possible to achieve very low power consumption limits. This is corroborated by the fact that no input anti-aliasing filter and sample and hold circuit are required. The limitations caused by clock jitter make it harder for a CT loop to perform under higher frequencies. Moreover, the ability of continuous-time filters to damp their own thermal noise and the fact that it is possible to design them under most technologies give rise to the potential of designing such circuits under wider range of technologies.

Table 1.2. Main advantages of Discrete-time $\Delta\Sigma$ over their continuous-time counterparts.

	Discrete-Time $\Delta\Sigma$	Continuous-Time $\Delta\Sigma$
Excess loop delay	low sensitivity	SNR degradation
Rise and fall time asymmetry	low sensitivity	Causes harmonic distortion
Clock jitter	low sensitivity	Increases noise floor

2. Architecture

In this chapter, the design methodology incorporated for designing the modulator is presented. Section 2.1 contains a brief review of the mainstream CT loop design methodologies and their corresponding issues. In section 2.2, the approach taken in this work is presented and discussed in detail. Finally, an overall design to be implemented in circuit mode is suggested.

2.1. Loop Filter Design Methods

Design of a Continuous Time $\Sigma - \Delta$ modulator is more challenging than the Discrete Time counterparts. As depicted in Fig. 2.1, segments before comparator are continuous time, in other words Laplace form, whereas the rest of system is Discrete time. This is a critical restriction on system design since there is no transfer function relating Yn to input Int since these values are in different calculation spaces.

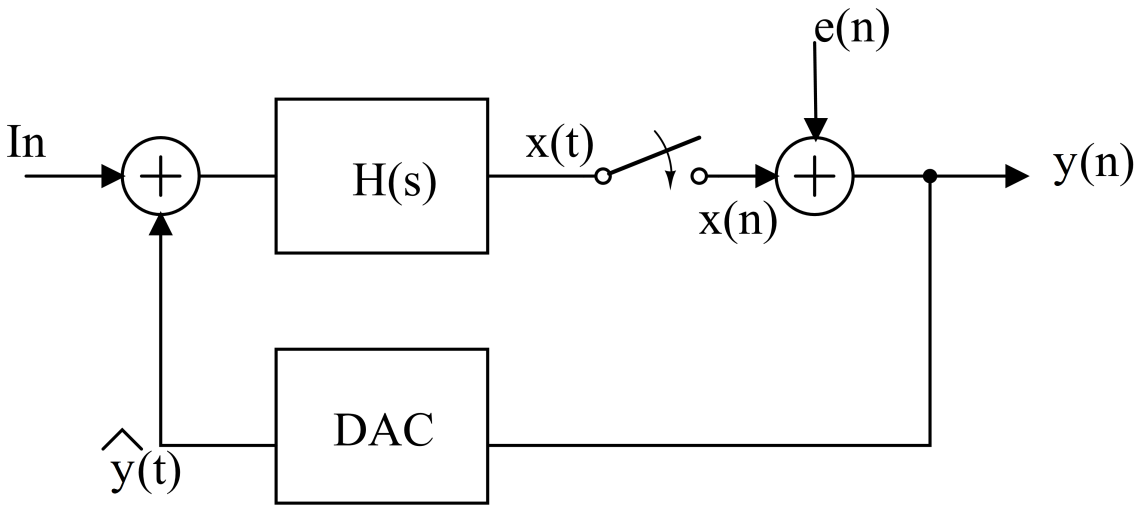

Figure 2.1. CT modulator loop in their respective states.

if $H(s) = \frac{1}{s\tau}$ then the transfer function of modulator can be represented as follows:

$$\pm y(n+1) = x(n+1) = x(n) + e(n) - \frac{T_s}{\tau}\hat{y}(nT) + \frac{1}{\tau}\int_{nT_s}^{(n+1)T_s} In(t)dt \tag{2.1}$$

Where $\hat{y}(nT)$ is the feedback based upon output signal and T_s represents sampling period. Equation 2.1 delineates a rough estimation of the transfer loop. It is important to note that in the case of a single bit latch, the overall output ,$y(n)$ thus $\hat{y}(nT)$, can only take two values which are in digital form with an unknown value and can not be converted into an analog signal representation.

Henceforth, two main approaches are used for designs, DT to CT conversion and direct CT design [4]. DT to CT conversion method is widely used since Discrete Time modulators have been present in the market long before Continuous Time loops were seriously considered. Thus, design tools for DT sigma delta modulators are improved to perfection. Two main DT to CT conversion methods are used; the Impulse-Invariant transfer function and Modified z transform [4]. Apart from being fairly complicated and failing to accurately model phenomena such as excess loop delay and jitter, these conversion methods demonstrate fairly precise translation.

Direct CT loop design methods have also emerged which yield less complicated loop coefficients [5]. It is suggested in [5] that the transfer function of Fig. 2.2 could be estimated to be Equation 2.2.

$$STF = \frac{ke^{s\theta}D(s)}{\frac{s^5}{\omega_5\omega_4\omega_3\omega_2\omega_1} + ke^{s\theta}\frac{1-e^{-sTs}}{s}D(s)} \tag{2.2}$$

Where $H_u(s) = \frac{\omega_u}{s}$, k is DAC loop gain and D(s) is:

$$D(s) = c_5 + \frac{s}{\omega_5}(c_4 + \frac{s}{\omega_4} + (c_3 + \frac{s}{\omega_3} + (c_2 + c_1 + \frac{s}{\omega_2}))) \tag{2.3}$$

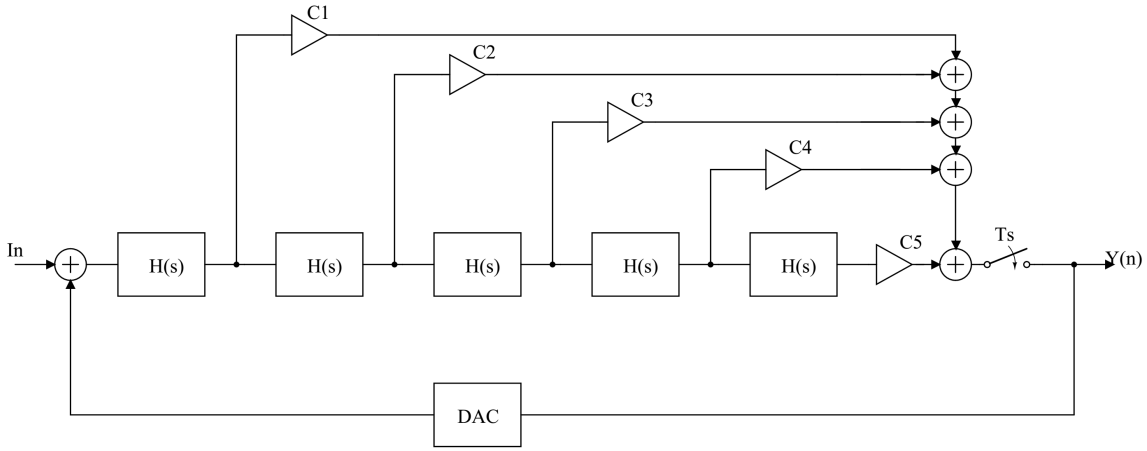

Figure 2.2. Block representation of a fifth order loop.

The term $+ke^{s\theta}$ determines the effects of excess loop delay and comparator gain, whereas the term $\frac{1-e^{-sT_s}}{s}$ is a representation of hold operation of Feedback DAC. The equation gives a rough estimation of loop pole placement. Henceforth, tuning in proper poles and zeros using feed-forward coefficients and ω_u terms according to an optimum zero placement technique such as Butterworth, an efficient loop can be designed. The model is still ineffective since the gain coefficient, k,is unknown and input dependent and thus can not be used for complicated architectures.

2.2. Architecture design

In this section, a method of loop coefficient estimation using Matlab Simulink is introduced. The proposed loop structure is demonstrated in Fig. 2.3. A second order loop is selected to benefit from characteristics such as simplicity, robustness and straightforward design procedure. Due to the unavailability of a DT to CT conversion toolbox, the option of enhanced z transform and consequently a complicated modulator design was discarded. Since the bandwidth of the proposed structure is 25 kHz, high precision could be obtained using a SNR as high is 256. This approach mitigates the need for incorporating multiple integrators. In other words, instead of increasing the sensitivity of loop gain, it is possible to do a more aggressive sampling. Reducing the number of integrators results in lower power consumption, since they consume most

of the power in a CT $\Delta - \Sigma$ modulator. Another benefit is having less chip area consumption. Consequently, it was deduced to use a second order loop. A simple replica of Equation 2.2 was incorporated to delineate system behavior as represented in Equation 2.4. The effects of the hold function and latch are ignored for the sake of simplicity.

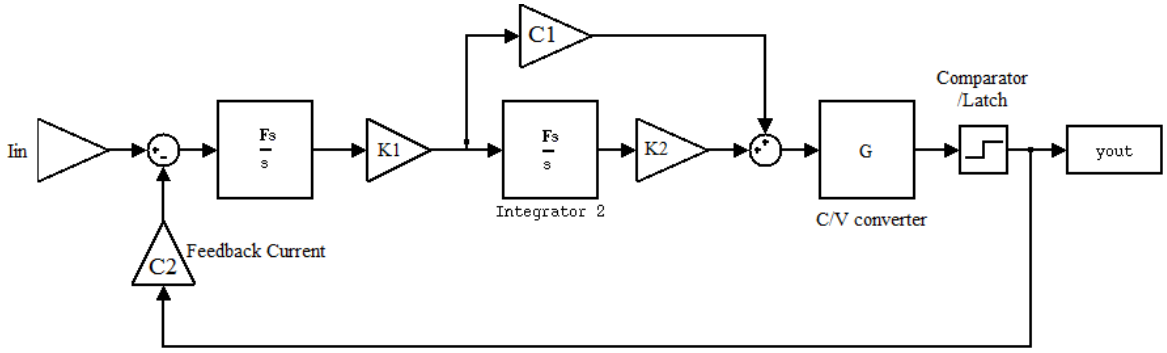

Figure 2.3. Structure of the proposed CT sigma-delta modulator.

$$yout = \frac{c_1 k_1 F_s s + k_1 k_2 F_s^2}{s^2 + c_1 c_2 k_1 F_s s + c_2 k_1 k_2 F_s^2} Iin + \frac{s^2}{s^2 + c_1 c_2 k_1 F_s s + c_2 k_1 k_2 F_s^2} \epsilon \tag{2.4}$$

Since the only significance the term C2 possesses is bounding input, it can be assigned unity value. Consequently, the input is to be held at a value less than unity. the natural frequency and damping ratio could be written as:

$$\omega_n = F_s \sqrt{k_1 k_2} \tag{2.5}$$

$$\xi = \frac{c_1}{2} \sqrt{\frac{k_1}{k_2}} \tag{2.6}$$

Thus:

$$k_1 = k_2 (\frac{2\xi}{c_1})^2 \tag{2.7}$$

Table 2.1. Simulink results for an over damped system $\xi = 0.9$.

	$C_1 = 1$				$C_1 = 2$				$C_1 = 3$			
k_2	k_1	SNR	OP_1	OP_2	k_1	SNR	OP_1	OP_2	k_1	SNR	OP_1	OP_2
2	-	-	-	-	1.62	50.9dB	1000v	1v	0.72	97.8dB	1v	5v
1	3.24	95.5dB	5v	10v	0.81	92.9dB	2v	5v	0.36	95.5dB	0.5v	1v
0.5	1.62	87.2dB	2v	5v	0.405	97.8dB	0.5v	0.5v	0.18	87.2dB	0.2v	0.5v
0.1	0.324	73.4dB	0.4v	0.5v	0.081	73.4dB	0.1v	0.2v	0.036	73.4dB	0.05v	0.05v

Table 2.2. Simulink results for a critically damped system $\xi = 0.6$.

	$C_1 = 1$				$C_1 = 2$				$C_1 = 3$			
k_2	k_1	SNR	OP_1	OP_2	k_1	SNR	OP_1	OP_2	k_1	SNR	OP_1	OP_2
2	2.88	51dB	2000v	2v	0.72	93.9dB	2v	10v	0.32	50.9dB	200v	2v
1	1.44	93dB	5v	10v	0.36	97.8dB	0.5v	0.1v	0.16	92.9dB	0.5v	1v
0.5	0.72	97.8dB	1v	1v	0.18	90.6dB	0.2v	0.2v	0.08	97.8dB	0.1	0.1
0.1	0.144	81.8dB	0.2v	0.1v	0.036	76.7dB	0.05v	0.05v	0.016	-	-	-

Three states of critically damped 2.2, under damped 2.3 and over damped 2.1 systems together with three feedforward coefficients, C_1, that are compatible with integrator topology ,to be explained later, are swept.

The terms OP_1 and OP_2 refer to the first and second integrator output voltage variation. It should be noted that even though the circuit implementation is in current mode, the Simulink simulation is in voltage mode for simplicity. The best attained results are indicated with gray shading in the Table 2.3. The introduced coefficients

Table 2.3. Simulink results for a under damped system $\xi = 0.3$.

	$C_1 = 1$				$C_1 = 2$				$C_1 = 3$			
k_2	k_1	SNR	OP_1	OP_2	k_1	SNR	OP_1	OP_2	k_1	SNR	OP_1	OP_2
2	0.72	50dB	500v	5v	0.18	92.9dB	0.5v	2v	0.08	50.6	100v	2v
1	0.36	92.9dB	1v	2v	0.09	97.8dB	0.1v	0.2v	0.04	92.5dB	0.2v	0.5v
0.5	0.18	97.8dB	0.2v	0.2v	0.045	90.6dB	0.05v	0.05v	0.02	97.5dB	0.05v	0.05v
0.1	0.036	81.8dB	0.05v	0.05v	0.009	76.5dB	0.1v	0.1	0.004	-	-	-

demonstrate low variation at each integrator output with high precision. A more detailed simulation indicated the values $k_1 = 0.3$ and $k_2 = 0.55$ obtain an optimum SNR of 99dB. Fig. 2.4 and 2.5 demonstrate the acquired SNDR and output voltage variations of each integrator respectively. It should be noted that the low output variations are not of concern in a noise performance retrospect since the circuit implementation is in current mode. Minimal variation of outputs is essential to ensure efficient power performance and linearity. Such voltage changes require extra power to take place and are best kept at minimum. It is also the case that high output variation would push integrators into nonlinear regions, causing third harmonic and loss of accuracy. The depicted voltage range is determined by the feedback signal C_2. Thus, the circuit implementation of integrators are to handle output currents as big as half the feedback signal while retaining their linearity.

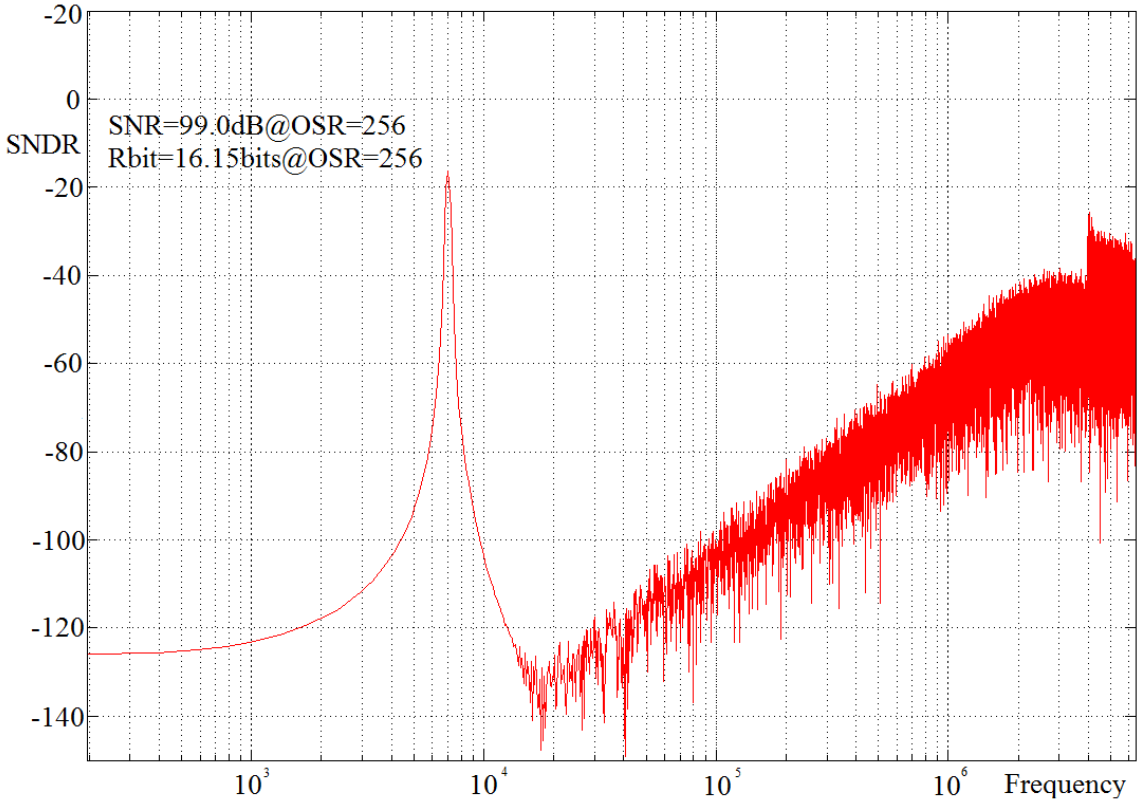

Figure 2.4. SNDR results of Simulink simulation of coefficients: $k_1 = 0.3$ and $k_2 = 0.55$.

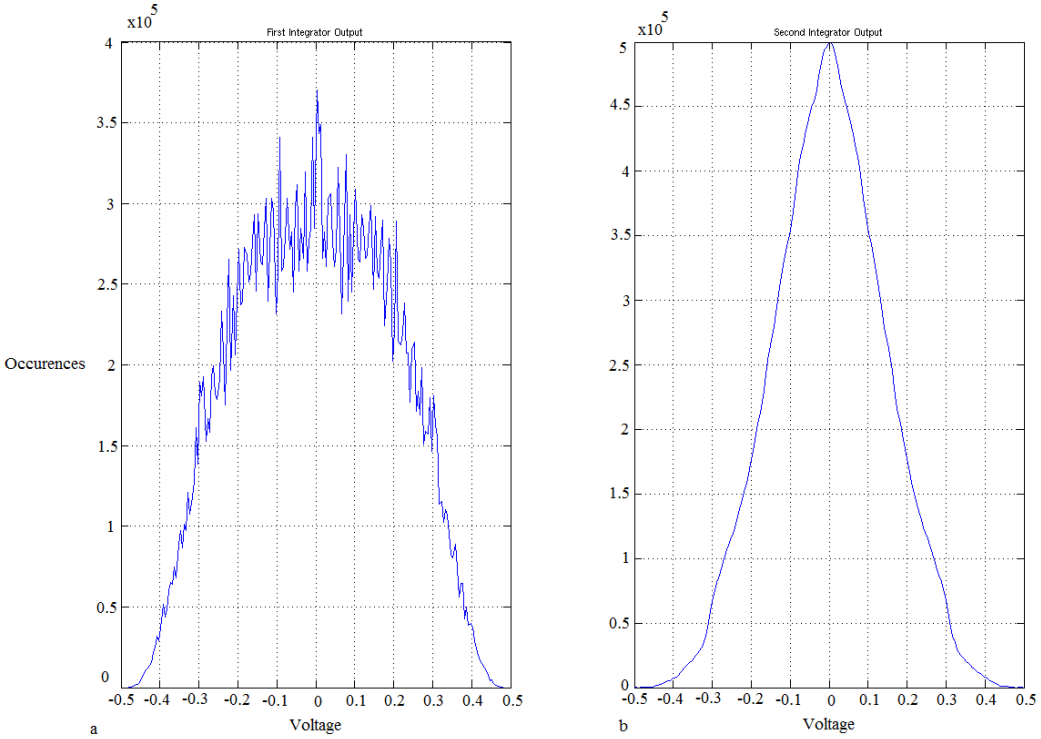

Figure 2.5. a: Output voltage variation of (a) first integrator and (b) second integrator during a 24μs simulation.

3. Integrator Circuit Implementation

In this chapter, the current mode C-gm integrator used for implementation of CT ΣΔ modulator is presented. Section 3.1 contains a detailed analysis on circuit functionality, operation and design concerns. In Section 3.2 the noise performance of Integrators is studied to see if the noise floor is appropriate for the target precision. Finally layout implementation of the integrator unit is presented in Section 3.3.

3.1. Integrator Circuit Design

Fig. 3.1 depicts the architecture of the integrator units. It is fundamentally composed of two cross coupled inverter pairs [1]. A gain boosting method [6] has been implemented through the enhancement resistors R_e. Unlike the implemented approach by [1], inverters are used instead of current mirror circuits. This modification results in a wider linear region of operation, which together with minimal current and voltage swing, enabled by the selected structure, results in minimal third harmonic in SNDR performance. The enhancement resistors R_e are considerably small. Thus, it is safe

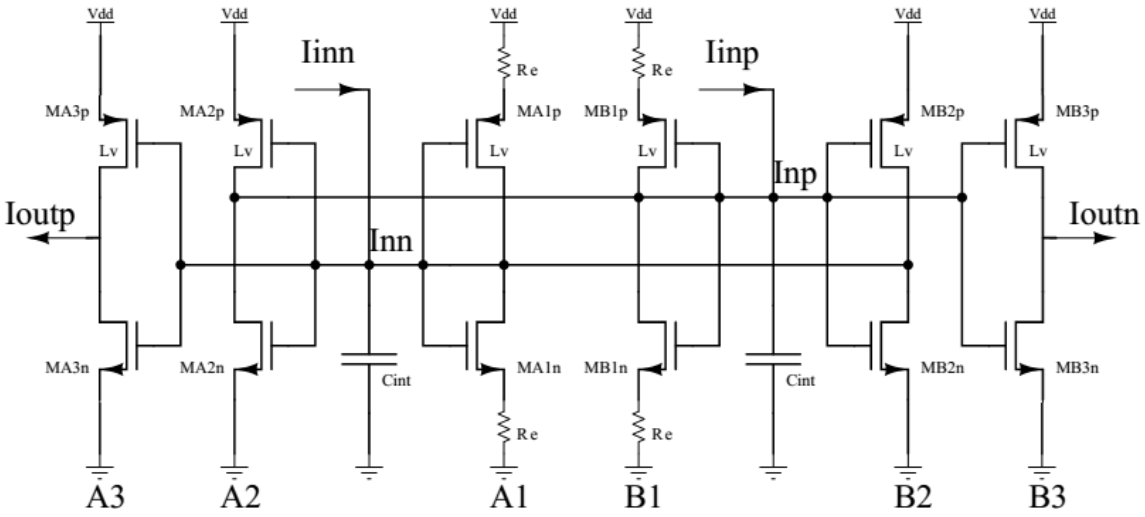

Figure 3.1. Integrator circuit schematic.

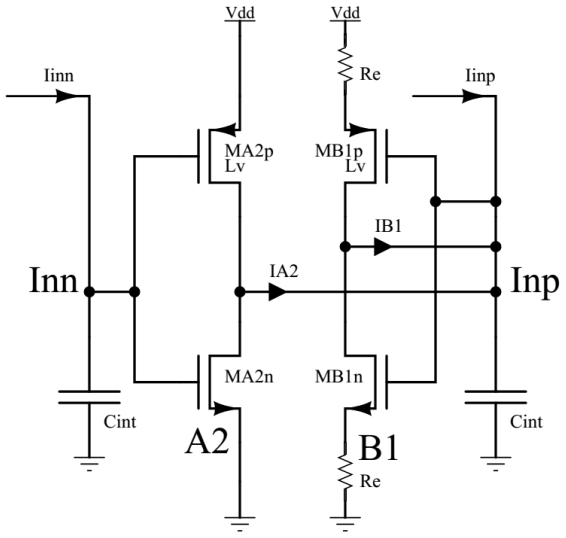

Figure 3.2. Closer inspection of positive input interface.

to assume that there is only one internal node in each differential path to which a large capacitance is attached. Hence, any extra wiring and gate capacitance are only added to the total capacitance. Consequently, the circuit has only one pole which makes it a perfect candidate for integrating circuitry. Moreover, the circuit does not require any additional biasing stages which adds to the overall simplicity of design. In order to analyze circuit performance, the model represented in Fig. 3.2 is used. The process of integrating input current into a voltage signal on the input node can be described as follows:

$$V_{inp} = (I_{inp} - G_{B1}V_{inp} - G_{A2}V_{inn}) \times \frac{1}{Cs + g_0} \tag{3.1}$$

$$V_{inn} = (I_{inn} - G_{A1}V_{inn} - G_{B2}V_{inp}) \times \frac{1}{Cs + g_0} \tag{3.2}$$

$$V_{inp}(Cs + g_0) = I_{inp} - G_{B1}V_{inp} - G_{A2}\frac{I_{inn} - G_{B2}V_{inp}}{Cs + g_0 + G_{A1}} \tag{3.3}$$

$$V_{inp}(Cs+g_0+G_{B1})(Cs+g_0+G_{A1}) = I_{inp}(Cs+g_0+G_{A1}) - G_{A2}V_{inn} + G_{A2}G_{B2}V_{inp} \tag{3.4}$$

Since $I_{inp} = -I_{inn}$:

$$V_{inp} = I_{inp}\frac{Cs + g_0 + G_{A1} + G_{A2}}{(Cs + g_0 + G_{B1})(Cs + g_0 + G_{A1}) - G_{A2}G_{B2}} \tag{3.5}$$

$$V_{inp} = \frac{I_{inp}}{(Cs + g_0)\frac{Cs+g_0+G_{B1}+G_{A1}}{Cs+g_0+G_{A1}+G_{A2}} + \frac{G_{A1}G_{B1}-G_{A2}G_{B2}}{Cs+g_0+G_{A1}+G_{A2}}} \tag{3.6}$$

where G represents the overall transconductance of each individual inverter and g_0 represents the overall input transconductance seen on the input node. Having a matched circuit with $G_{A1} = G_{B1}$ and $G_{A2} = G_{B2}$, it is concluded that:

$$V_{inp} = I_{inp}\frac{1}{Cs + g_0 + G_{A1} - G_{A2}} \tag{3.7}$$

$$I_{outp} = I_{inp}\frac{G_{A3}(s)}{Cs + g_0 + G_{A1} - G_{A2}} \tag{3.8}$$

If G_{A1} is slightly less than G_{A2} due to the enhancement resistor R_e, it would cause the value of g_0 to diminish. Consequently, the 3 dB frequency of circuit pole would fall below 1 kHz and the overall DC gain of the circuit will increase, causing more aggressive noise shaping. However, it should be noted that g_0 is not to be completely

eradicated for it would make the DC phase prone to a change of 180 degrees and make the loop unstable at very low frequencies. Fig. 3.3 depicts the effects of multiple critical resistance values on the frequency response of integrators.

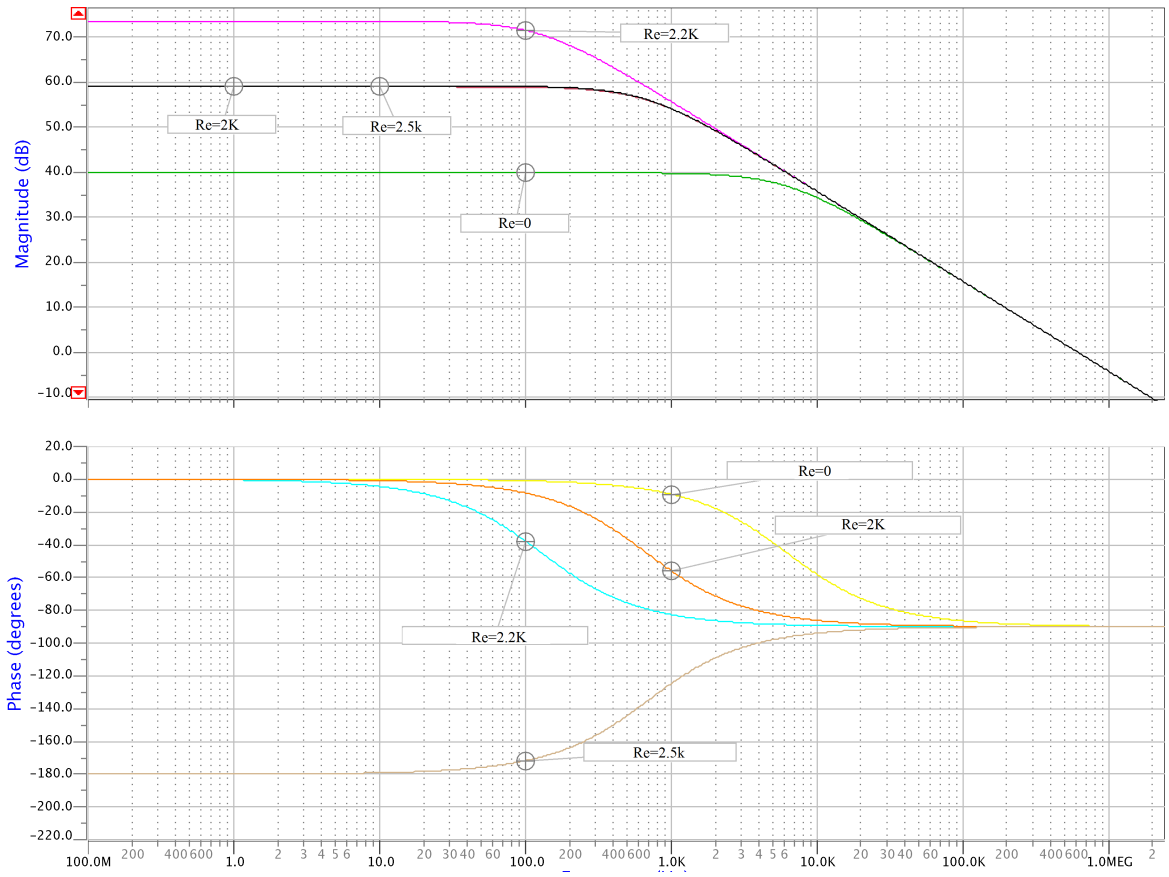

Figure 3.3. Frequency response with multiple enhancement resistors.

Long transistors with small width were selected for implementation in the integrators. The aim is to increase the resistance seen at the internal nodes, decreasing the value of g_0. Having such long transistors also causes the transconductance of inverters to decrease. As a result, the value of integrating capacitance can diminish as well, saving chip area. It should be noted that the amount of threshold voltage on both NMOS and LvPMOS, low threshold voltage PMOS, devices is close to 0.3V. Consequently, the DC operating point of integrators is close to 0.4V. For optimum linearity, the transconductance of PMOS and NMOS transistors on each inverter are to be closely matched. The term G_{A3}(s) can be represented as follows [7]:

Table 3.1. Corner analysis results for an input of -4.8 db.

Corners	TT	FF	SS	FnSp	SnFp
SNDR	91.4dB	90.7dB	87.4dB	90.2dB	91.4dB

$$G_{A3}(s) = 2g_m(1 - \frac{s}{z_1}) \tag{3.9}$$

$$z_1 = \frac{g_m - g_{ds}}{2C_{gd}} \tag{3.10}$$

The unwanted zero is located at approximately 1GHz frequency, which means that the maximum operating range of this integrator is 100 MHz. It is obvious from Equation 3.6 that this current mode integrator is sensitive to g_m matching [1]. Fig 3.4 shows three possible cases of matching possibilities which include all G_ms having perfect matching, a 1% error between G_{A1} and G_{B1} and finally a 1% mismatch between G_{A1} and G_{A2} based on Equation 3.6. Therefore it is essential to have perfect matching between integrators to ensure optimum performance. It is also the case that any process variations between PMOS and NMOS transistors would alter the operating voltage of the internal nodes. However, the effects of process variation may only cause the bias voltage of input to change 30 mV for the most extreme corners of simulation. Table 3.1 demonstrates the overall circuit performance under corner analysis simulation. It is worth noting that it is possible to have as many feedforward paths as desired since adding any additional feedforward path is the equivalent of having an extra pair of inverters in the circuit. However, each extra feed forward results in extra power consumption and the value of the path is only an ordinal number. Thus, it is best to use a single feedforward path with a gain of 1 and design the loop accordingly.

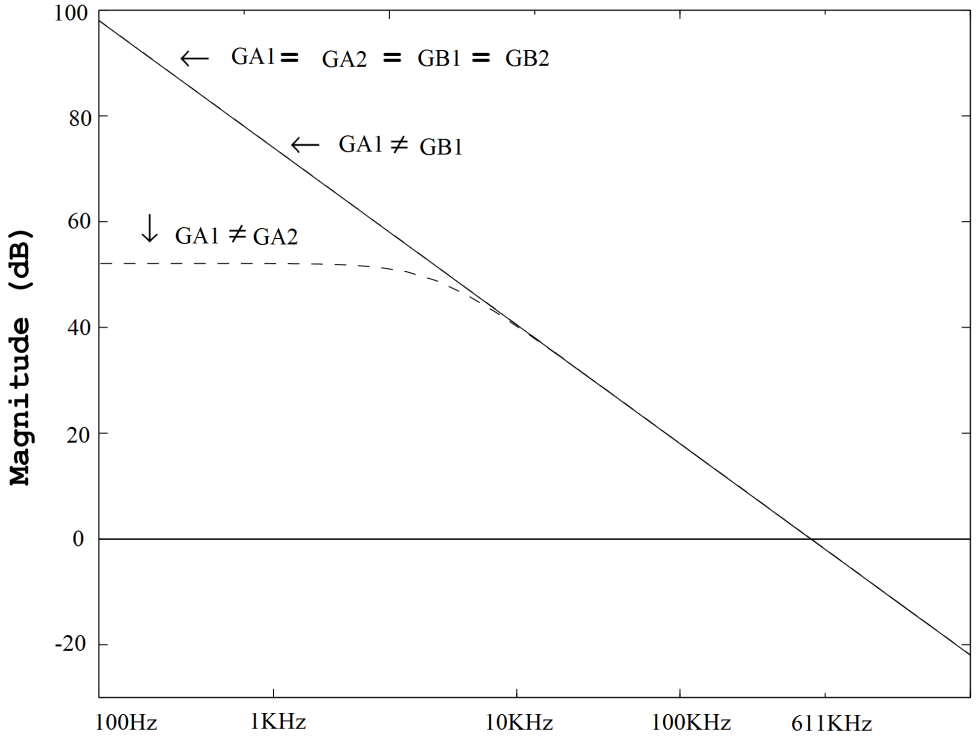

Figure 3.4. Conceptual frequency response based on 3.6.

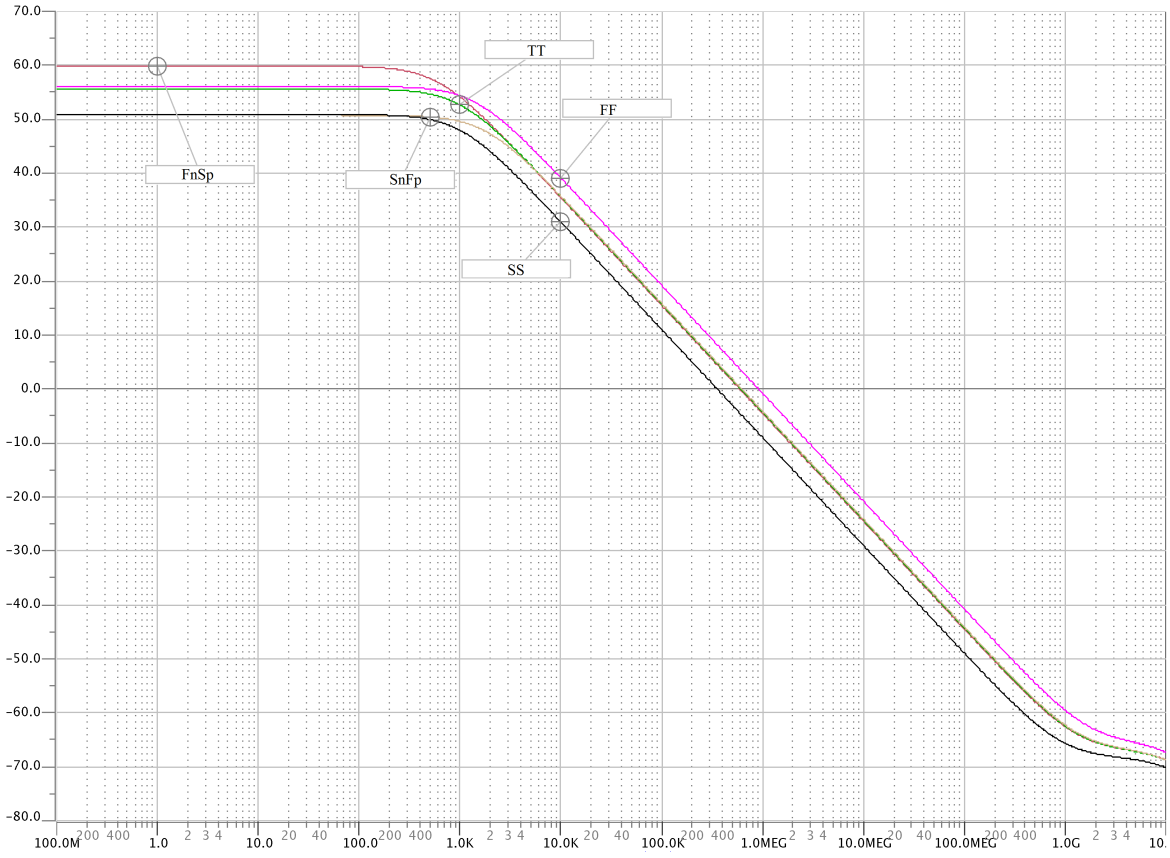

Figure 3.5. Frequency response of Integrators under corner analysis simulation sweep.

3.2. Noise Performance

The single node/pole structure of integrators means that the input node is also the output node and thus there is no need for calculating input referred noise of integrators. Thus, measuring the overall noise at the input node would suffice [1]. The total noise is due to three inverters plus two enhancement resistors.

$$\frac{i_d^2}{\Delta f} = 4kT \times [6(\frac{2}{3}g_m) + 2R_e(g_m + \frac{1}{R_e})^2] \tag{3.11}$$

$$R_e(g_m + \frac{1}{R_e})^2 = 2.3k(\frac{1}{750k} + \frac{1}{2.3k})^2 \simeq \frac{1}{2.3k} \tag{3.12}$$

$$\frac{i_d^2}{\Delta f} = 1.66 \times 10^{-22} \times [\frac{4}{750k} + \frac{1}{2.3k}] = 704.13 \times 10^{-28} \tag{3.13}$$

$$i_d^2 = 704.13 \times 10^{-28} BW + 2.7 \times 10^{-3} ln(BW) = 22 \times 10^{-22} \tag{3.14}$$

The flicker noise is negligible. Total input noise power for a 90nA input current is 4.05×10^{-15}. Thus, the maximum achievable precision is:

$$TotalSNDR = 20log_10(\frac{4.05 \times 10^{-15}}{22 \times 10^{-22}}) = 105.03dB \tag{3.15}$$

where g_m is the transconductance of both NMOS and PMOS transistor in an inverter unit. As mentioned in section 3.1, these transistors are designed to have similar g_m

values. All in all, the rough estimation acquired in Equation 3.15 indicates that the noise floor is mainly due to enhancement resistors; however, it is acceptable for the target total SNR.

3.3. Layout Design

As mentioned in Section 3.1, it is essential to have all the integrators closely matched together to acquire optimum accuracy. The transistors used have large lengths with minimal width. Consequently, fingering them is not an option. It is best then to draw the transistors as close to one another as possible and have a fully symmetrical and balanced placing and routing with enough number of vias. Since it is critical to have matching between B_1 and B_2 and also A_1 and A_2, they are drawn next to each another and their width has been raised to 0.5μ, avoiding minimum width, to ensure process variation will not have a toll on circuit performance. The integrator is designed as compact as possible so that any process variation would affect the whole circuit and not just a few of the transistors. The interface between the first and second integrator is capable of tolerating small offsets and thus it is not necessary to have them both drawn very close. The design has a length of 36.68μm and a width of 18.82μm and consequently a total area of $690.32\mu m^2$.

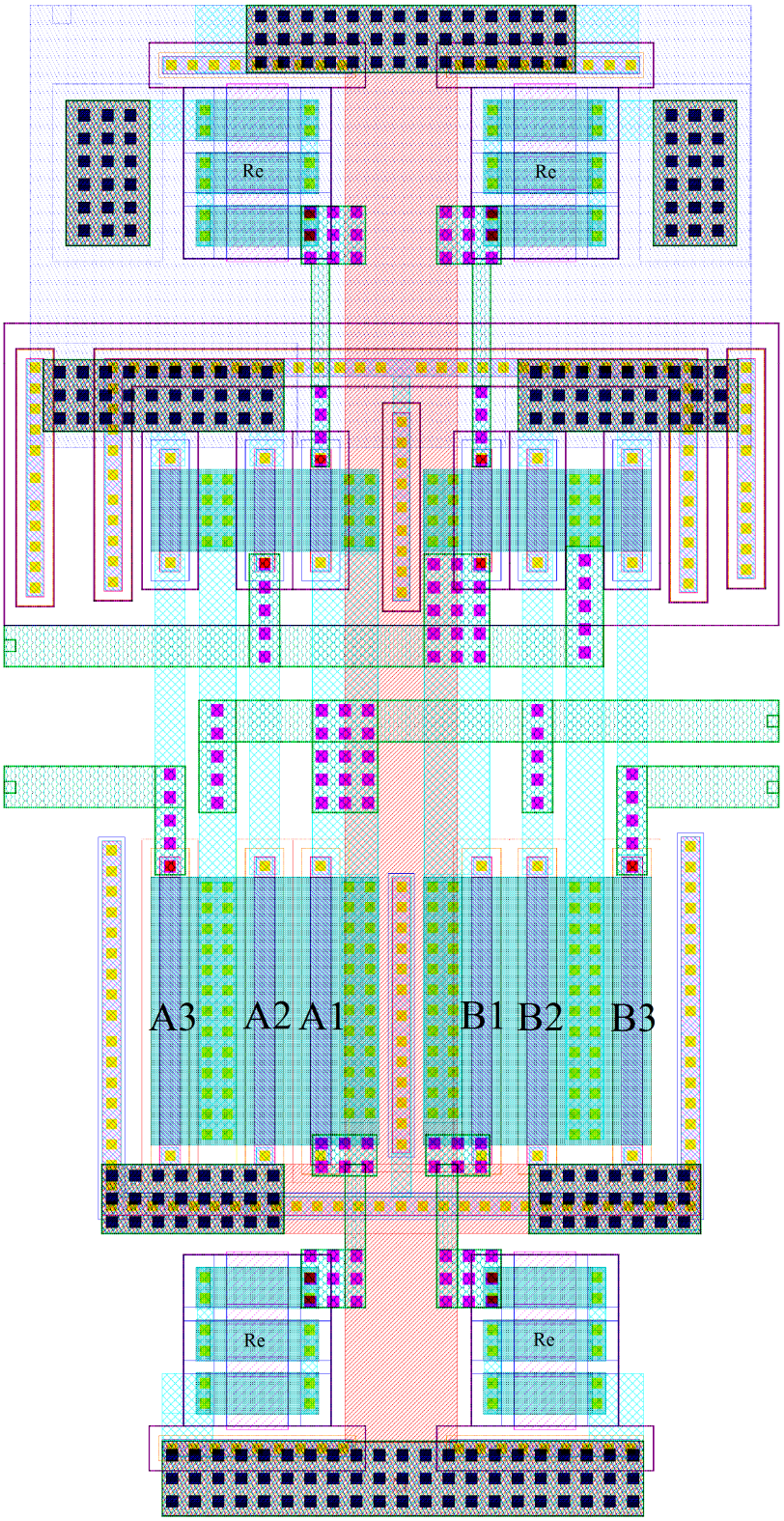

Figure 3.6. Layout implementation of Integrator unit.

4. Gain Stage, Comparator and DAC Circuit Implementation

In this chapter, a detailed study on the rest of the circuit blocks and their corresponding design constrains is conducted. Section 4.1 revolves around the I/V converter functionality and circuit and layout implementation. In Section 4.2, a voltage mode comparator circuit and layout is presented and simulations proving its functionality are demonstrated. Finally, the most prominent segment of this chapter, Section 4.3, introduces the challenges and design examples revolving around current mode CT DAC design.

4.1. Gain Stage

The lack of a proper current mode comparator imposes limits on current-mode delta Sigma modulators. Thus, it was decided to use a low power consuming conventional voltage comparator. As a result, an interface between the current mode blocks and the voltage comparator was deemed necessary. The output currents of both integrators are summed at the input of the gain stage. Thus, the circuit is to convert a nano-scale current into voltage while keeping the input node at a constant voltage by having a small input resistance. Moreover, it is essential to prevent having any extra poles in the loop in both the input and output of the gain stage which necessitates having low input resistance and converting current input signal into an output voltage with the least amount of phase shift. A modified version of [8] is incorporated in the design. The proposed circuit is depicted in Fig. 4.1. The input is composed of a couple of source follower transistors driven by a positive voltage feedback inverter. Such circuitry scales the input resistance to that shown in Equation 4.1. For compatibility with the integrator stages and mitigating power consumption, this segment is run under the 0.8V supply voltage.

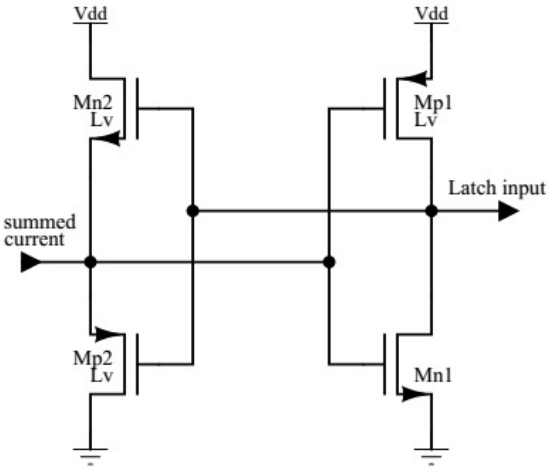

Figure 4.1. Gain Stage circuit.

$$R_{inconv} = \frac{1}{g_{mT}(1+G)} \tag{4.1}$$

where g_{mT} is the input transconductance without the feedback loop and G is the voltage gain of the inverter. The inverter is to have a low phase shift at the clock frequency of 12.8 MHz while maintaining a reasonable gain of at least 20dB. Thus, a power budget of $1\mu W$ was devoted to the converter to ensure critical performance. This unit also carries the duty of buffering out the kickback noise created by the Latch circuit as depicted in Fig. 4.3. This figure also points out the nonlinearity of the gain stage output. However, it is important to note that this circuit is not required to be linear since it drives a single bit comparator; thus, the trade off between linearity and power consumption is futile and best be avoided. The proposed device is not differential; it is composed of two single ended circuits. Thus, symmetrical layout drawing becomes a necessity for optimal performance of this unit. The layout implementation of the circuit is given in Fig. 4.2.

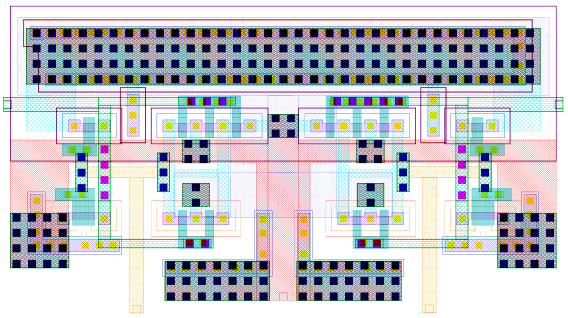

Figure 4.2. Gain Stage circuit layout.

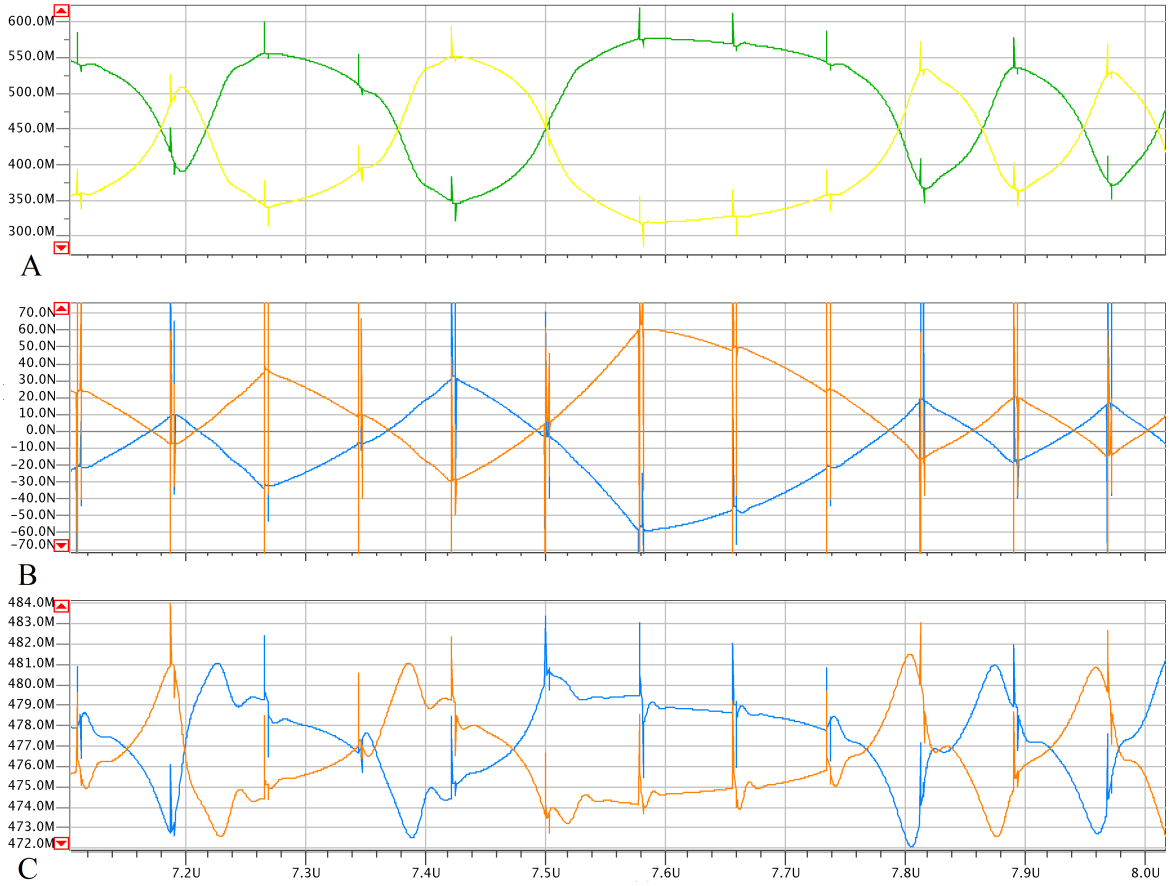

Figure 4.3. A gain stage output. B circuit current input. C voltage variations at input node.

4.2. Comparator Design

Fig. 4.4 depicts the latch circuitry [9] used for the design. It is of crucial importance to have a minimum amount of delay and a precision of sub millivolt since the design is run by only one latch and any mismatch or offset on this design would compromise the SNDR of the second order system. Consequently, a huge portion of power consumption is devoted to optimizing this segment. In spite of loop elements, this segment is run at a supply voltage of 1.2V to boost its accuracy and speed. The input transistors are of low threshold type so that the latch segment can interact with the low VDD segments of circuit. Transistors M1-M10 implement a classical clocked comparator circuit in which M3 and M4 are to isolate the input transistor from the cross coupled pair in reset phase, limiting power consumption while reducing the kickback noise imposed on the circuit. M9 and M10 are responsible for driving comparator outputs to VDD in the reset phase, paving the way for the next comparison to come. Transistors M11-M18 are to latch the results for a whole clock pulse. The reset phase of clock, which drives both comparator outputs to VDD, is to keep the previous value for comparators and thus holds the comparison for a whole clock period regardless of the clock pulse being in comparison mode or reset mode. Fig. 4.5 delineates the layout implementation of circuit. Latch output is not solely used as an output for the modulator. Both positive and negative outputs drive the feedback DAC. However, due to the DAC system implemented, the loop can tolerate any kind of delay and timing mismatch between positive and negative outputs, resulting in mitigated loop layout symmetry and timing requirements.

4.3. Feedback DAC

The signal imposed delay to the comparator for small inputs could have impairing effects on performance the same way clock jitter affects the circuit [1]. It is also the case that rise and fall time of the latch output are considerably large and unequal. Besides, the crossover point of the falling and rising latch signals is unpredictable and asymmetric regarding feedback transistor bias points. Such non-idealities would introduce uncontrolled and undecided feedback current to the circuit for short burst

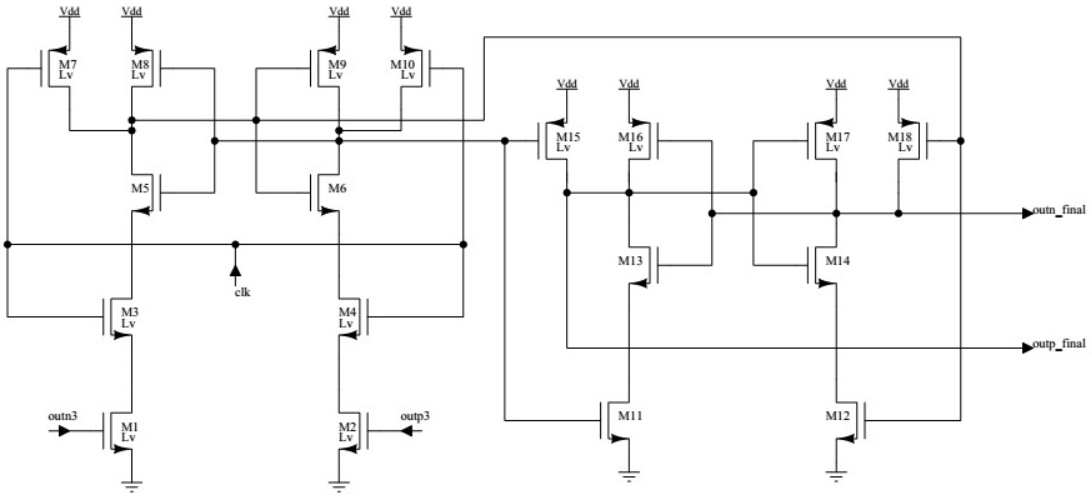

Figure 4.4. Latch circuit schematic.

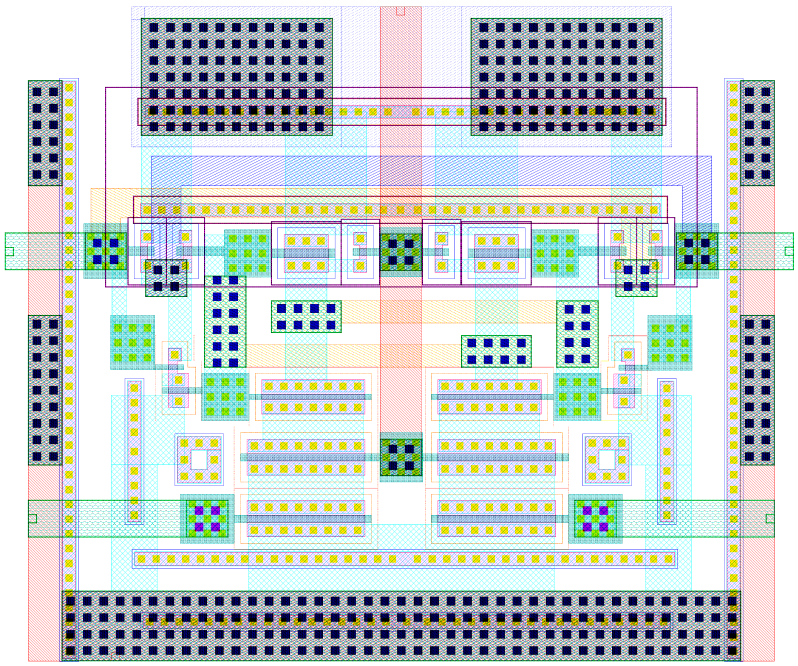

Figure 4.5. Latch circuit Layout implementation.

of time with negative effects on SNDR. Hence, it is best if a Return to Zero (RZ) feedback signal with sharp changing edges is used [1]. In this work a clock signal of 12.8 MHz with a pulse width of 3ns is implemented. The phase during which the clock value is high, is used as the return to zero period. Fig. 4.6 depicts the first proposed feedback architecture introduced in [1]. Fig 4.7 depicts the corresponding control

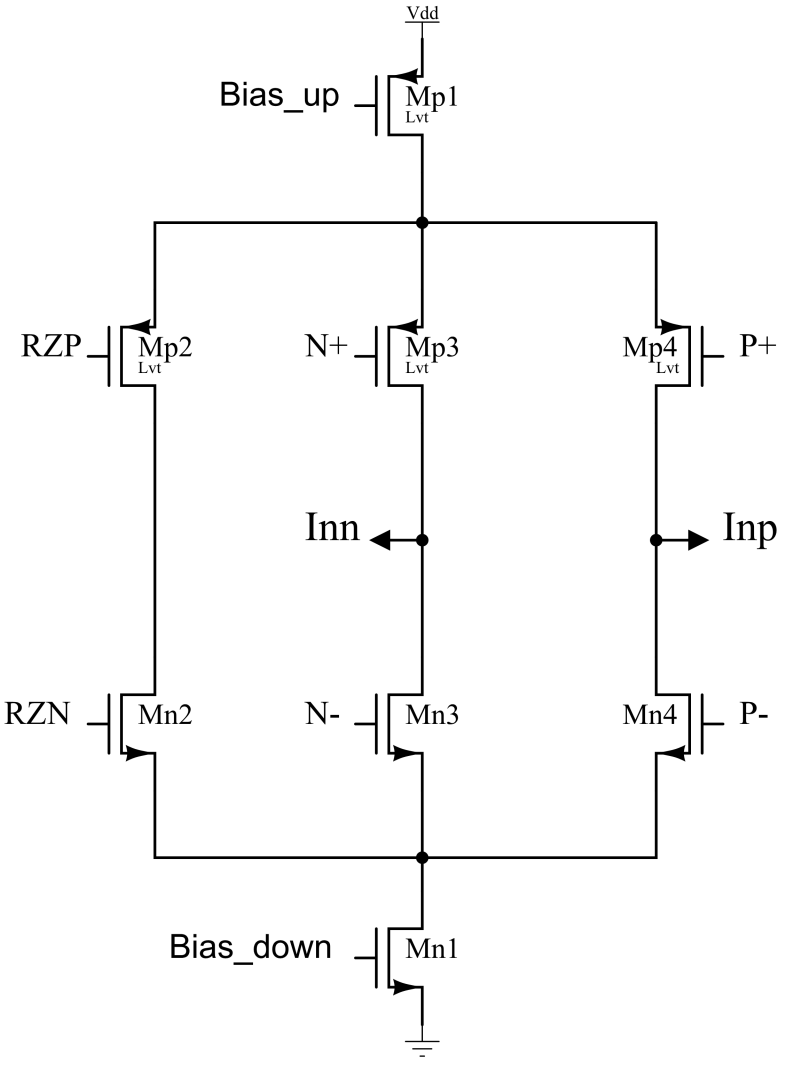

Figure 4.6. Feedback DAC introduced by [1].

signals. The logic driving the signals is written in Equations 4.2, 4.3, 4.4 and 4.5. It should be noted that the latch circuit is not affected by the short clock pulse width since it demonstrates a maximum delay of 1.5 ns. This switching architecture is data

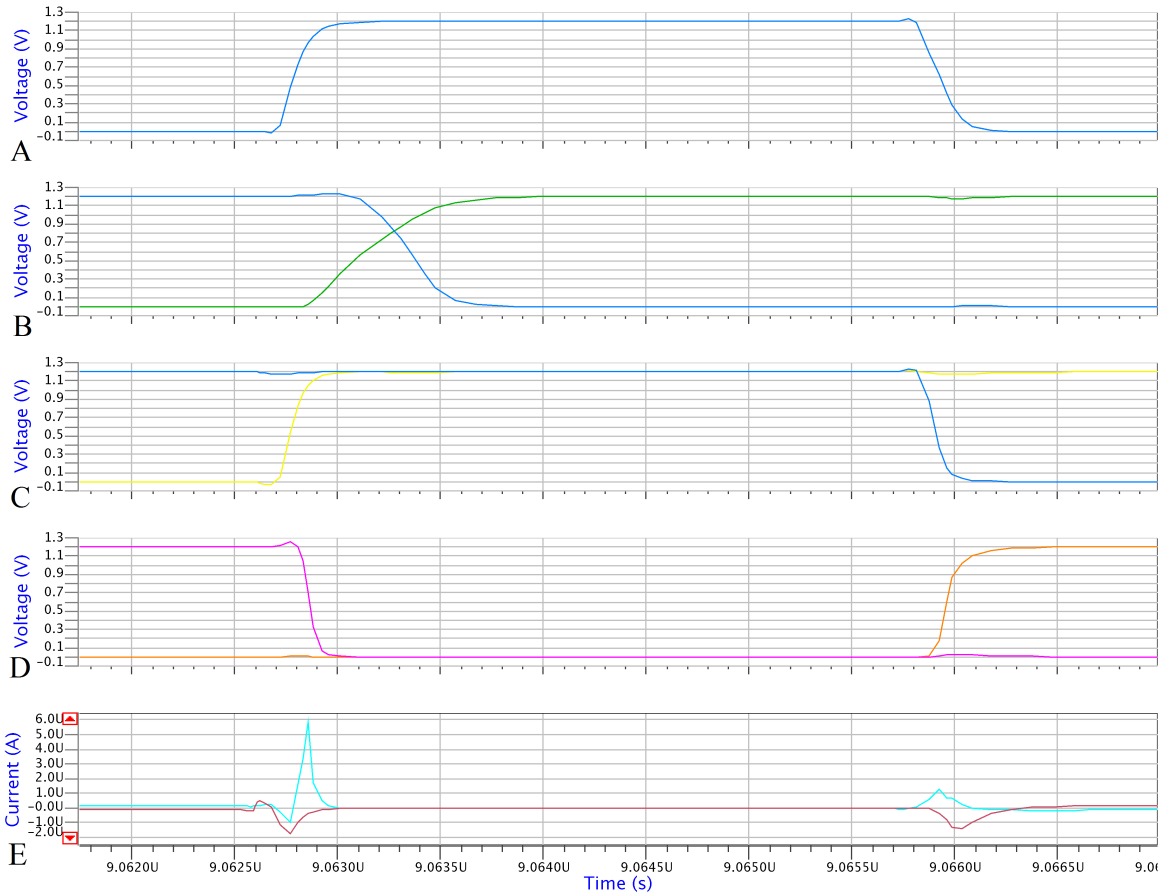

Figure 4.7. A: loop Clock pulse. B: Latch output waveforms C: P+/P- functions. D: N+/N- functions. E: Feedback current output.

independent and so is the feedback charge injection. Consequently, no excess noise is produced.

$$P+ = \overline{RZP\&OUTn} \tag{4.2}$$

$$P- = \overline{RZP\&OUTp} \tag{4.3}$$

$$N+ = \overline{RZN\&OUTn} \tag{4.4}$$

$$N- = \overline{RZN\&OUTp} \tag{4.5}$$

where RZP is the complementary signal to the buffered global system clock, RZN. OUTn and OUTp signals are latch differential digital outputs. During the RZ phase, the negative and positive current paths are connected together through the dummy path composed of Mp2 and Mn2. As a result, the flow of current sources is never interrupted and the voltage on the mirrors is kept constant, thus eliminating the excess time required to charge these nodes after the RZ phase. As indicated in Fig. 4.7 part E, huge stray currents are observed during the switching phase. The reason is that the path that connects the positive and negative integrating capacitances of first integrator through a chain composed of Mn4, Mn2, Mp2 and Mp3 or Mn3, Mn2, Mp2 and Mp4 during the rising and falling edges of control signals. The observed phenomenon has pernicious effects on system accuracy since it discharges integrating capacitances. Consequently, a new feedback circuit is introduced to mitigate the addressed charge sharing issue. Fig. 4.8 delineates the proposed schematic. The Transistors Mp6 and Mp7 buffer the integration capacitances away from one another, ensuring short circuits

between the two capacitances never occurs. The new switching scheme is different in

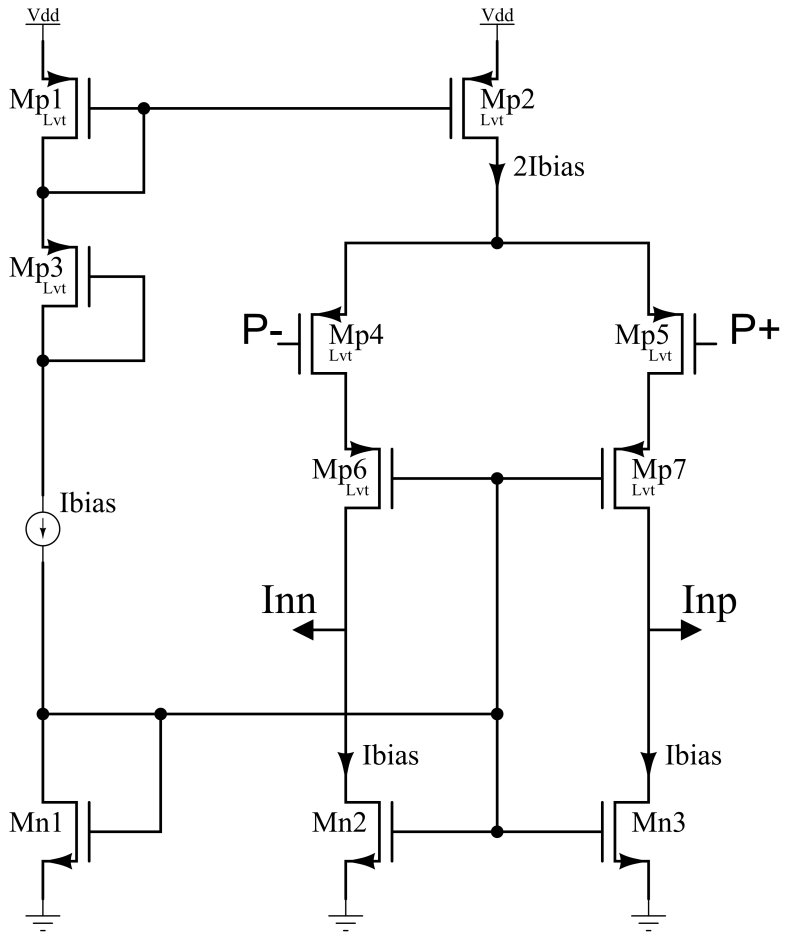

Figure 4.8. Proposed Feedback circuit.

the sense that during the reset phase, both Mp4 and Mp5 switches are on, dividing the $2I_{bias}$ current between the positive and negative branch, bringing the circuit output current down to zero. Fig. 4.9 delineates the acquired current output. The switch and buffer transistors incorporate minimum dimensions to reduce the time it takes for a buffer to turn off and the other one to accumulate enough charge for doubling its current flow. As implied by Equations 4.6 and 4.7, the proposed structure does not require a complementary clocking signal since signals P+ and P- only require the RZN clock signal to drive them. Consequently, the amount of digital circuitry required for loop functionality is almost reduced by half, increasing accuracy and reducing digital power consumption.

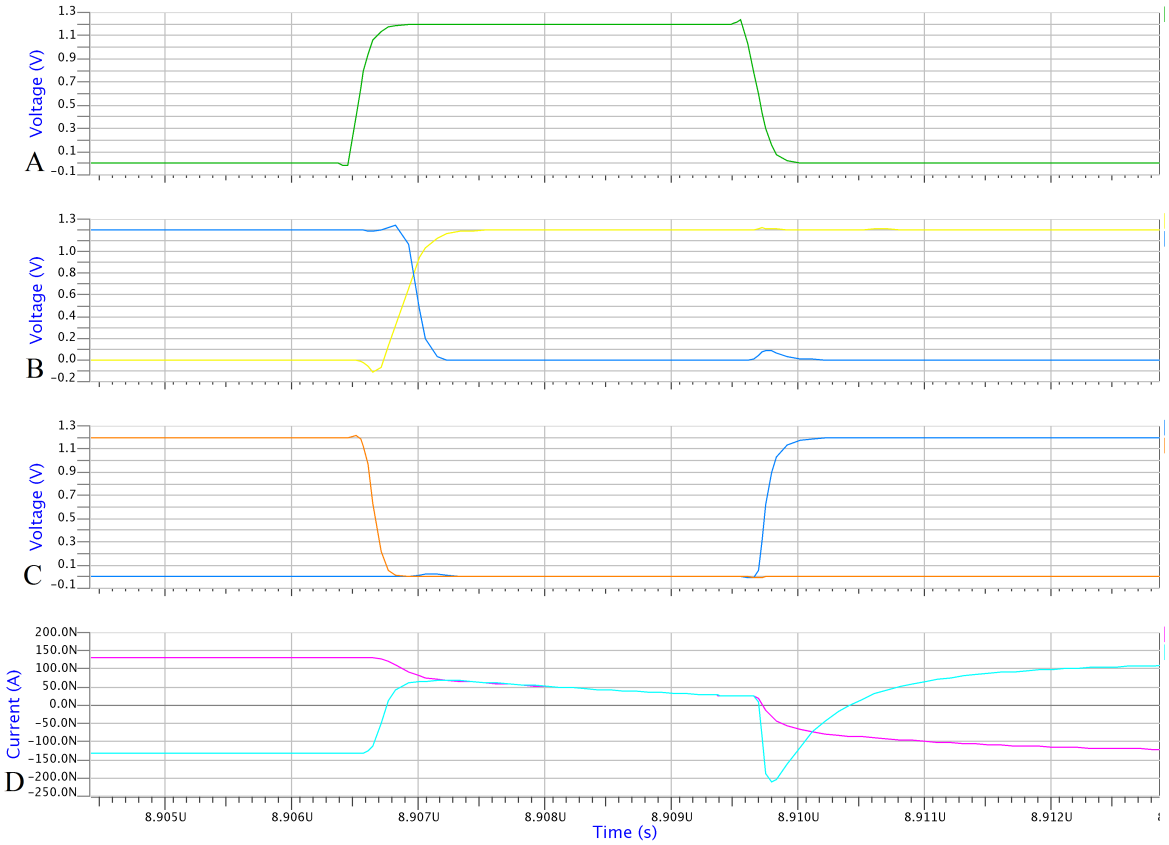

Figure 4.9. A: loop Clock pulse. B: Latch output waveforms C: P+/P- functions. D: Feedback current output.

$$P+ = \overline{RZN \& OUTn} \tag{4.6}$$

$$P- = \overline{RZN \& OUTp} \tag{4.7}$$

It should be noted that for compatibility with the latch circuit, the feedback circuit operates under 1.2V. This decision does not interfere with the first integrator input. The transistors Mn2 and Mn3are long, thus, the overall output resistance of the DAC is large enough not to affect Equation 3.8 to a great extent. Although mismatch between positive and negative current outputs is not of concern and can be considered as input offset, the mismatch between positive and negative outputs when circuit output is 1 and when it is 0 can have pernicious effects on overall SNDR, increasing system noise in form of a second harmonic signal. Thus it is crucial to have identical transistor pairs with symmetrical layout design. Fig. 4.10 depicts the implementation of proposed circuit. The circuit is drawn as compact as possible to minimize the effects of random process variation, thus, avoiding any mismatch.

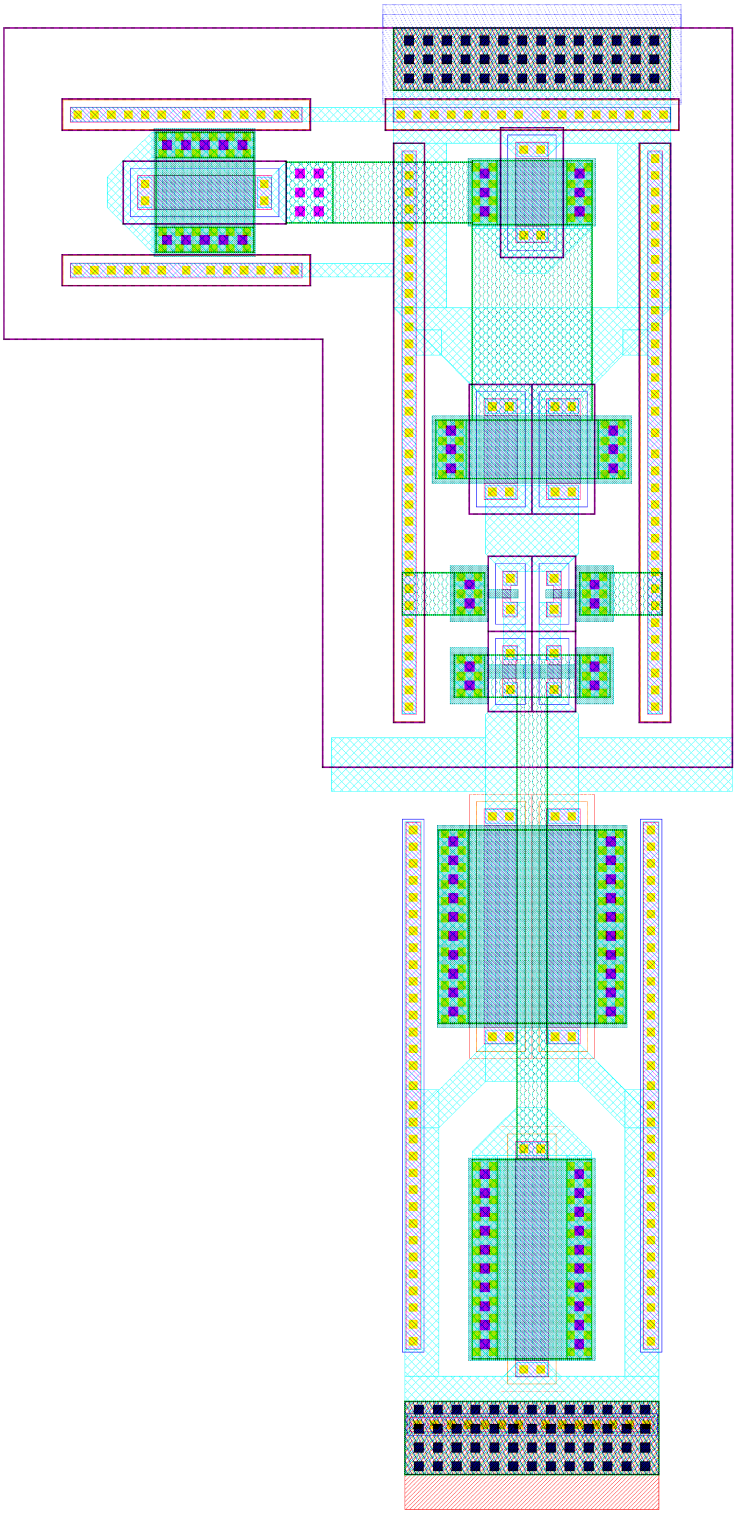

Figure 4.10. Proposed Feedback circuit.

5. Circuit Implementation and Simulation Results

In this chapter, circuit implementation constrains and final simulation results are presented. Section 5.1 revolves around design specific implementation issues and solutions. The implemented circuits are analyzed in a system scope, interacting with the rest of components. A voltage input alternative to system implementation is also proposed in this section. In Section 5.2, power performance of both proposed systems and their components are analyzed. An insight to power consumption distribution in the system is presented as well. Section 5.3 discusses circuit precision in postlayout and schematic simulation and the performance loss endured due to such an implementation. Finally, a comparison with the with the literature based on a global Figure of Merit, FOM, is conducted in section 5.4.

5.1. Overall Circuit Implementation

The block diagram of the overall circuit is depicted in Fig. 5.1. The two integrators are marked as integrator 1 and 2. Integrator 2 does not possess an output stage since the current adder stage performs that duty instead. Fig, 5.2 depicts the current adder block. It acts as an output stage for integrator 2 and as a feed forward path for 1. These circuits are compiled into a single compact block for perfect matching between coefficients. Since the output of current adder block is directly connected to the gain stage input, the low input resistance of this block prevents the voltage on current adder block output stage to vary out to nonlinear regions, ensuring linear circuit functionality. The overall circuit layout is provided in Fig. 5.3. The dimensions are $110\mu m \times 215\mu m$ consuming a total area of $23650\mu m^2$. The capacitances are implemented as depicted in Fig. 5.4. The clock distribution is only between the latch Stage and DAC driver unit. Thus, it was decided to draw these two blocks in close proximity to clock distribution unit as shown in Fig. 5.3. Doing so, the effects of clock jitter can be mitigated to some extent. Extra care was spent to ensure that the input ports are as symmetric as possible. Thus, the input is directly connected to Metal 5 layer of input capacitances, reducing the input resistance to that of a relatively large

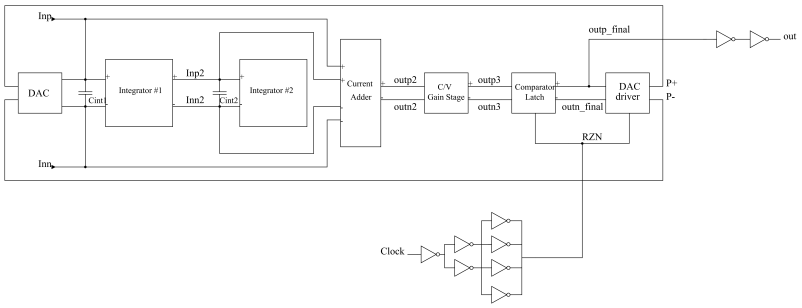

Figure 5.1. Proposed Feedback circuit.

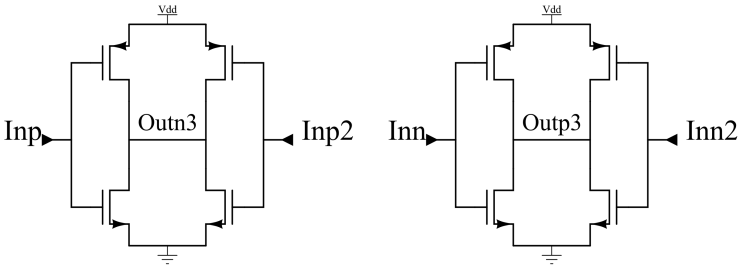

Figure 5.2. Current Adder Block.

Metal 6 to 5 via. The current adder circuit layout is depicted in Fig. 5.5. This circuit reads the voltage of each capacitance, converting the signal back to current for a final summation at the low resistance input ports of gain stage circuit.

Three versions of this circuit were implemented on chip as shown in Fig. 5.6. The original version of the circuit, the reduced input capacitance and a voltage mode input. The decision spans from the fact that the proposed loop is a current mode circuit with capacitance at input node. The main problems with such implementation is that building a fully differential current input regardless of the loop input voltage is challenging. It is also the case that there is an unknown amount of wiring and port capacitance at the input of circuit. This amount is unfortunately not documented in design kit and the added wiring makes it very hard to find the exact number with simulation. Thus as a safety factor, a second loop with 20% less input capacitance was also included in the chip. Another instance of circuit is drawn with internal voltage to current conversion capabilities. The voltage mode input is immune to the input capacitance uncertainty effect since a voltage input neglects the wiring capacitances, and is directly transfered to input. The circuit is depicted in Fig. 5.7. The input is directly transfered to the resistor R_{in} where it is converted to current and forwarded to the current mode circuit input. The use of resistor is essential to ensure a linear transformation. Linearity is of extreme importance since any nonlinearity would affect circuit precision in form of a third harmonic. Fig. 5.8 demonstrates the layout of the voltage mode circuit. The dimensions are $342\mu m \times 371\mu m$ with a total are of $126882\mu m^2$ which is almost 5.4 times bigger than the current mode circuit. The capacitance on the input bias points are for ensuring DC stability. This is the case since the bias circuit for this stage is internal. There are no precision requirements on this stage's biasing, so it was decided to have a separate biasing stage for this circuit through a large internal resistance. The noise contribution of input resistance is not a concern since the noise attribution of the $1M\Omega$ input resistance pales away in comparison to the contributions the enhancement resistor of first integrator as shown in Equation 3.13. The circuit of the enhancement architecture is fully differential, Consequently, there are less constraints on layout symmetry and circuit susceptibility

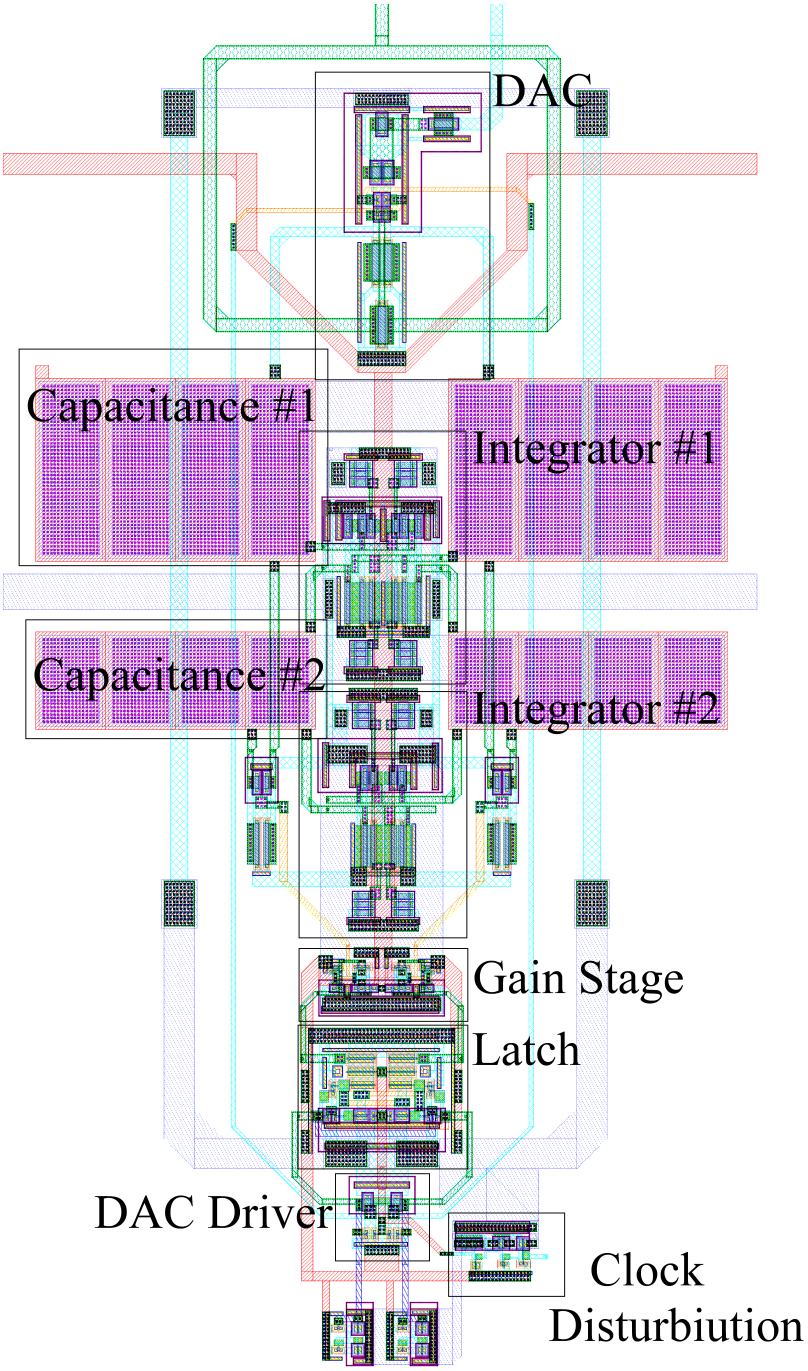

Figure 5.3. Overall Circuit layout.

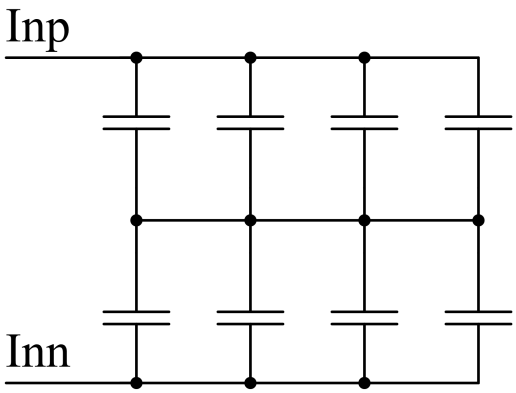

Figure 5.4. Capacitance placement in Circuit.

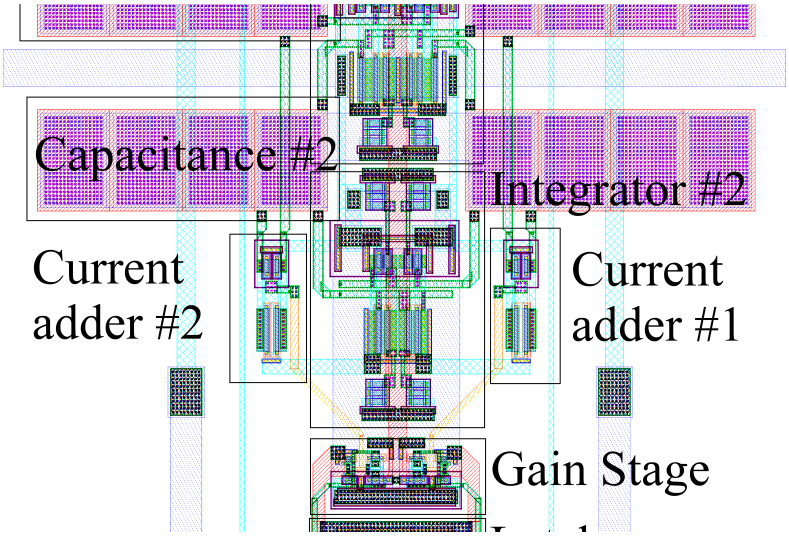

Figure 5.5. Current Adder Circuit Layout implementation.

to second harmonics. Such attribution causes the design to be more immune to extreme process variations.

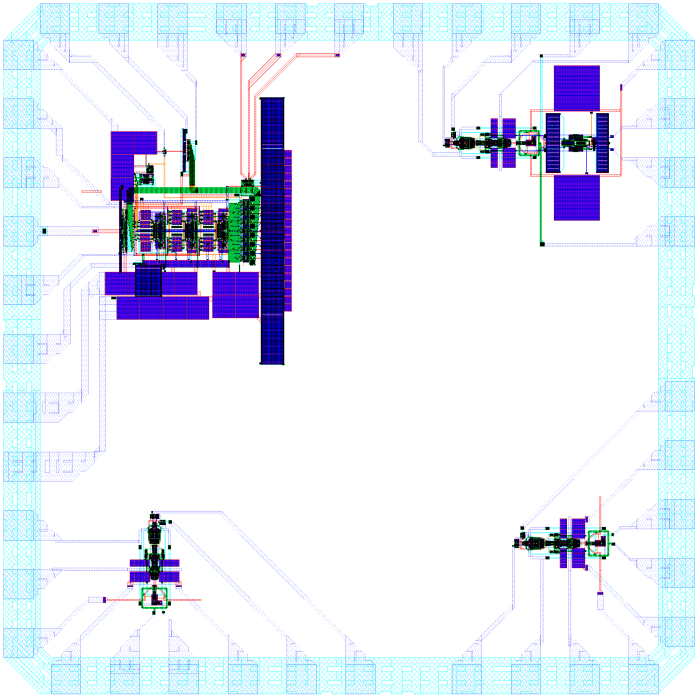

Figure 5.6. Overall Chip Design.

Fig. 5.9 depicts the loop implementation coefficients. Elements are designed such that they fulfill the following criteria:

$$\frac{kF_s}{s} = \frac{G_3}{Cs} \tag{5.1}$$

where the operand G_3 represents the transconductance of the A_3 and B_3 inverters from Fig. 3.1. The value of G_3 is approximately $2.7\mu S$. Thus the value of first and second integrator capacitances are $560fF$ and $290fF$. The value of G_3 is susceptible to change due to process variations as well as the value of capacitances. Consequently, a tuning mechanism is to be implemented. A closer inspection to the values of Table

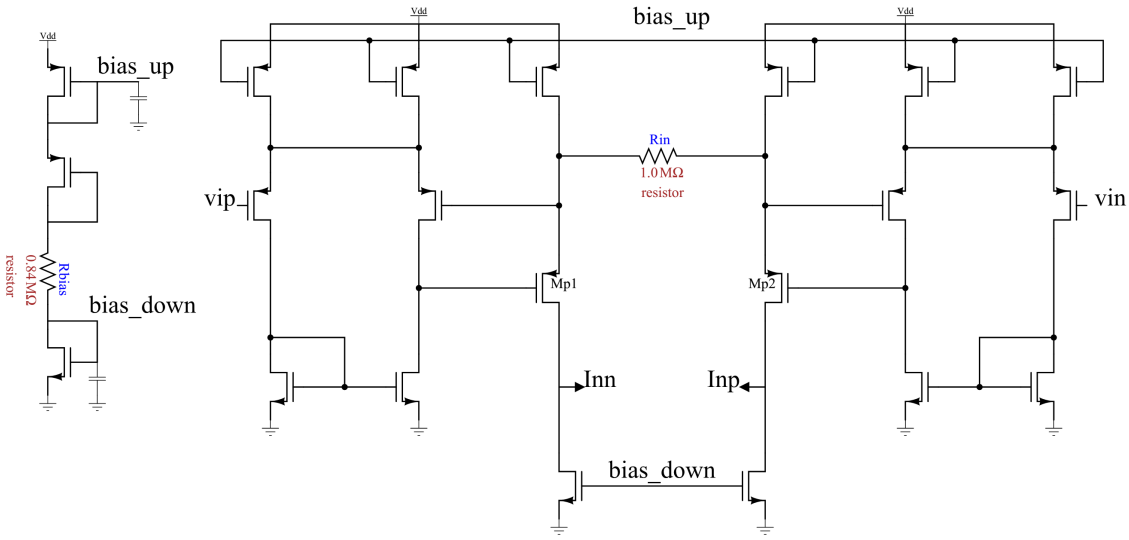

Figure 5.7. Voltage mode circuit interface.

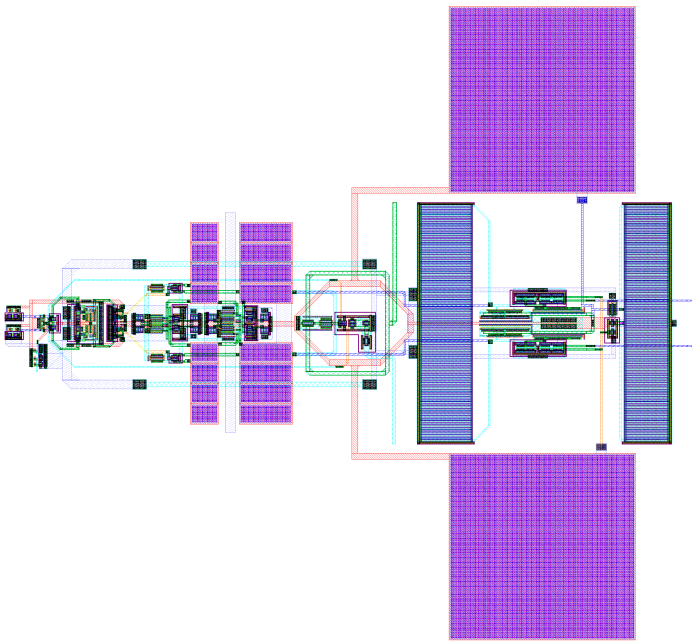

Figure 5.8. Voltage Mode circuit layout.

2.2 indicates that the SNR is dependent on the value of k_2 whereas the variation of integrator outputs are dependent on k_1. Thus, it is possible to fine tune the value of k_2 through changing the 0.8V supply voltage of both integrators. Only large variation of k_1 can harm circuit linearity, consequently small changes on supply voltage does not have pernicious effects on overall linearity. Fig. 2.5 indicates that the output

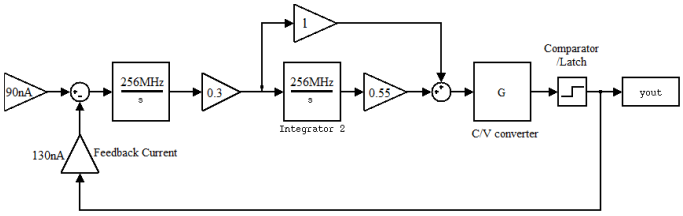

Figure 5.9. modulator characteristics.

variations of each integrator maximally reaches half of the feedback value. In the case of the implemented circuit, the feed back current is 130nA which would mean that a maximum output of 65nA will be observed as depicted in Fig. 5.10 A and C. However, it should be noted that the output voltage variation is relatively low, since the outputs are connected to large capacitances. Consequently, integrators do not abandon their linear region of operation. The maximum observed voltage deviation is 20mV from the DC operation point of 475mV. The DC current of each inverter in the integrators is chosen twice the maximum deviation value of 65nA. Since integrators are composed of 6 inverter units, the total DC supply current is 780nA and the overall DC power consumption is 624nW.

It was stated in Section 4.1 that the phase delay of the gain stage is critical and is better kept to a minimum. Thus, the transistors Mn1 and Mp1 from Fig. 4.1 are scaled to $\frac{0.24\mu}{0.8\mu}$ and $\frac{0.3\mu}{0.4\mu}$ respectively to ensure the transfer function depicted on Fig. 5.11. A rough estimation of the transimpedance of this stage is depicted on part B of the same figure. Due to relatively small scaling of transistors, each stage consumes about 600nA of current, and a total power of 960μW.

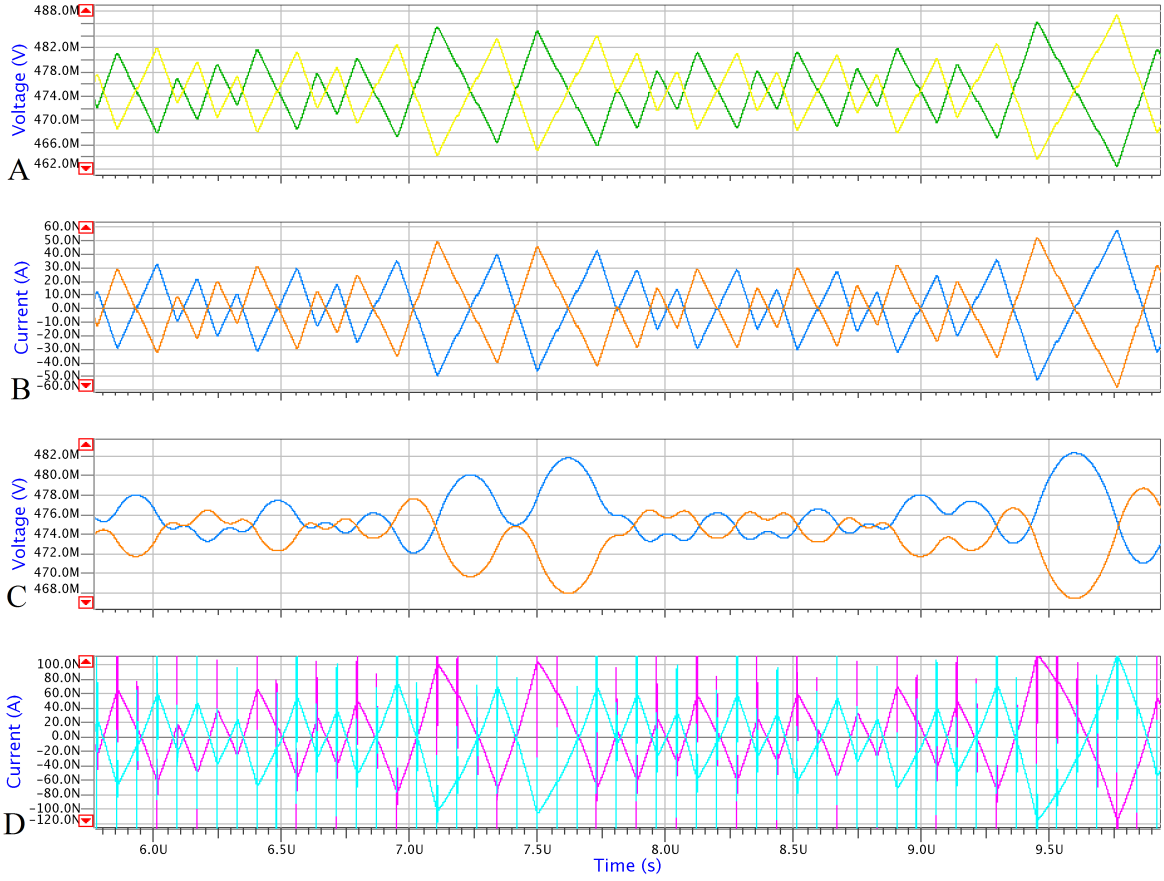

Figure 5.10. A: voltage variations on first integrator. B: Current output of first integrator. C: Voltage variations on second Integrator. D: Current variations on second integrator.

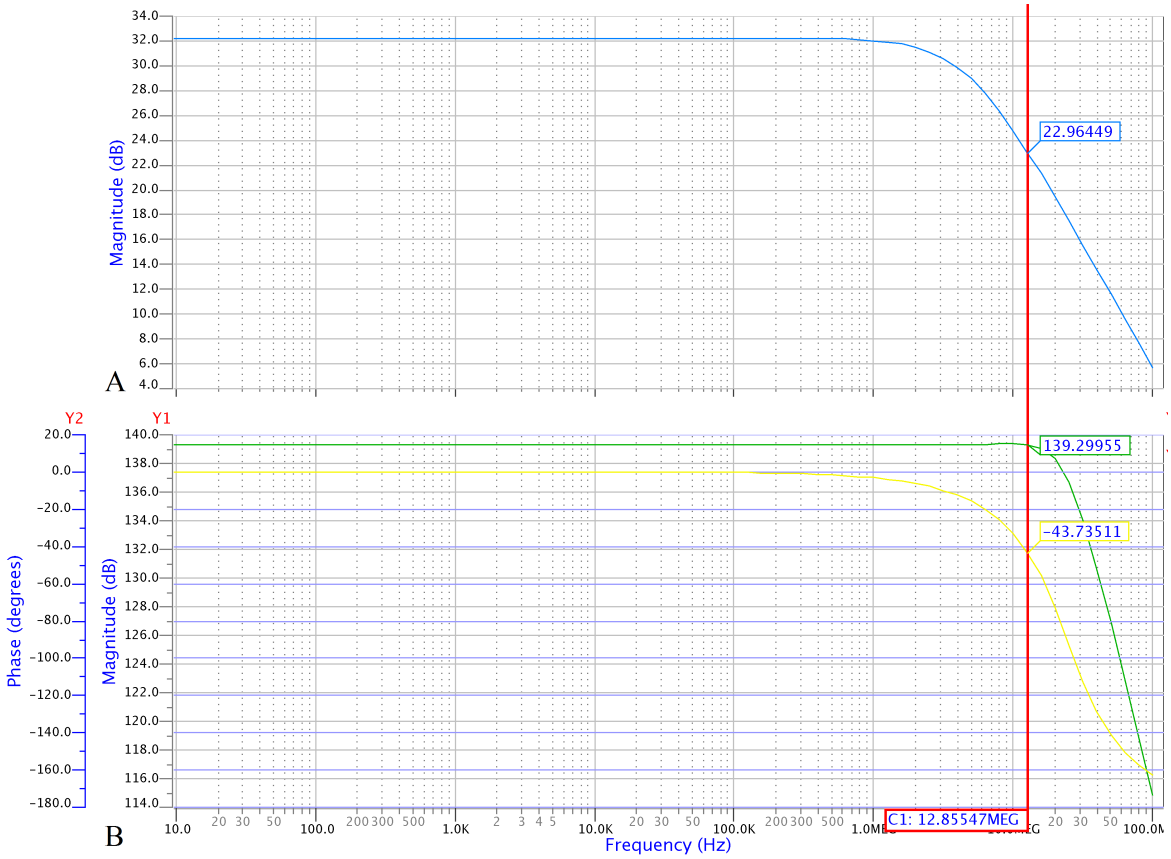

Figure 5.11. A: Gain Stage inverter transfer function. B: Transimpedance and total phase of stage.

Table 5.1. Simulink results for an over damped system $\xi = 0.9$.

Component	Power Consumption
Integrator 1	943nW
Integrator 2	719nW
Current Adder	675nW
Gain Stage	1188nW
Comparator/Latch	910nW
Clock Driver	884nW
DAC driver	98nW
DAC	443nW
Output Buffer	100nW
V/I converter	2348nW

5.2. Power Performance

Great effort is put into equalizing and reducing the power consumption of each component. The simulation results indicate that the overall power consumption of current and voltage input circuits are 5.967μW and 8.4μW respectively. The power performance of each individual cell is as depicted on Table 5.2. A comparison of each cell's power performance is represented in Fig. 5.12 and 5.13. It is evident that the addition of the V/I converter has a certain toll on circuit power consumption. However, this sacrifice is necessary to ensure overall linearity.

5.3. Circuit Precision

The SNDR results of the circuit are acquired through transient simulation using Mentor Graphics Eldo simulator with UMC 180nm design kit. Euler solution method is implemented instead of the classical trapezoidal approach. Since the circuit is in current mode, a Trapezoidal solution causes an oscillation in the outputs of DAC unit as depicted on Fig. 5.14. Thus, the command line ".option be" is to be included in circuit the netlist. The formula for extracting the estimated number of bits, ENOB, is a derivation from Equation 1.12. The relation is as shown on Equation 5.2. It should be noted that the large DC signal seen on some of the SNDR figures are due to DC

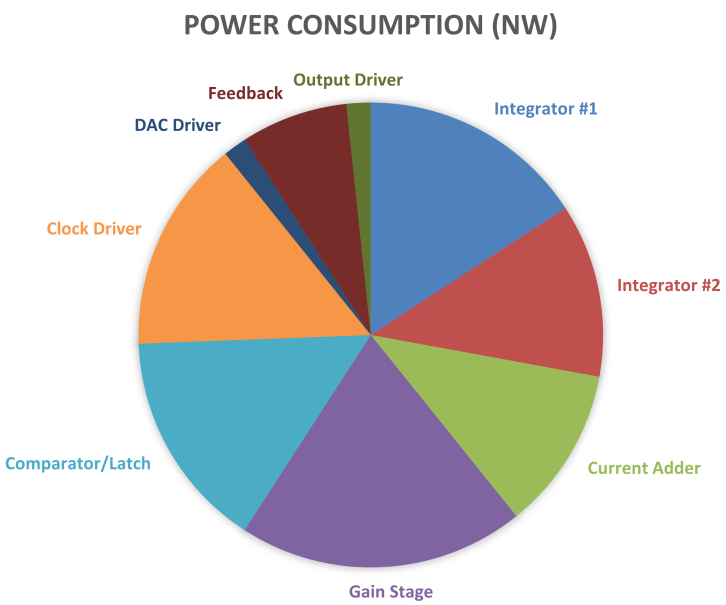

Figure 5.12. Power Consumption ratio of each individual cell in Current mode modulator.

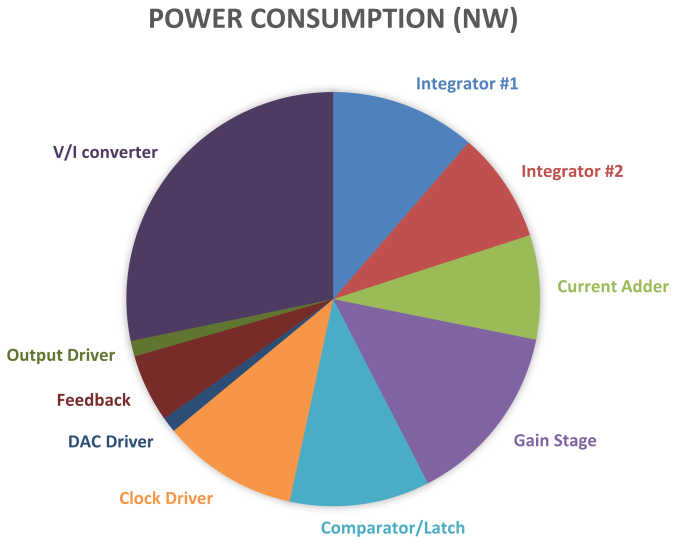

Figure 5.13. Power Consumption ratio of each individual cell in Current mode modulator.

offset and do not have negative effects on system functionality, or stability.

$$ENOB = \frac{SNDR_{db} - 1.76}{6.02} \tag{5.2}$$

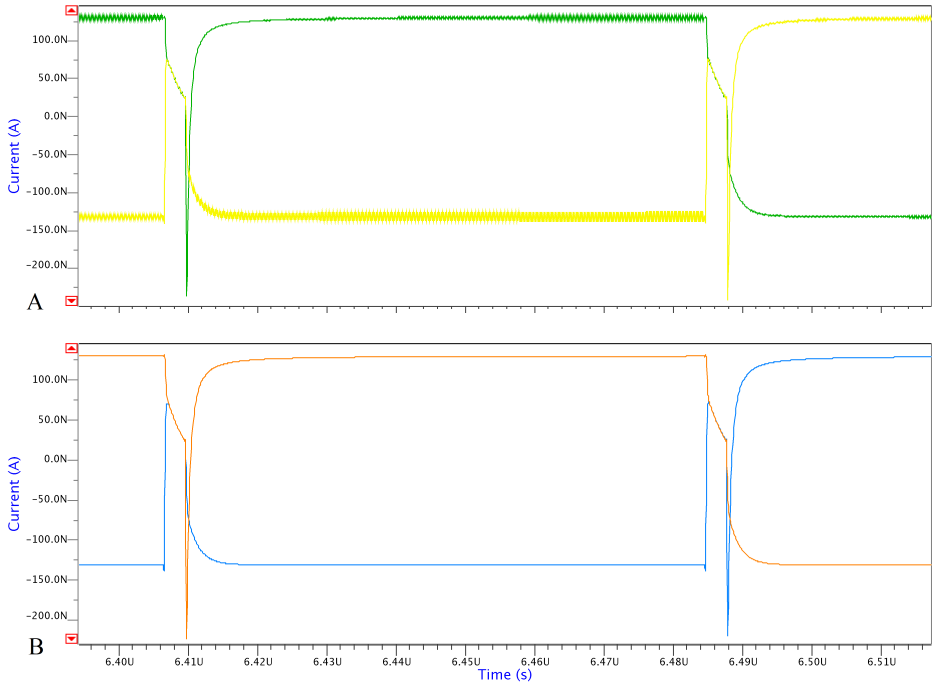

Figure 5.14. DAC output current with A: Trapezoidal and B: Euler solution.

Simulation outputs are then analyzed with Matlab for SNDR and ENB results. The overall SNDR of the schematic representation of the design is depicted in Fig. 5.15. The overall SNDR is 97.5 dB incorporating 131072 data points with an input amplitude of -3.19 dB which corresponds to an input of 90 nA in comparison to the feedback signal of 130nA. The layout implementation of Fig. 5.3 demonstrates the performance shown in Fig. 5.16. It is evident that a second and third harmonic are added to the circuit. However, the noise floor is identical to that of the schematic simulation. The overall SNDR is 94.4 dB which is tolerable compared to the acquired 97.5 dB. The voltage mode circuit presented in Fig. 5.8 establishes the results of Fig. 5.17. A slight increase in noise floor is observed as well as increased third harmonic.

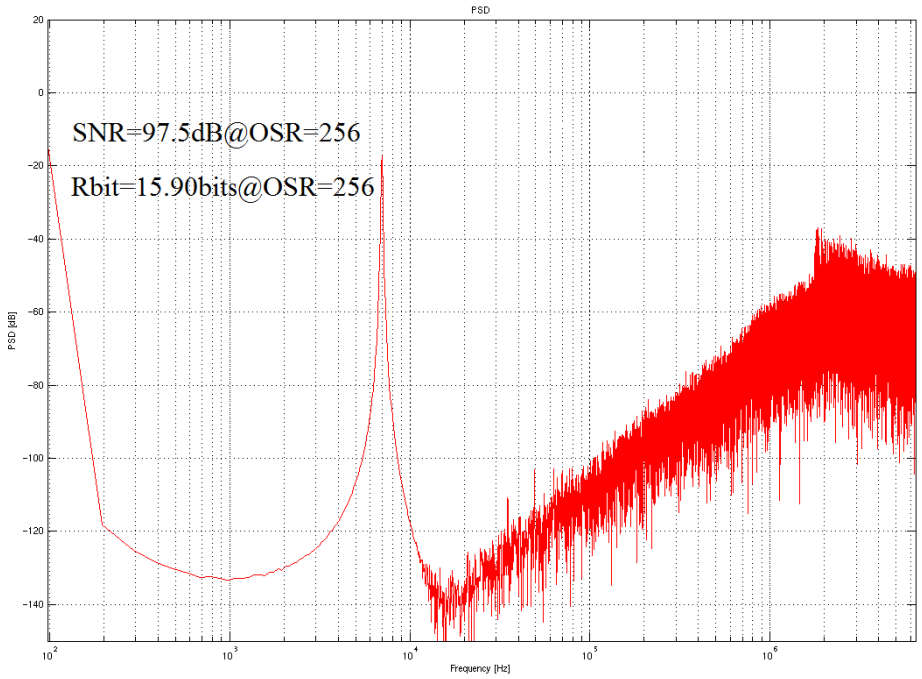

Figure 5.15. Results of Schematic mode simulation.

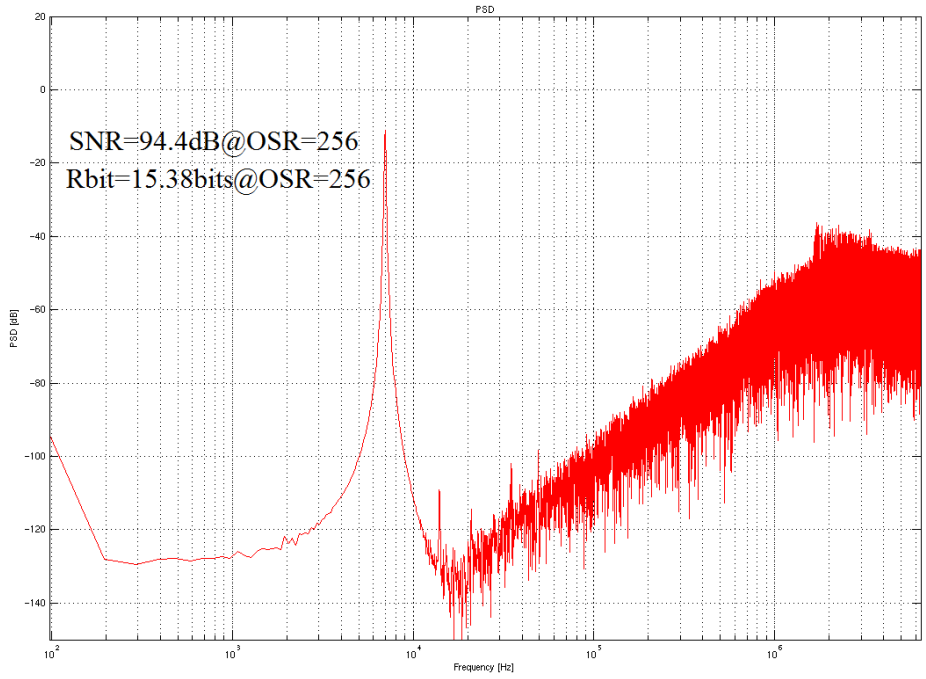

Figure 5.16. Post layout simulation results of Current mode circuit.

This effect impairs the circuit precision, decreasing the SNDR to 87.2dB, a 7.2 dB loss of precision. The dynamic range of the design, is also provided in Fig. 5.18.

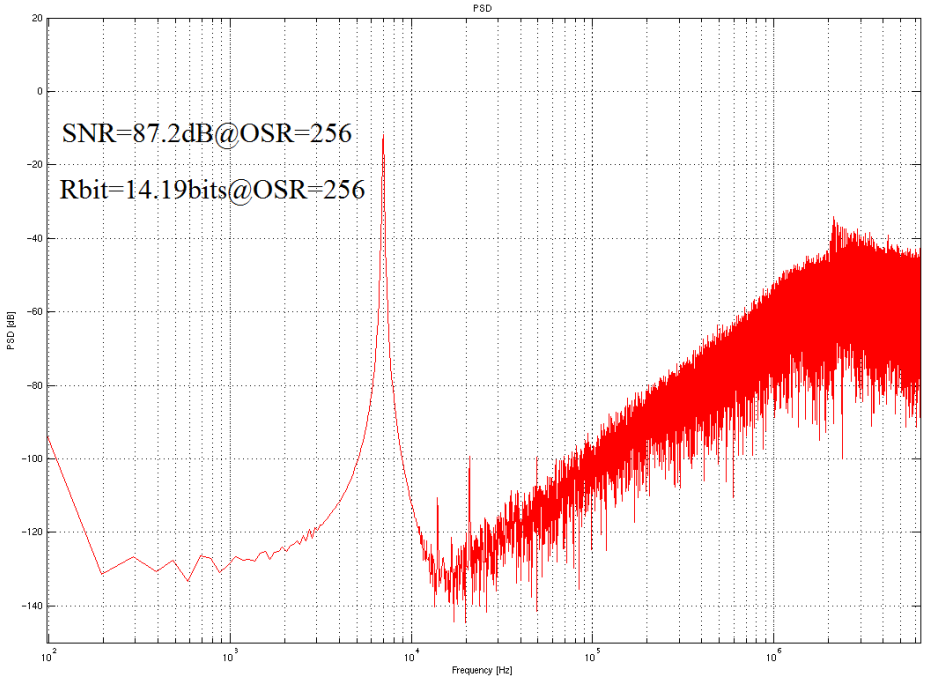

Figure 5.17. Post layout simulation results of Voltage mode circuit.

5.4. Performance Comparison

A comparison between acquired results and several results of similar state of the art designs is presented in Table 5.4. The comparison is conducted through a global data converter figure of merit as represented in 5.3. It is evident that the best acquired figure of merit is six times better than the best attained results in the state of art designs. Thus, it is safe to assume that the attained results are extensively satisfactory. However, it should be stated that The provided data is the result of postlayout simulations where as the comparison subjects are all chip implementation results published in peer reviewed Journals.

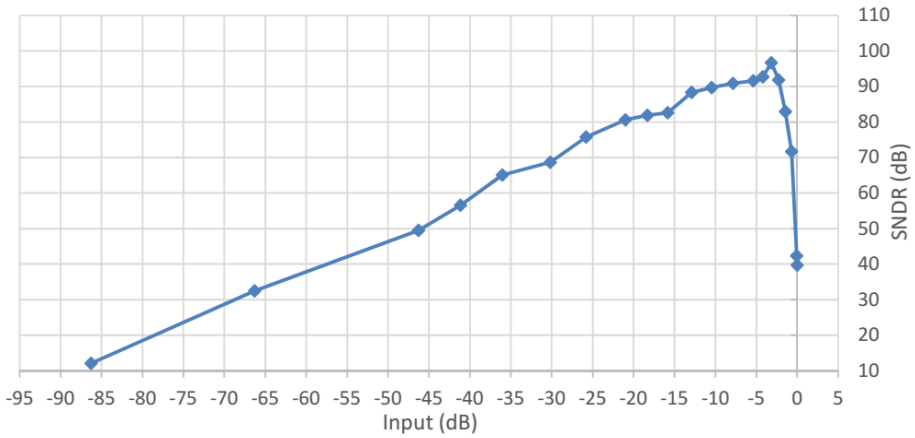

Figure 5.18. Dynamic Range of Proposed Sigma-Delta modulator.

Table 5.2. Comparison results of proposed modulator with literature.

Ref	**Tech**	**Power**	**BW**	**OSR**	**SNDR**	**FOM(fJ/conv)**
[10]	180nm	90μW	24KHz	64	93.5dB	54
[11]	180nm	90μW	24KHz	64	93.5dB	49
[12]	130nm	28.6μW	20KHz	64	79.1dB	97
[13]	130nm	42.6μW	20KHz	64	97.3dB	17
[14]	180nm	38μW	8KHz	128	92dB	73
Current mode Circuit	180nm	5.97μW	25KHz	256	94.4dB	2.8
Voltage mode Circuit	180nm	5.97μW	25KHz	256	87.2dB	8.98

$$FOM = \frac{Totalpower}{2 \times BW \times 2^{nbits}} \tag{5.3}$$

6. Conclusion and Future Work

In this work, several concepts of CT $\Delta\Sigma$ have been reviewed:

- **Fundamental differences between CT and DT circuits:**
  Several design aspects and performance differences between CT and DT data converters have been studied. It was concluded that while DT circuits are best suited for high frequency operation due to their clock jitter and excess loop delay immunity, CT circuits have superior perfromance advantages in low frequency and low power design paradigms. This is due to the fact that no switches are used in the circuit design, which eliminates the need for large supply voltages and mitigates biasing constrains on active components and reduces the need for high slew rate opamp design. The CT modulator also has inherent anti aliasing filter, thus redeeming the need for an external one.
- **A simple design method for CT loops:**
  The lack of a proper DT to CT and direct continuous time design tool, signified the need to build a simple tool for pragmatic loop design. A methodology for designing a second order CIFF loop is proposed by modeling the loop as a second order system and using multiple damping and feed forward coefficients as sweeping parameters. The best scenarios are selected based on their maximum integrator output variation and SNDR results. The solutions are later fine tuned to acquire the optimum performance point.
- **C-gm integrators:**
  A new approach to C-gm integrators introduced by [1] is presented. The resulting circuit is able to perform under extremely low supply voltages while consuming minimal power and operating in a linear region. The proposed circuit does not require a control circuit. The tuning can be conducted through varying supply voltage. A boosting method is introduced to mitigate node resistance and increasing DC gain of integrators. The proposed C-gm filters require relatively low chip space which makes them suitable for sensory arrays.
- **I/V converter gain stage:**

The circuit proposed in [8] is incorporated to act as an interface between current mode segments of the circuit and the voltage mode comparator/latch system. The block acts as a gain stage to the comparator while preventing the kickback noise to corrupt the integrated signal on capacitances. The proposed circuit is composed of inverters, thus, it is fully compatible with the low supply voltage incorporated in C-gm integrators.

- **DAC circuit**

  A current mode DAC design proved to be a very problematic stage of work since it can produce second harmonics and excess noise floor if not designed properly. A low power consuming replacement to the DAC introduced in [1] is presented which does not require complementary clock signals and has redundant digital control signals. The proposed DAC has output buffer stages to keep the integrating capacitances from discharging on clock edges, preventing incrementation of noise floor. The proposed circuit is fairly small and thus, it is easy to balance the positive and negative port outputs, preventing unwanted second harmonics.

- **Voltage mode circuit:**

  It is challenging to provide the current mode system with a truly differential input. Furthermore, due to the nature of C-gm integrators, the first integrating capacitance is in the input node. Consequently, the unknown chip port capacitance may influence the loop coefficients of system. Two solutions are taken into account. A current mode circuit is represented with 20% less input capacitance and a voltage mode circuit is introduced. The latter, incorporates a V/I converter unit in its input. Thus, the input voltage is converted into current and injected into the circuit. The conversion has to be linear to avoid the third harmonic caused by the conversion to harm circuit performance. Thus, a large resistance is used as the main component for the V/I conversion. The postlayout simulations indicate that the circuit has acceptable results, yet not the optimum performance its current mode counterpart demonstrates.

- **Chip Implementation:**

  The three introduced designs were taped out to fabrication together with a DT circuit. The proposed circuits consume very little space with minimal number of

ports compared to the DT counterpart.

6.1. Future Work

Several design expansion points seem to be of interest:

- **Higher order loop with voltage mode and passive elements:**
  While having efficient power and linearity performance, C-gm circuits have general shortcomings of current mode circuits. Expanding the loop order using a proper design tool, it will be possible to have voltage mode integrators and passive integrating components in system. Voltage mode integrators would act as an interface with the outside world while passive elements will be incorporated to enhance power consumption versus circuit precision.
- **Hybrid loop implementation:**
  Hybrid loops can be implemented to accumulate the merits of CT and DT circuits such as inherent anti-aliasing and jitter immunity into a single modulator. Of course, there are challenges to be tackled, however, the opportunities lying ahead are too great to ignore.
- **Enhanced voltage mode circuit:**
  Efforts can be placed in V/I converter to improve the performance of the system to the optimum point where current mode systems currently are. A more linear, less power consuming and smaller block would replace the current V/I converter.

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