FABRICATION AND TESTING OF POLYMER THIN FILM TRANSISTORS FOR BASIC DIGITAL CIRCUITS

by

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B.S., Electronics and Communications Engineering, Yıldız Technical University, 2006

Submitted to the Institute for Graduate Studies in
Science and Engineering in partial fulfillment of
the requirements for the degree of
Master of Science

Graduate Program in Electrical and Electronics Engineering Department
Boğaziçi University

2009

ACKNOWLEDGEMENTS

I would like to express my gratitude to Şenol Mutlu for his constant support and valuable guidance throughout my thesis. His optimism and never ending energy played a key role in the progress and the final success of this work. I am also very grateful to Ali Osman Sevim of BUMEMS Laboratory for helping me in the fabrication and measurement tasks.

Additionally, I would like to extend my appreciation to my friends Yiğit Dağhan Gökdel, Baykal Sarıoğlu, Okan Zafer Batur, Feyyaz Melih Akçakaya and Evren Akdağ at Boğaziçi University BETA Laboratory for their support and the time we spent together having enjoyable conversations. İskender Haydaroğlu also deserves special thanks for his advices and having a great sense of humor which helped a lot.

Finally, without the support of my family, I probably never would have made it through the graduate study, so I must thank my parents, my two sisters and my cousin Güner Mutlu.

There are many others who have helped me indirectly for all these years. Thanks everyone!

This work has been fully supported by Scientific&Technological Research Council of Turkey (TUBITAK) under the project name INPOMIS-INtegrated Polymer MIcro Systems with project number 106E013. The financial support of TUBITAK in this project is gratefully acknowledged.

ABSTRACT

FABRICATION AND TESTING OF POLYMER THIN FILM TRANSISTORS FOR BASIC DIGITAL CIRCUITS

In this thesis we developed fabrication and characterization methods for polymer thin film transistors(PTFTs) and circuits. After analysis of the various aspects related to the PTFTs, we propose a new method to fabricate self-aligned transistors on a transparent flexible substrate. This method relies on the back-side exposure and allows self-aligned short-channel transistors to be fabricated in close proximity to not-self aligned ones. Self-aligned transistors with a length of 50 μm and width of 1000 μm have a saturation current of around 1 μA and a saturation voltage of around -38 volts at a V_{GS} of -40 volts.

Following the self-aligned fabrication method, we use a regular process flow to fabricate fully patterned bottom-gate bottom-contact transistors on glass substrate. PTFTs with interdigitated, corbino and standard layout are fabricated. Gate dielectric and organic semiconductor are SU-8 and poly(3-hexylthiophene)(P3HT), respectively. Two methods for the patterning of the polymeric active layer are proposed. MIMIC is used to obtain P3HT patterns with several micrometer thickness. Lift-off, however, is found to be suitable for the patterning of relatively thin(20 to 100 nm) P3HT films. Moreover, leakage current of about one twentieth of the channel current, resulting from the non-patterned active layer is eliminated successfully by P3HT patterning with both MIMIC and lift-off.

A simple method for fabricating discrete transistors with silver epoxy drain/source electrodes is proposed next. PTFTs fabricated with this method showed a saturation

mobility of 0.036 cm^2/Vs and I_{ON}/I_{OFF} ratio of about 8.

Finally, we examine a treatment route for de-doping of the P3HT film. Vacuum treatment is found to be an effective way for desorption of the doping species from P3HT, heat treatment after vacuum, however, did not result in the reduction of the film conductivity. Electrical conductivity of drop-casted P3HT film decreased from 2.2x10^{-5} Scm^{-1} to 0.5x10^{-6} Scm^{-1} after vacuum treatment. Influence of heat and light at different wavelengths on the conductivity of the film is investigated at the last part of the thesis. Conductivity increased exponentially to 8x10^{-5} Scm^{-1} from initial 0.5x10^{-6} Scm^{-1} when temperature swept from 30 °C to 140 °C. Light with different wavelengths has also a observable effect on film conductivity. Exposure to blue light caused 9 fold increase in conductivity. Elimination of the light induced effect took around 5 hr for each wavelength.

ÖZET

TEMEL SAYISAL DEVRELER İÇİN İNCE FİLM TRANSİSTÖRLERİN ÜRETİMİ VE TESTİ

Bu tezin konusunu polimer ince film transistör ve devreler için üretim ve karaterizasyon yöntemlerinin geliştirilmesi oluşturmaktadır. Polimer ince film transistörler ile ilgili temel konulara kısaca değinildikten sonra saydam ve esnek yüzeyler üzerinde kendinden hizalı transistörlerin üretimine olanak sağlayan yeni bir yöntem incelenmiştir. Arka yüzeyden pozlandırma esasına dayanan bu yöntem kısa kanallı kendinden hizalı transistörlerin hizasız transistörlerle aynı yüzey üzerinde üretilmelerine olanak sağlamaktadır. Bu yöntemle üretilen 50 μm kanal uzunluğuna, 1000 μm kanal genişliğine sahip kendinden hizalı transistörlerin savak akımı 1 μA, -40 V taki doyma gerilimi de -38 V olarak ölçülmüştür.

Kendinden hizalı üretim yöntemini takiben polimer ince film transistör üretiminde sıkça kullanılan ve kapı-altta kontak-altta mimariye sahip transistörlerin bütün katmanları şekillenecek şekilde cam yüzey üzerinde üretimini sağlayan standart bir yöntem denenmiştir. Bu üretimde kapı yalıtkanı olarak SU-8, yarıiletken polimer olarak da poly(3-hexylthiophene)(P3HT) kullanılmıştır. Bununla birlikte yarıiletken polimer katmanının şekillendirilmesi için iki farklı yöntem önerilmiştir. Bu yöntemlerden MIMIC, nispeten kalın (3-5 μm) P3HT filmleri için daha elverişli bulunurken, lift-off yönteminin ince P3HT filmlerinin şekillendirilmesinde başarılı olduğu görülmüştür. Yarıiletken katmanın bu yöntemlerle şekillendirilmesi neticesinde kanal akımının yirmide biri boyutlarına ulaşan sızıntı akımı başarılı bir şekilde yok edilmiştir. Bu iki polimer ince film transistör üretim yöntemine ek olarak görece daha basit ve ayrık transistörlerin elde edilmesine olanak veren üçüncü bir yöntem de kullanılmıştır.

Bu yolla üretilen transistörlerde taşıyıcı hareket kabiliyeti 0.036 cm^2/Vs ve I_{ON}/I_{OFF} akımı 8 olarak hesaplanmıştır.

Bu tezde en son olarak P3HT filmlerinin tedavisi üzerine çalışılmıştır. Bunun sonucunda P3HT filmlerinin vakumda bekletilmeleriyle polimerin içindeki katkılayıcı gazların etkin bir şekilde geri bırakıldığı, bunu takip eden ısıl tedavinin ise önemli bir etkisinin olmadığı gözlenmiştir. Vakum ile tedavi sonucunda polimer filmin elektriksel iletkenliği 2.2x10^{-5} Scm^{-1} seviyesinden 0.5x10^{-6} Scm^{-1} değerine düşmüştür. Sıcaklıkla birlikte, farklı dalga boylarındaki ışığın da filmin iletkenliğine etkisi olduğu görülmüştür. Mavi renkte ışık 9 kat iletkenlik artışına neden olurken, ışık etkisinin tamamen yok olması her dalga boyu için yaklaşık 5 saat sürmüştür.

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LIST OF SYMBOLS/ABBREVIATIONS

f_T	Transition frequency of a transistor
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
I_{DS}	Drain current
V_T	Threshold voltage
C_i	Insulator capacitance
ϵ_o	Permittivity of free space
ϵ	Relative permittivity
V_{GS}	Gate to source voltage
μ	Field-effect mobility
g_m	Transistor transconductance
OTFT	Organic Thin Film Transistor
PTFT	Polymer Thin Film Transistor
OLED	Organic Light Emitting Diode
LUMO	Lowest Unoccupied Molecular Orbital
HOMO	Highest Occupied Molecular Orbital
a-Si:H	Hydrogenated Amorphous Silicon
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
RFID	Radio frequency identification
PET	Polyethylene terephthalate
rr-P3HT	Regio-regular poly(3-hexylthiophene)
RPM	Rotation per minute)
Au	Gold
Cr	Chromium
Ag	Silver

1. INTRODUCTION

1.1. Motivation and Organic Electronics Overview

Plastic materials have been readily used where an electrical insulation was needed for quite a long time. Advances in material and device science during the last twenty year, however, recently started to present new kind of products which are likely to change this common convention. Dating back to the discovery of the conducting polymers, this new and broad field of research area is called "organic electronics" because the devices emerging from this area use semiconducting and sometimes conducting materials that are made of molecules containing carbon, mostly in combination with hydrogen and oxygen.

Over a few decades, crystalline silicon and CMOS technology have been dominating the integrated circuit market. However, there is a large market for lower-performing, yet extremely inexpensive circuits and large area electronics where silicon technologies are not economical. The development of low-cost circuits, even with degraded performance, would enable the use of electronics in systems and applications where they previously would be cost-prohibitive. For those applications, organic thin film transistors (OTFTs) are the technology of choice. Unlike silicon MOSFET, OTFTs are field-effect transistors which use a thin film of organic semiconductor material as the active layer and can be deposited inexpensively on a variety of substrates. Currently glass substrates are the most widely used materials. However, the low-cost and large-area fabrications are compatible with arbitrary substrates such as several metals, polymeric films, cloth and even paper sheets. However, the flexible substrates, unlike rigid, brittle, heavy, and bulky inorganic substrates, are mechanically rugged, thin, and lightweight, and they potentially promise many new applications.

Many expect that the use of organic semiconductors will result in a wide range of applications. Organic light-emitting diode(OLED) displays are already commercially available; it is expected that organic photovoltaics and polymer thin-film transistors(PTFTs) will also be used in some low-cost applications. Today, the largest market for PTFTs is flat panel displays and RFID tags.

Polymer thin film transistors are the subject of this thesis. In chapter 2, after a brief introduction to organic electronics we first describe some important PTFT issues such as commonly used device topologies, transistor operation in organic electronics, organic semiconductors, electrical characterization methods and basic digital circuits.

Development of fabrication skills for PTFTs using in-house equipment and gaining insight into the polymer transistor operation and process related performance variations constitute the main part of our work. In chapter 3, a self-aligned(SA) PTFT fabrication method on flexible and transparent substrates using back-side exposure is developed first. Following SA PTFT fabrication, a regular process is experienced to fabricate fully patterned polymer transistors and circuits based on inverted coplanar topology. Next we describe soft-lithographic and photo-lithographic patterning methods for active layers deposited from solution.

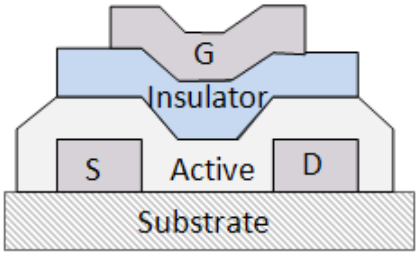
Finally in chapter 4, we investigate the effects of environmental factors like temperature and light exposure on the electrical conductivity of the active layer.

2. POLYMER THIN FILM TRANSISTORS(PTFTs) AND CIRCUITS

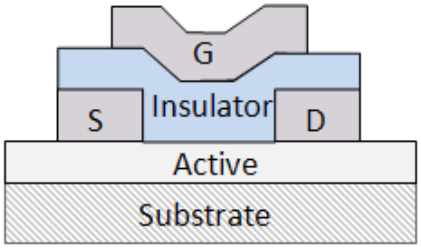
2.1. PTFT Topologies

The large number of the materials available in PTFT processing have allowed several device structures. Among them lateral device architecture, also commonly found in a-Si TFTs, is usually preferred over vertical devices due to simplicity and less number of steps involved in the fabrication. Lateral architecture can be divided into four different topologies, Figure 2.1 and Figure 2.2. These four topologies can be classified as being either "top-gate" or "bottom-gate(inverted)".

Cross sectional view of the two variations of the top-gate transistors is illustrated in Figure 2.1. In top-gate transistor fabrication, gate dielectric and the gate electrode deposition, respectively are the last steps in the process sequence. Top-gate topology also have two variations. Distinct feature of these two structures is the deposition orders of the drain/source electrode and the active layer. In top-contact topology, Figure 2.1a, drain/source electrodes are formed prior to the active layer deposition whereas in the bottom-contact topology, Figure 2.1b, the sequence of the electrode and the active layer deposition is vice versa. In literature other designations commonly used for top-contact and bottom-contact structures are staggered and coplanar, respectively. This naming conventions arise from the relative positions of the accumulated conductive channel and the drain/source electrodes upon application of a gate voltage. Channel and the electrodes are at the same plane in bottom-contact devices and hence they are also called "coplanar" where "staggered" term is used for top-contact transistors because the direct path between the accumulated channel and the electrode is interrupted by the bulk of the active layer.



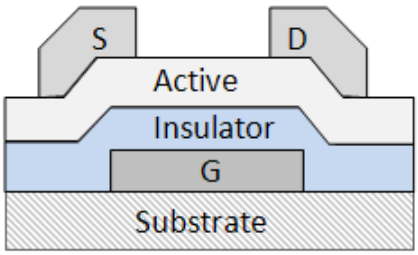
(a) Top-gate top-contact(staggered)



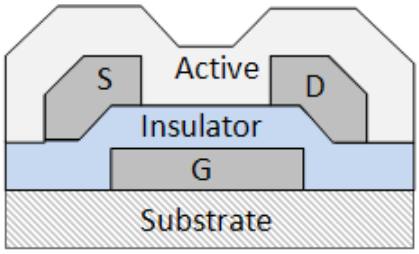
(b) Top-gate bottom-contact(coplanar)

Figure 2.1. Top-gate TFT topologies

Figure 2.2 shows the two variations of the bottom-gate or inverted transistors in which the first layers to be deposited and patterned for both are the gate electrode and the gate dielectric. Following the gate dielectric patterning either the active layer or the drain/source electrodes are formed on top of the insulator. In the former case, the topology is referred to as top-contact(staggered)(Figure 2.2a), if the active layer deposition is left as the last step then the topology is bottom-contact(coplanar) (Figure 2.2b).



(a) Bottom-gate top-contact(staggered)



(b) Bottom-gate bottom-contact(coplanar)

Figure 2.2. Bottom-gate(inverted) TFT topologies

The inverted architecture is considered to be more beneficial in term of transistor performance since the deposition and patterning of the active layer occurs later in the process sequence and in the case of bottom-contact TFTs, practically active layer formation is the last step. One of the most important parasitic element in polymer TFTs is contact resistance which leads to a potential drop at the contacts thus preventing

the full source-drain bias from being applied across the channel. Top-contact inverted devices are likely to have smaller parasitic drain/source contact resistance compared to the bottom-contact transistors because the effective area of the contact is larger in top-contact transistors [1]. The preferred method for drain/source electrode formation in top-contact transistors is vacuum evaporation through a shadow mask, however results in bulky devices with channel lengths around a few hundred microns which is not suitable for practical applications [2]. Moreover, it is quite a known fact that the quality of the deposited film tends to degrade if additional materials are deposited and processed on top of this sensitive layer [3]. Since in organic semiconductors the active layer film quality is directly related to carrier mobility that can be obtained from this film, fabrication methods resulting in higher mobilities are of primary interest. For this reason, bottom-gate bottom-contact topology has been the preferred architecture and has been the commonly encountered device structure for both a-Si and polymer TFTs because active layer deposition takes place at the last step of the fabrication.

2.2. Device Physics and Operation of PTFTs

In this thesis we focus on the fabrication and characterization of bottom-gate bottom-contact PTFTs which use conjugated polymers as active materials. Conjugated polymers are organic macromolecules which have an alternating single and double carbon-carbon bond structure. Carbon atom with six electrons has ground state configuration of $1s^2 2s^2 2p^2$ or more easily read:

$$C \quad \underset{1s}{\uparrow\downarrow} \quad \underset{2s}{\uparrow\downarrow} \quad \underline{\underset{2p_x}{\uparrow}} \quad \underline{\underset{2p_y}{\uparrow}} \quad \underline{\underset{2p_z}{}} \tag{2.1}$$

Carbon can also bond with other atoms via hybridization of the outer four $2s$ and $2p$ orbital electrons. In conjugated materials sp^2 hybridization between neighboring atoms is formed. In sp^2 hybridization the $2s$ orbital is mixed with only two of the three available $2p$ orbitals:

$$C^* \quad \underset{1s}{\uparrow\downarrow} \quad \underline{\underset{sp^2}{\uparrow}} \quad \underline{\underset{sp^2}{\uparrow}} \quad \underline{\underset{sp^2}{\uparrow}} \quad \underline{\underset{p}{\uparrow}} \tag{2.2}$$

In this configuration three sp^2 orbitals are combined in planar formation with a highly localized electron density in the plane of the molecule. This strong covalent bond is called a sigma (σ) bond, which forms the single bonds between carbon atoms and hence the backbone of the chain. Electrons in this orbital are highly localized between the atoms. The energy difference between the low energy (σ) state and the excited (σ^*) state is quite large. Thus the electronic properties associated with this bond are that of an insulating material [4]. Double bonds contain a σ-bond and a π-bond, where the π-bond is the overlap between p_z orbitals of neighboring atoms along the conjugation path (Figure 2.3). Electrons in π-bonds are less localized and more mobile. The conjugation of single and double bonds establishes a delocalization

of the electrons situated above and below the plane of the molecule. π-bonds are either empty (called the Lowest Unoccupied Molecular Orbital - LUMO) or filled with electrons (called the Highest Occupied Molecular Orbital - HOMO). The band gap of these materials determined from optical measurements is within the semiconductor range of 1 to 4 eV, which covers the whole range from infrared to ultraviolet region. A well-known example of a conjugated polymer is polyacetylene, which consists only of a single chain of alternating single and double bonds (Figure 2.4).

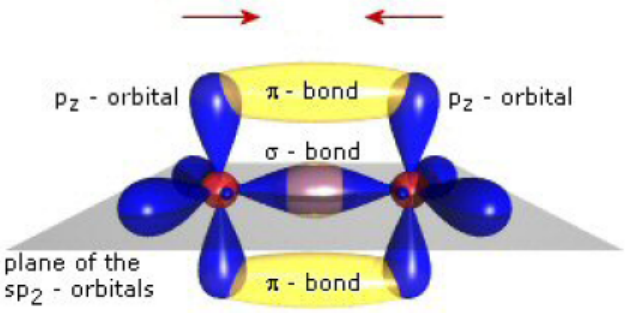


Figure 2.3. Bond structure between two carbon atoms(sp^2 hybridization).

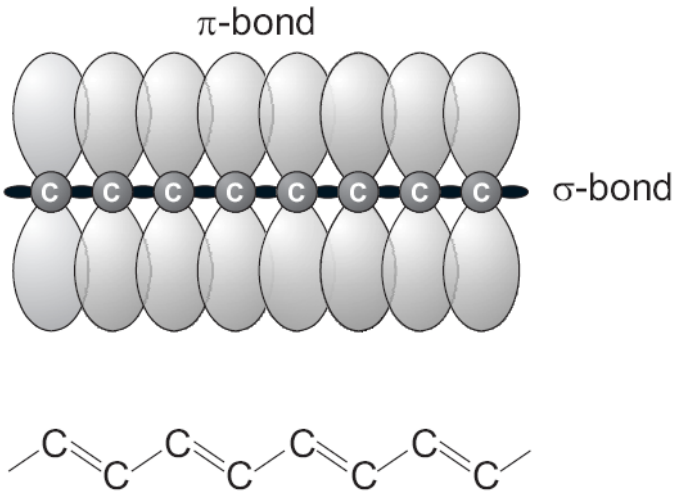


Figure 2.4. Representation of the sigma(σ) and pi(π) bonds between carbon atoms (above) in polyacetylene (below).

Since the discovery of organic semiconductors, extensive research has been carried out to understand and develop polymer thin film transistors and circuits. Polymer TFT is a three terminal device capable of switching and amplifying a current. The main processes that govern the operation of the polymer TFT are: charge accumulation, charge injection and charge transport. PTFTs are primarily operated as accumulation mode enhancement transistors as opposed to the usual inversion mode operation of silicon MOSFETs. When operating, a voltage is applied to the gate and the drain while the source is grounded (Figure 2.5). The potential difference between the gate and the source is called the gate voltage(V_{GS}), the potential difference between the drain and the source is called the drain-source voltage(V_{DS}). When a potential is applied at the gate, opposite charges accumulate in the insulator/semiconductor layer, thus opening a low resistance channel for conduction of carriers injected from source electrode. The current can flow both in the accumulation layer and in the bulk of the semiconductor due to the mobile charge induced by unintentional doping [5]. Since not all charges are mobile i.e. there are usually traps present and because there can be charges already present in the insulator, a certain voltage has to be applied before a current is measured, this can be both positive and negative. This voltage is called the threshold voltage(V_T) and in PTFTs the underlying physical reason for observed Vt is different from the silicon MOSFETs. The effective gate voltage(overdrive voltage) is therefore $V_{GS} - V_T$.

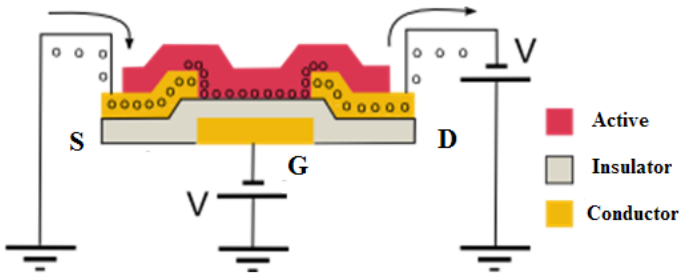


Figure 2.5. Representation of charge transport in a PTFT employing a p-type organic semiconductor.

Ideally the source and drain contacts should behave as ohmic contacts for the majority carrier type in the organic semiconductor. Single crystal MOSFETs, polycrystalline Si TFTs, and a-Si TFTs all make use of doped regions to form ohmic contacts and restrict the charge injection and transport to a single carrier type. The strategy of enhancing the current injection by means of heavy local doping of the semiconductor interfacial regions to provide a tunneling contact, which is usually adopted with inorganic semiconductors, is not viable in organic transistors [6]. Therefore one has to rely on proper alignment of metal Fermi level with highest(lowest) occupied(unoccupied) molecular level in order to achieve an ohmic contact for holes(electrons).

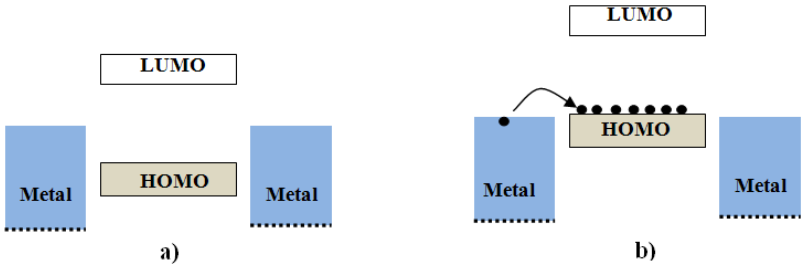


Figure 2.6. Representation of a working principle of a p-type PTFT a)no charges are accumulated when $V_{GS} = 0V$ b)when a negative voltage applied to the gate.

To demonstrate the operating principle of the PTFTs, a simplified energy level diagram for Fermi level of source-drain metal electrode and HOMO-LUMO levels of a semiconductor are shown in Figure 2.6. If there is no gate voltage applied (Figure 2.6a), the organic semiconductor, which is intrinsically un-doped, will not show any charge carriers. Direct injection from the source/drain electrodes is the only way to create flowing current in the organic semiconductor. Such currents will be relatively small owing to the high resistance of the organic semiconductors and large distance between the source and drain electrodes. When a negative gate voltage is applied (Figure 2.6b), positive charges are induced at the organic semiconductors adjacent to the gate dielectric (a conducting channel is formed). If the Fermi level of the source/drain metal is close to the HOMO level of the organic semiconductor, then positive charges can be extracted by the electrodes by applying a voltage, V_{DS}, between the drain and source.

2.3. Organic Semiconductors for Organic TFTs

The notions of n-type and p-type do not have the same meaning as for inorganic semiconductors. An organic n-type semiconductor is one in which electrons are more easily injected than the holes. Whereas in p-type materials holes are the mobile carriers that can be injected from the electrodes efficiently rather than electrons. Therefore, n-type and p-type designation is more related to the HOMO and LUMO levels in organic semiconductors.

2.3.1. n-type Organic Semiconductors

Whereas p-type FET materials are abundant, n-type FET materials are much rarer (Figure 2.7). Recently, however, more n-type materials are becoming available. The most successful class of compounds exhibiting high n-type mobility in TFTs is that of the fullerenes C60, C70, and their derivatives [19][20][21][22]. Mobilities close to 1 cm^2/Vs have been obtained. Other n-type materials are usually fluorinated p-type materials, like perfluorinated pentacene Figure 2.7a [23], and thiophenes with fluorinated side chains Figure 2.7(b, c) [24][25]. Good n-type conduction is furthermore obtained with TCNQ, Fig. 2.7d [26]. Currently the biggest challenge for n-type materials is air-stability.

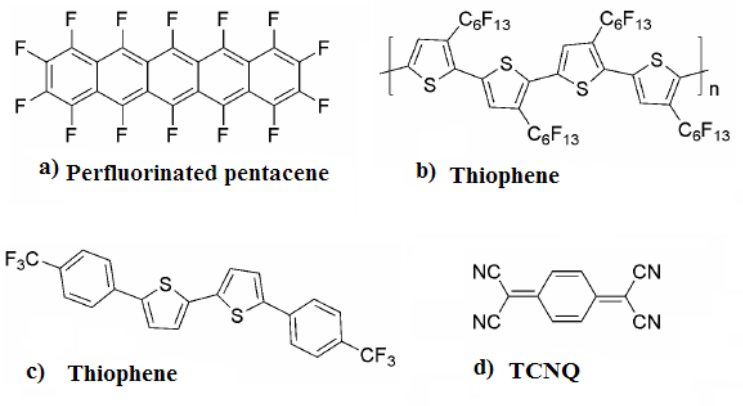


Figure 2.7. Molecular structures of n-type organic semiconductors.

2.3.2. p-type Organic Semiconductors

Charge carrier mobility is one of the most important PTFT parameters, since it determines the operation speed of the transistor. To date the highest mobilities for thin layer organic p-type TFTs are obtained with vacuum sublimed pentacene ($> 1 cm^2/Vs$) [7]. Pentacene Figure 2.8a is however, not solution processable, which would be more practical than vacuum sublimation. In recent years many efforts have been made to synthesize soluble pentacene derivatives, but they generally show much lower mobilities [8][9]. Functionalized anthradithiophenes Figure 2.8e, however, do show mobilities close to 1 cm^2/Vs [10][11]. Solution processable polymers offer a wide range of interesting materials for TFT application. The polymer with the highest mobility is regio-regular poly(3-hexyl)thiophene (RR-P3HT) Figure 2.8b, showing values of up to 0.1 cm^2/Vs, depending on the processing conditions [10][12][13]. The highest mobilities however, are obtained from single crystal TFTs [14]. The best examples of high mobility single crystals are vacuum sublimed pentacene [15], tetracene [16] Figure 2.8d and rubrene Figure 2.8c [17]. Mobilities of up to 20 cm^2/Vs have been obtained with single crystal rubrene TFTs [18].

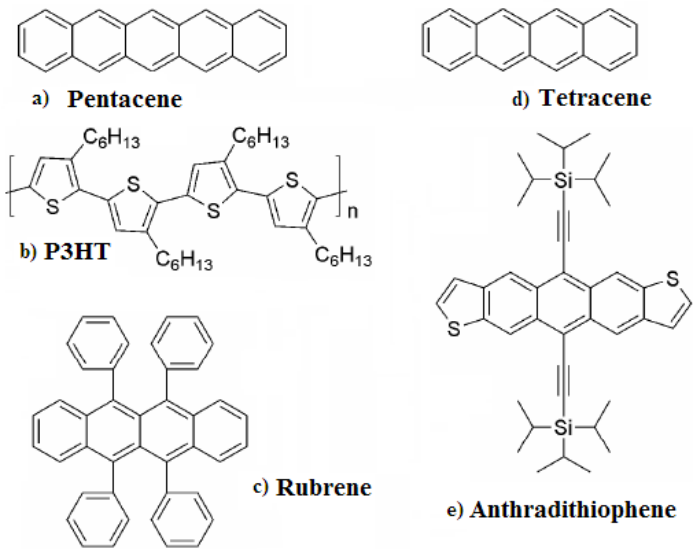


Figure 2.8. Molecular structures of p-type organic semiconductors.

2.4. Measurement and Electrical Characterization

Device operation and the drain current of PTFTs are described using terminology and expressions developed for crystalline silicon MOSFETs. While this is done usually for convenience, there are several important features that make PTFTs distinct from MOSFETs. Fundamentally, PTFTs differ from MOSFETs in their device physics and operation. MOSFETs are inversion and depletion mode devices while PTFTs operate as accumulation and depletion mode devices. The device structure and the electronic properties of organic active layer, intrinsically or due to degradation during processing, results in a non-ideal device behavior. This fact limits the accuracy of the extracted transistor parameters. Several analytical models have been proposed to describe the

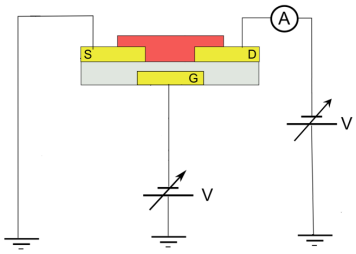


Figure 2.9. Measurement arrangement for DC characterization.

current-voltage relationship of PTFTs, many of them tries to account for the nonlinear effects that cause the deviation from the ideal MOSFET expression. However in practice PTFT parameters are frequently extracted using the standard equation developed by W. Schockley, eq. 2.3 for linear behavior when $|V_{DS}| < |V_{GS} - V_T|$ and eq. 2.4 for saturated behavior in the region $|V_{DS}| \geq |V_{GS} - V_T|$.

$$I_{DS}^{lin} = -\frac{W}{L}\mu C_i(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \tag{2.3}$$

$$I_{DS}^{sat} = -\frac{1}{2}\frac{W}{L}\mu C_i(V_{GS} - V_T)^2 \tag{2.4}$$

Here W stands for the transistor channel width, L for transistor channel length, μ for field effect mobility and C_i for gate insulator dielectric capacitance per unit area. C_i is given by:

$$C_i = \frac{\epsilon\ \epsilon_o}{t_i} \tag{2.5}$$

where ϵ_o is the permittivity of the free space, ϵ is the relative permittivity of the gate insulator and t_i is the thickness of the gate insulator.

DC measurements are a convenient method for characterization of PTFTs. Measurement setup illustrated in Figure 2.9 is used for DC voltage sweep and drain current measurement. When evaluating the electrical characteristics of PTFTs, often reported parameters are the field-effect mobility, on/off current ratio, subthreshold slope and threshold voltage. These parameters can be extracted from the measured output characteristics and the transfer characteristics of PTFTs. Field-effect mobility in the linear region is generally extracted from the transconductance, g_m, of the device. g_m is defined as the change of I_{DS} with V_{GS} for a small and constant V_{DS}:

$$g_m = \left(\frac{\partial I_{DS}}{\partial V_{GS}}\right)_{V_{DS}=small,const.} = \frac{W\mu C_i}{L}(V_{DS}) \tag{2.6}$$

Rearranging the equation 2.6 gives the field-effect mobility in linear region:

$$\mu = \frac{g_m L}{W C_i}\left(\frac{1}{V_{DS}}\right)_{V_{DS}=small,const.} \tag{2.7}$$

Threshold voltage, V_t, can also be extracted from the plot of the I_{DS} vs. V_{GS} characteristics for the device biased in the linear region by extrapolating the fitting line used for the mobility extraction to zero drain current and locating the intercept.

The field-effect mobility in the saturation region of the transistor can be extracted from transfer characteristics. Rearranging equation 2.4 and solving for μ gives:

$$\mu = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2 \tag{2.8}$$

The on/off current ratio($I_{on/off}$) is given as the ratio of the on current to the leakage current. Alternatively leakage current can be defined as the current at zero gate voltage:

$$I_{on/off} = \frac{I_{DSAT}(V_{DS}, V_{GS})}{I_{DSAT}(V_{DS}, V_{GS} = 0)} \tag{2.9}$$

The subthreshold slope, S, describes the turn on characteristics of the device and is defined as the change in V_{GS} required for one decade change in I_{DS} below the threshold voltage and given by:

$$S = \frac{\partial V_{GS}}{\partial(\log I_{DS})} \tag{2.10}$$

Current varies exponentially with V_{GS} in the subthreshold region whereas quadratical and linear variation can be observed in saturation and linear region, respectively. For silicon MOSFETs subthreshold slope of 60mV/decade is common whereas in PTFTs subthreshold slope varies with processing conditions and usually lies between $1 - 5$V/decade.

Figure 2.10 and 2.11 are the simulated characteristics of a PTFT employing P3HT active layer. Simulation model is based on the standard HSPICE MOSFET model equations where the voltage voltage dependency of charge carrier mobility and

bulk conductivity of the semiconducting polymer are modeled by additional voltage controlled current sources [27]. By fitting a line to the I_{DS} vs. V_{GS} characteristics and extracting the slope we can calculate field-effect mobility in linear region from the equation 2.7 provided that the device parameters W, L and C_i are known. An average mobility of 10^{-3} cm^2/Vs is calculated from the transfer characteristics in linear region (Figure 2.11).

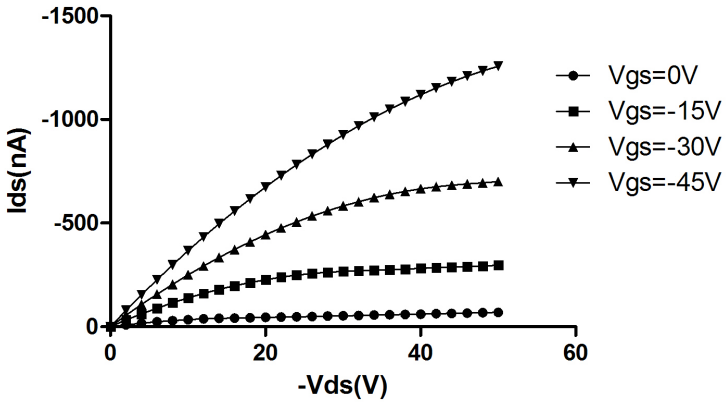


Figure 2.10. Simulated output characteristics($C_i = 11$ nF/cm^2, $W = 2$ mm, $L = 30$ μm).

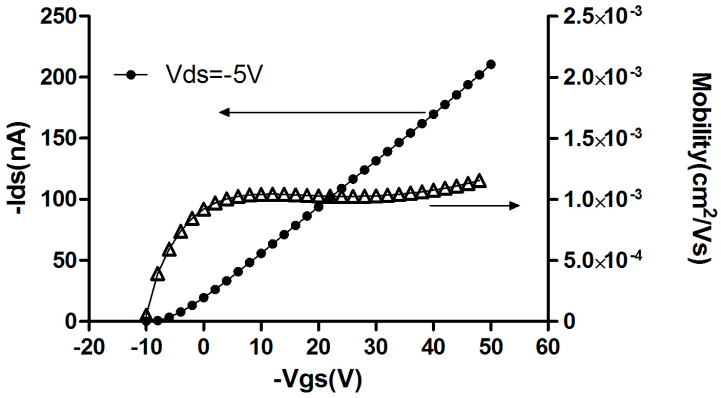


Figure 2.11. Simulated transfer characteristic in linear region and extracted mobility variation ($C_i = 11$ nF/cm^2, $W = 2$ mm, $L = 30$ μm).

2.5. Fundamental Digital Circuits

Demonstration of the first organic semiconductor based transistors lead to the development of the organic circuits. The first of these circuits were inverters, ring oscillators and logic gates. In addition to these basic circuits decoders, shift registers, frequency dividers, analog differential amplifiers and AMOLED driver circuits were realized with variety of organic semiconductors on several substrates. Majority of these circuits are based on p-type transistor. The reason behind this is the better stability of the most of the p-type organic semiconductors compared to n-type organic semiconductors. Although intense research effort is going on to improve n-type semiconductors, the highest stability n-type materials still fall behind many p-type semiconductors today.

P-type only circuits have an advantage that it only needs one kind of semiconductor so that processing and stability concerns are minimized. However, it has the disadvantages of having higher static power consumption and lower switching speed. In p-type only circuits, ratio of the transistors are the main design parameter. Wider load devices mean higher capacitances that need to be charged-up and down during the voltage level transitions which severely limits the circuit speed.

The fundamental building block for any digital circuit is perhaps the inverter and the NAND gate. Using only NAND gates any logic operation and therefore the circuit can be realized. In p-type only organic circuit design usually two kinds of inverter topologies are of primary importance, Figure 2.12 shows these two topologies.

The circuit in Figure 2.12a is called diode load inverter, to ensure proper functionality for this inverter, the driver transistor is made r times wider than the load transistor. The diode-load inverter is much faster than the zero-Vgs load inverter because the pull-down device (load transistor) is always on. However the gain is much smaller in diode-load topology causing lower noise margin compared to zero-Vgs inverter [31].

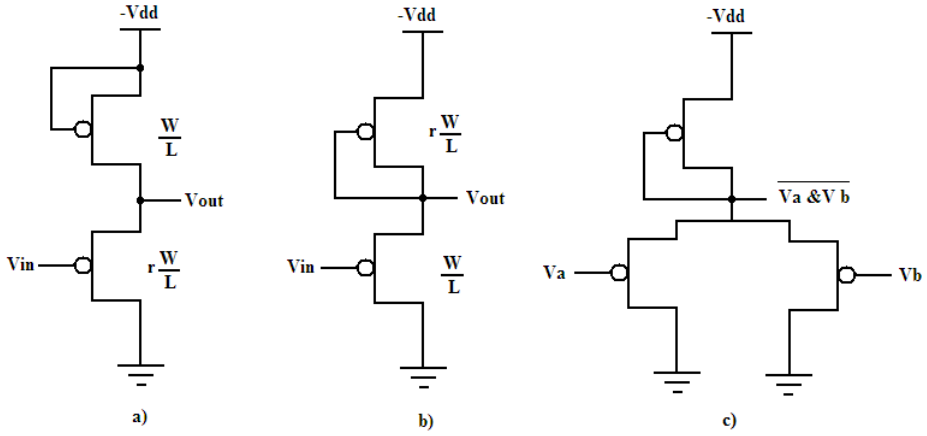


Figure 2.12. Inverters and NAND gate usually employed in digital PTFT circuits a)diode load inverter b)zero-Vgs load inverter c)two-input NAND gate.

Figure 2.12b shows zero-Vgs load inverter. In zero-Vgs topology load transistor is connected to have V_{gs}=0V and is designed to be r times wider than the driver transistor to ensure a higher noise margin. For all input voltages both transistors are on and the output voltage is determined from voltage division. Figure 2.13 is the simulated transfer characteristic for this type of inverter. Here the load transistor is 8 times wider than the driver transistor.

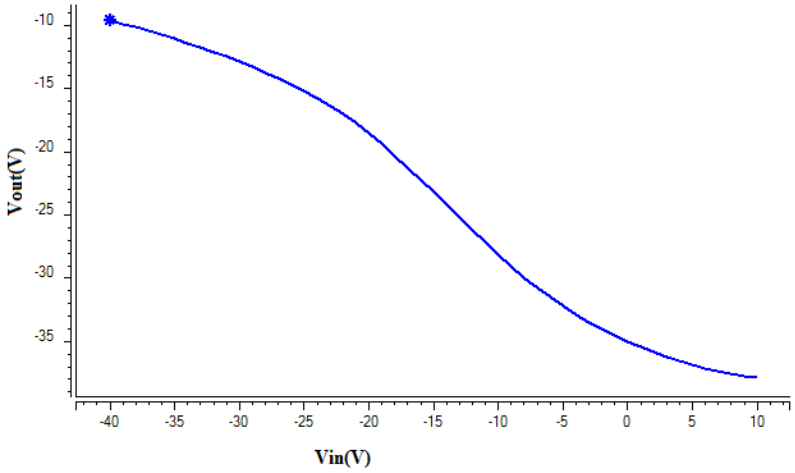


Figure 2.13. Transfer characteristic of zero-Vgs load inverter.

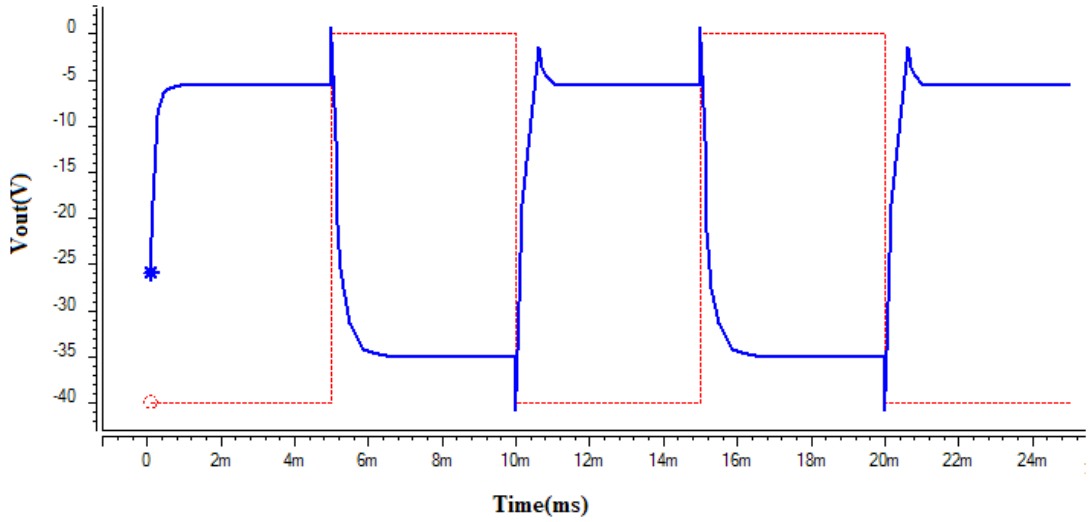


Figure 2.14. Transient output voltage waveform of a zero-Vgs load inverter with square-wave input voltage.

Figure 2.14 shows the voltage waveform at he output of the zero-Vgs load inverter driven by 100 Hz square-wave input voltage. Observed glitches at the pulse transitions arise from the parasitic gate-to-source and gate-to-drain overlap capacitances, since the transistor dimensions are on the order of millimeters. These parasitic capacitances severely limit the dynamic performance of the inverter.

2.6. Concluding Remarks

This chapter introduced the fundamental issues related to the polymer thin film transistors. First, different PTFT topologies are explained along with the fabrication aspects of related to these architectures. Following a short discussion on conjugated polymers and polymer transistor operation, n-type and p-type organic semiconductors of significant importance are briefly mentioned. Explanation of electrical characterization and parameter extraction methods for commonly referred PTFT performance metrics is carried on next. Brief analysis of basic building blocks for digital polymeric circuits concluded the chapter.

3. FABRICATION OF P3HT THIN FILM TRANSISTORS

3.1. Fabrication and Measurement Equipment

Thin metal film deposition process throughout this thesis work is realized with the thermal evaporator manufactured by Nanovak, Figure 3.1. With this system vacuum level can be pumped down to 4x10^{-6} Torr and two different kinds of materials can be evaporated without ceasing the vacuum.

Figure 3.1. High vacuum thermal evaporator system.

Photolithography is an essential part of every microelectronic fabrication facility and the most important element in photolithography is perhaps the light source. We have designed a custom-made UV exposure system housing a Phillips HPA 2000 UV lamp which served as the light source in our exposure steps (Figure 3.2). The peak wavelength of the custom made exposure system is 380 nm and output intensity is 0.5 mW/cm^2 [28]. In an exposure system used for microelectronic fabrication, UV light beam should be perfectly collimated for both high aspect ratio and high resolution patterns. However, in polymer transistor and circuit fabrication, materials are usually deposited in the form of thin films and also the resolution do not need to be

in nanometer levels because the contact resistances start to be the dominant factor limiting the drain current of an organic transistor below a certain channel length [30]. With this custom-made exposure system patterns with dimensions above 20 μm can be transferred using wide variety of photoresists and substrates successfully.

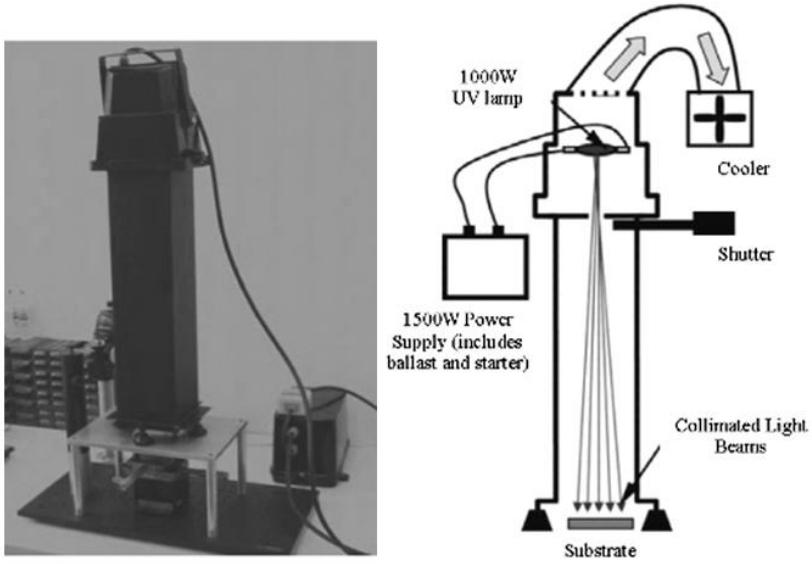


Figure 3.2. Custom made UV exposure system.

Exposure of the photoresist can be realized in three different modes: contact, proximity, and projection [29]. In contact printing, very high resolutions can be achieved due to the physical contact with the mask, although defects on both resist layer and mask can be formed in this mode. The proximity exposure technique is similar to contact printing but there is 10 to 25 micrometer space between the wafer and the mask after alignment. This gap reduces mask damage. Projection printing eliminates the damage of mask by the large gap between mask and wafer. The mask image is projected towards the wafer but to achieve high resolution only a small segment of the mask is imaged. In our polymer based microfabrication process, to obtain sufficient resolution and to realize the exposure stage with minimum cost, contact-printing method is selected.

To observe the mask and the wafer concurrently for mask alignment a homemade platform including a stereo-microscope and a wafer holding stage mounted on micro-manipulators is designed (Figure 3.3). Using this custom-made aligner and exposure system, maximum lithography resolution of 20 μm and minimum alignment error of about $5 - 10$ μm could be achieved.

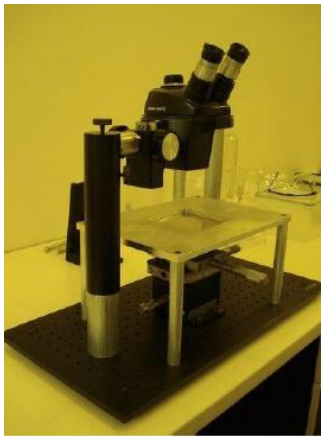
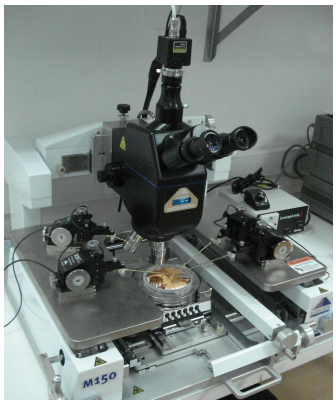
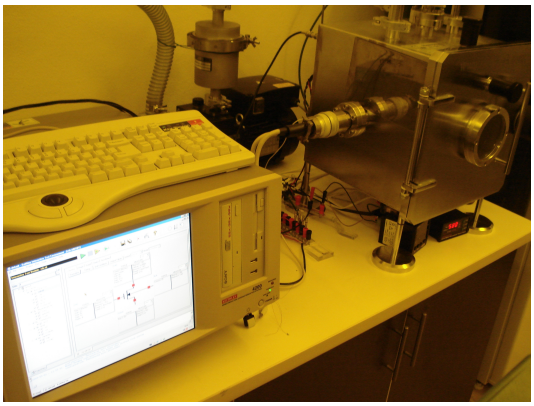


Figure 3.3. Custom made optical alignment setup.

All the measurements are made using the Cascade Microtech M150 probe station (Figure 3.4a) and Keithley SCS 4200 semiconductor parameter analyzer (Figure 3.4b).



(a) Probe Station(Cascade Microtech M150)



(b) Vacuum chamber and Keithley SCS 4200 semiconductor parameter analyzer

Figure 3.4. Measurement equipments.

3.2. Self-Aligned PTFTs

One of the most favorable advantages of flexible electronics is attributed to roll-to-roll batch processing of continuous substrates, in which meters of flexible circuits can be fabricated in a minute [32]. In fully automated systems with such a high throughput, layer-to-layer registration is extremely difficult because high-speed fabrication needs to be compromised for layer alignment, which is not acceptable from the point of today's commercial needs. Layer-to-layer mismatch is the major source of device parasitics for PTFTs and implies serious performance limitations for specific applications. Overlap capacitance is one of these parasitics and inversely related to the transition frequency (f_T)(eq. 3.1) of a transistor [33]. Figure 3.5 illustrates the capacitances of a thin film transitor. Here the parasitic capacitances denoted by C_F are formed by gate overlap.

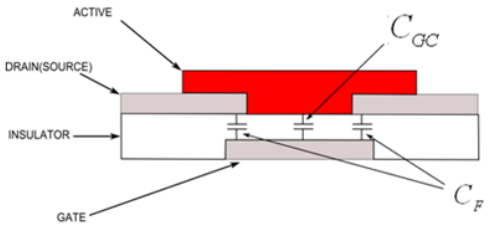


Figure 3.5. Cross-section of a TFT together with parasitic capacitors.

$$f_T = \frac{g_m}{2\pi C_T} \tag{3.1}$$

Considering a digital PTFT circuit running at %30-40 of its transition frequency, overlap capacitance severely limits the clock speed, thus restricting the use of polymer transistors in many applications such as 13.56 MHz RFID tags [34]. These limitations can be eliminated if polymer transistors with self-aligned gates can be fabricated. Developing a fabrication process with a self-aligned gate is very important since inevitable alignment errors in a fabrication do not result in any significant overlap.

Research efforts for the development of self-aligned PTFTs have been limited to the usage of inkjet-printing, surface tension effects and embossing [35][36]. However, these methods have some limitations. Inkjet printing requires additional equipments that are not common in thin-film processing. Furthermore, the smallest achievable feature size in inkjet printing changes from 20 to 200 μm depending on the smallest volume of droplets that can be jetted [37].

3.2.1. Self-Aligned PFET Fabrication Method Using Backside Exposure

In this thesis, backside exposure is used to fabricate bottom gate bottom contact PTFTs with the drain/source self-aligned to the gate. This method has been successfully applied to a-Si thin-film transistors on glass [38] and on flexible substrate [39] previously. We fabricated self-aligned PTFTs employing regioregular poly(3-hexylthiophene)(rr-P3HT) active layer using this method. With the second frontside exposure used in the process, both self-aligned and regular (not self-aligned) transistors with large overlaps are fabricated on the same wafer together for the first time in this work. Since the second exposure is mandatory for the interconnections of transistors to form a functional circuit, it does not add an additional step to the process. Figure 3.6 shows the layout of the test structures fabricated by the self-aligned process. Test structures include Kelvin bridges, metal-insulator-metal(MIM) capacitors, transistors having various drain/source geometry with different aspect ratios, inverters of both zero-Vgs load and diode load topology and ring-oscillators consisting of back-to-back connected inverters.

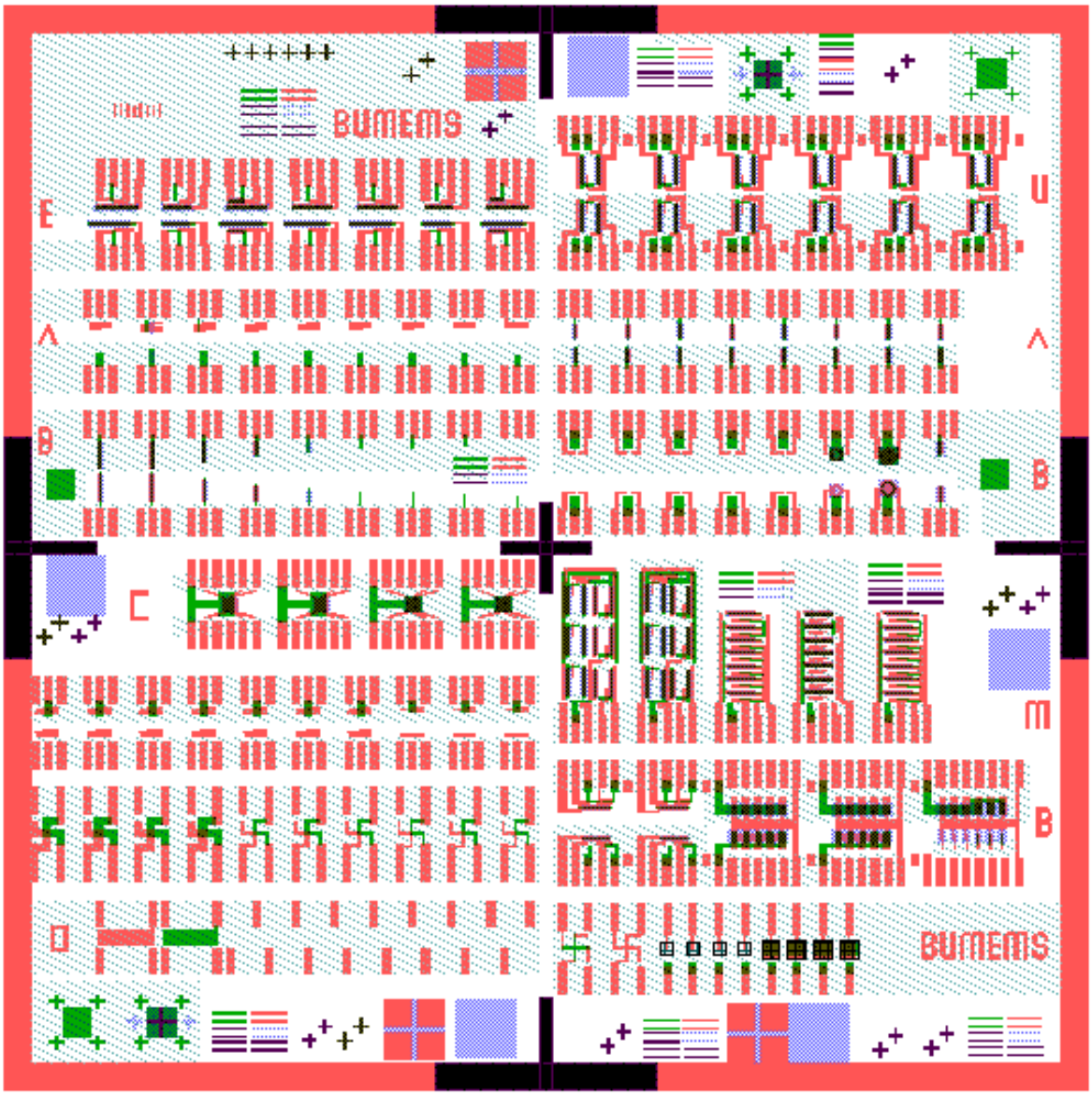


Figure 3.6. Layout of the test structures fabricated with self-aligned process.

Self-aligned process followed to fabricate polymer thin-film transistor is shown in Figure 3.7. 125 μm thick polyethylene terephthalate (PET) film is used as substrate. 80x80 mm^2 PET film is temporarily laminated on a 2 mm thick glass carrier and substrate is cleaned using standard acetone, 2-propanol, DI water rinsing procedure for 10 minutes in each step. In order to limit the dimensional distortions during the fabrication steps, substrate is heated up to 150 °C for 30 min before any other material is deposited. Chromium and gold is thermally evaporated under the vacuum better than

10^{-5} Torr to form 10 nm and 60 nm films respectively and lithographically patterned to form gate electrode. In order to leave photoresist only on the gate electrode, therefore to achieve self-aligned gates, substrate and the gate dielectric should be transparent to UV light. For this reason, SU-8 2000.5 permanent negative epoxy photoresist which has optical transmittance greater than %90 in the 375-400 nm wavelength range is chosen as gate dielectric [40]. SU-8 is spin-coated at 4000 RPM, which gives thickness of about 400 nm and subsequently patterned to form via openings. After this step, positive photoresist (Shipley 1828) is spin-coated and soft baked on top of the SU-8 layer. In this fabrication, self-alignment of drain/source electrodes to the gate electrode is obtained by a backside flood exposure without a mask. Gate electrode itself serves as a mask for the positive photoresist in this step.

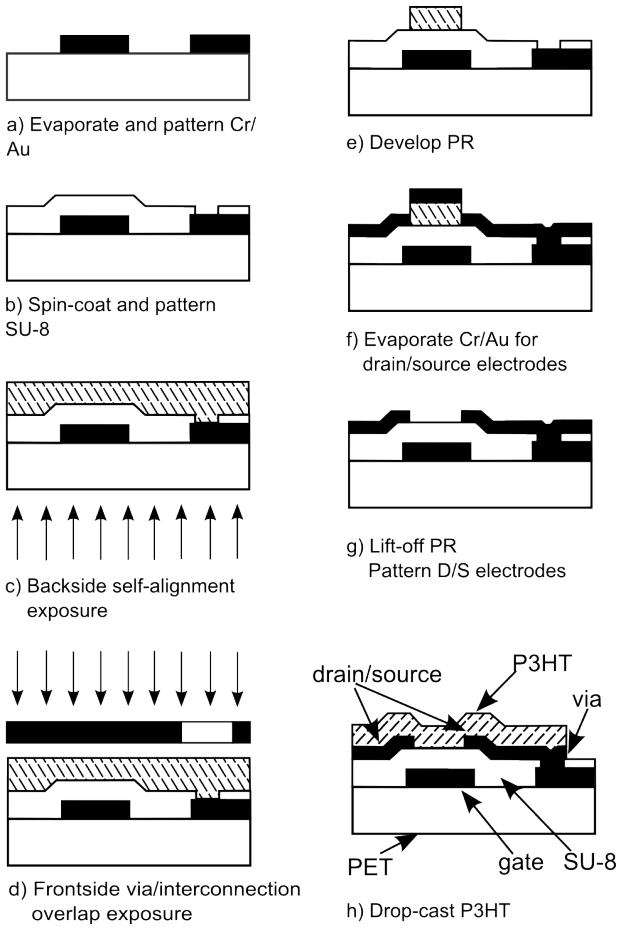


Figure 3.7. Process flow of a self-aligned PTFT

To guarantee the continuity of the channel a small overlap is desirable and this is achieved by the overexposure of the photoresist. In our case, 6 minute exposure time gave an overlap profile of 1.8 μm as measured and shown in Figure 3.8.

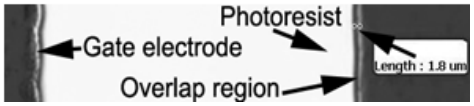


Figure 3.8. Picture showing the intentional overlap profile

Backside exposure without a mask must be followed by a frontside exposure with a mask in order to prevent the second metal layer over the via from lifting-off. Otherwise, interconnections between gate metal and source/drain metal layers cannot be formed. The frontside exposure does not affect the self-alignment of the gate since this exposure happens outside the critical gate region. In the second metallization step 5 nm Cr and 40 nm Au is evaporated under the same vacuum level used for gate metal evaporation. Then, the photoresist and hence the metals on top of it is lifted-off in acetone. Following the lift-off, drain/source electrode patterning is finalized by a positive lithography step. Since drain/source edges on the gate region are determined by the preceding lift-off, mask alignment is not critical in this step and does not affect the self-alignment of the gate. This step is also used to fabricate regular (not self-aligned) transistors in close proximity to the self-aligned ones on the same wafer.

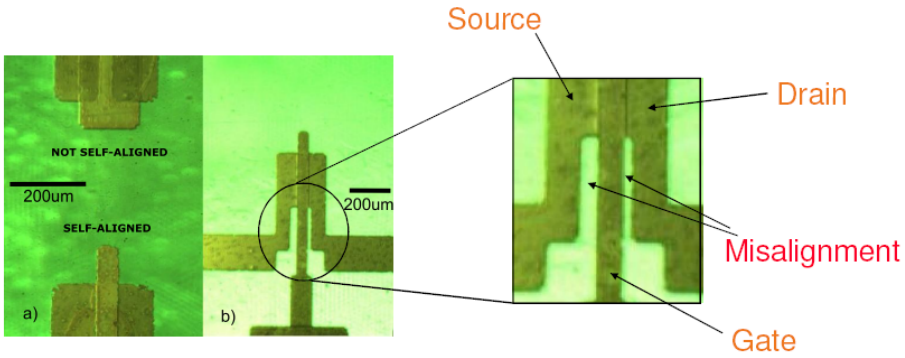


Figure 3.9. a) Picture of self-aligned and not self-aligned PTFTs b) Picture of a self-aligned PTFT alone.

Pictures of fabricated devices with patterned gate, gate dielectric and source/drain electrodes are shown in Figure 3.9. Regular (not self-aligned) transistors in close proximity to the self-aligned ones on the same wafer are shown in Figure 3.9(a). This picture shows the success of the self-alignment process clearly. Details of the self-alignment process can better be understood with the drawings in Figure 3.10. These drawings explain how interconnections over via regions that are needed to build digital circuits are made and how both self aligned and not self-aligned transistors are fabricated together after backside exposure.

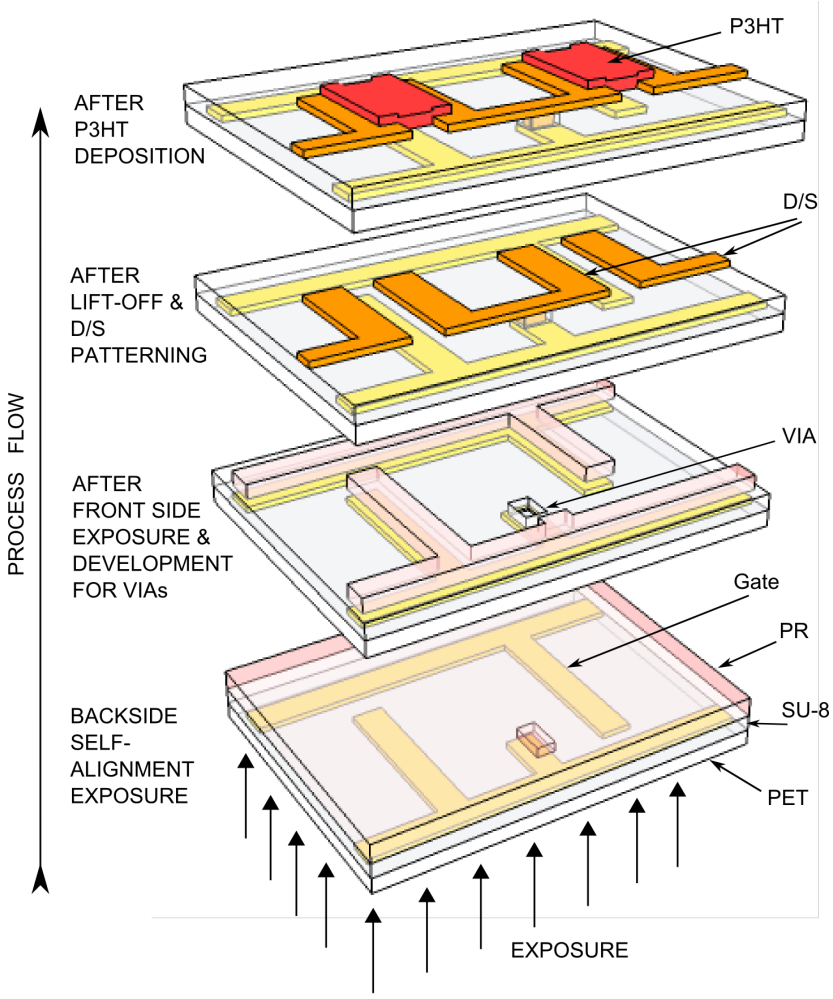


Figure 3.10. Process flow of a self-aligned PTFT

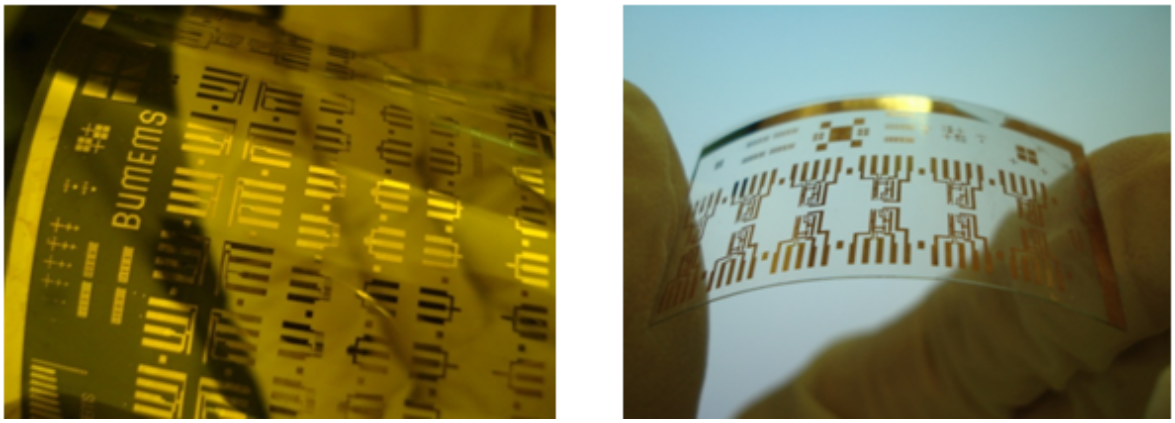


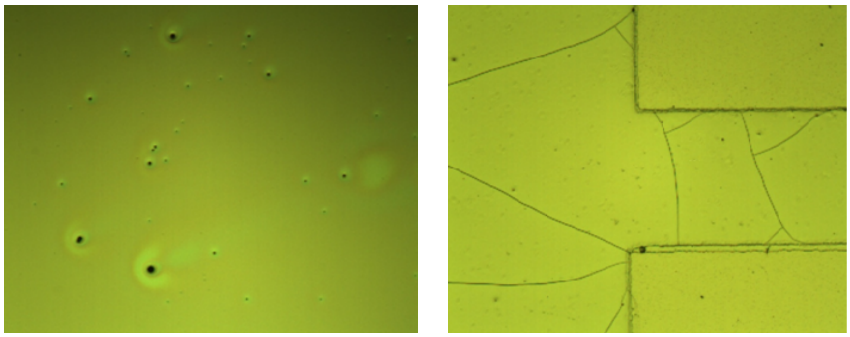
Figure 3.11. a) Picture of self-aligned and not self-aligned PTFTs on flexible substrate. b) PTFT circuits on flexible substrate.

Fabricated PTFT arrays of both self-aligned and not self-aligned transistors on flexible substrate are shown in Figure 3.11.

Following the formation of gate electrodes, gate dielectric layer with vias and source/drain electrodes with the necessary interconnections to implement a polymer circuit, regioregular poly(3-hexylthiophene) (rr-P3HT from Sigma-Aldrich) solution is deposited by drop-casting and annealed for one hour at 110°C to evaporate solvent. The polymer is dissolved in 1,2,4-Trichlorobenzene to give a weight concentration of 2.5 mg/ml and filtered through a 0.2 μm pore sized PTFE membrane syringe filter. Finally, the devices are wired to the printed circuit boards (PCBs), which had patterned copper lines for testing, using silver epoxy.

3.2.2. Measurement Results and Comments

Transistors are measured and characterized under dark in ambient air with Keithley SCS-4200 semiconductor parameter analyzer. During fabrication several cracks are observed on the SU-8 dielectric film after via opening definition. These cracks resulted in the partial failure of the dielectric film. This kind of defects are frequently encountered is SU-8 films [41][42][43]. Since the dielectric covers the whole 80x80 mm^2 surface except for the via regions, we attributed these defects to the stress on the film developed during SU-8 baking and patterning (Figure 3.12).



(a) Point defects (b) Cracks

Figure 3.12. SU-8 defects.

Possible remedies to reduce stress could be to remove SU-8 in the blank areas of the substrate thus leaving room for the process induced dimensional changes, and to eliminate sharp edges in the layout, which distribute the total stress homogeneously over the whole via border rather than allowing it to accumulate at the sharp edges, Figure 3.13.

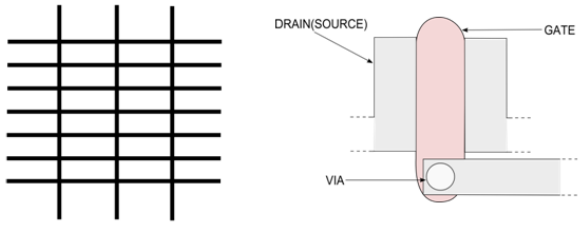


Figure 3.13. Possible remedies for SU-8 cracks.

Cracks are likely to cause electrical shorts between gate and drain/source or semiconducting polymer layer, resulting in a dysfunctional device. Regular (not self-aligned) transistors with gate to drain/source overlap areas suffered from these defects. They did not show any transistor characteristics at all. Nevertheless, self-aligned PTFTs showed deteriorated but still working transistor output characteristics as can be seen in Figure 3.14(a).

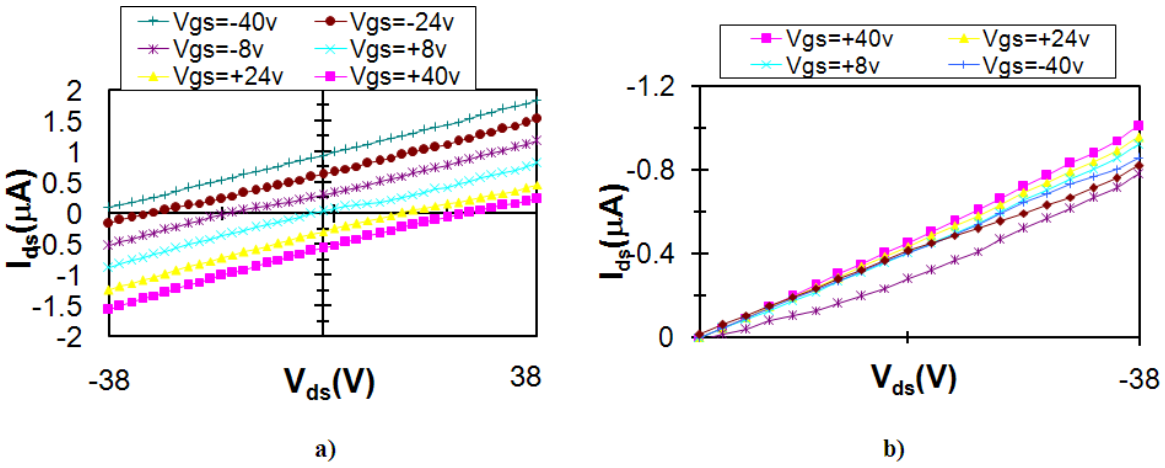


Figure 3.14. Measured output characteristics of a self-aligned transistor with defective gate insulator (L=50 μm and W=1000 μm).

Self-aligned transistors with a length of 50 μm and width of 1000 μm have a saturation current of around 1 μA and a saturation voltage of around -38 volts at a Vgs of -40 volts. Output characteristics in Figure 3.14a show leakage current that is comparable to the drain current. Deviation from ideal behavior can be observed on these output characteristics. Drain current modulation with gate voltage is less than expected for polythiophene transistors. Since the characterized transistors conduct substantial amount of drain current even when the gate-to-source voltage is +40 volts, we conclude that during the fabrication and measurement steps the excessive environmental doping and the deterioration of the polythiophene film occurred.

Sensitivity of P3HT to environmental oxygen and moisture is a well-known issue as a limiting factor for the polymer electronics from the device life-time and stability point of view [44]. Molecular oxygen causes the p-type doping of the polythiophene thus increasing the bulk conductivity of the polymer film whereas atmospheric water is found responsible for the creation of surface dipoles in the vicinity of semiconductor-insulator interface [45, 46]. If devices are not packaged properly both mechanisms result in large off-current and hence instability.

To evaluate possible leakage mechanisms a transistor can be modeled with additions of gate dielectric and bulk leakage resistances between the gate-drain, gate-source and drain-source regions (Figure 3.15). Average value of this total leakage resistor can be found to be around 80 $M\Omega$ from Figure 3.14a, which is comparable to the resistance of the semi-conducting polymer layer [47]. Since regular(not self-aligned) transistors showed no functionality, we conclude that destructive dielectric defects are present between gate and drain electrodes, as well as gate and source electrodes, in these transistors. Consequently, since there is practically no overlap between gate and source/drain electrodes in self-aligned transistors, we can assume that leakage resistance in these transistors mainly consists of bulk conductivity component. After removing the gate leakage effect analytically, the resulting Ids-Vds curves can be seen in Figure 3.14b.

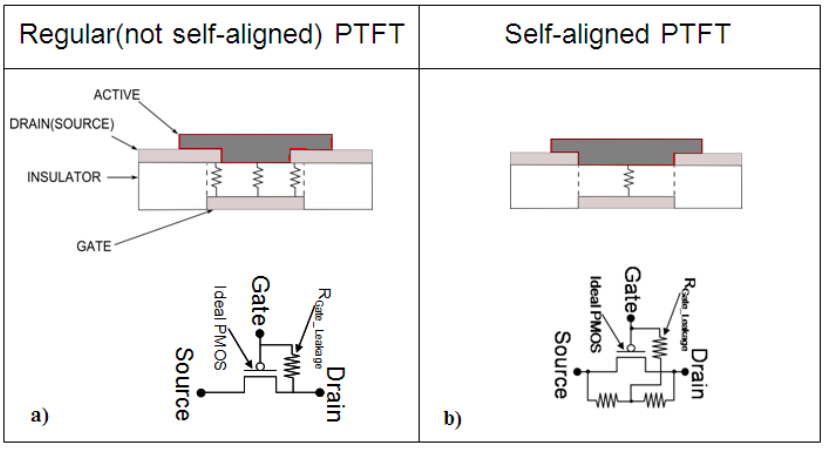


Figure 3.15. Device structures due to fabrication nonidealities.

3.3. Regular PTFTs

3.3.1. Fabrication of Bottom-Gate Bottom-Contact PTFTs

In the fabrication of PTFTs one of the most commonly used topologies is the so called bottom-gate bottom-contact(BGBC) topology as mentioned in the first chapter. This transistor structure has been very popular in the a-Si TFT fabrication for decades since it offers the advantage of minimum process steps and handling time after the semiconductor deposition.

In the fabrication of transistors of BGBC topology, deposition and patterning of the gate electrode material is done first. Commonly used materials for the gate electrode are ITO, gold, silver and aluminum. After the formation of gate electrode, gate insulator is deposited on top of the gate. Deposition method of dielectric material and be either spin-coating, printing, blading and spraying. Gate dielectric is usually regarded as one of the most crucial elements in polymer transistors thus a great deal of research is being carried on to improve the process compatibility of the available materials and also to synthesize new insulators through advanced chemical routes. The next step in fabrication is the formation of drain/source electrodes. Suitable metal or conductive polymer is deposited and patterned using standard lithographic methods.

The last step in the fabrication of a BGBC transistor is the deposition of the semiconducting polymer. Different deposition methods are utilized again depending on the semiconducting material. Semiconducting polymers soluble in organic solvents such as P3HT can be deposited by spin-coating, dip-coating, drop casting or printing. Thermal evaporation through a shadow mask is usually employed for deposition and patterning of pentacene. Since thermal evaporation needs a high vacuum it is not a commercially viable option for organic electronics which gained popularity by offering low-cost high-volume fabrication capability.

However, since pentacene has the highest hole mobility achieved up to date, pentacene precursor routes have been developed such as 6,13-bis(triisopropylsilylethynyl)-pentacene to take advantage of the processing abilities of the materials in solution. The main advantage of the BGBC topology lies in the deposition order of materials. With this topology active layer is subjected to least number of process steps that may lead to damage in the film morphology and hence a deteriorated device performance.

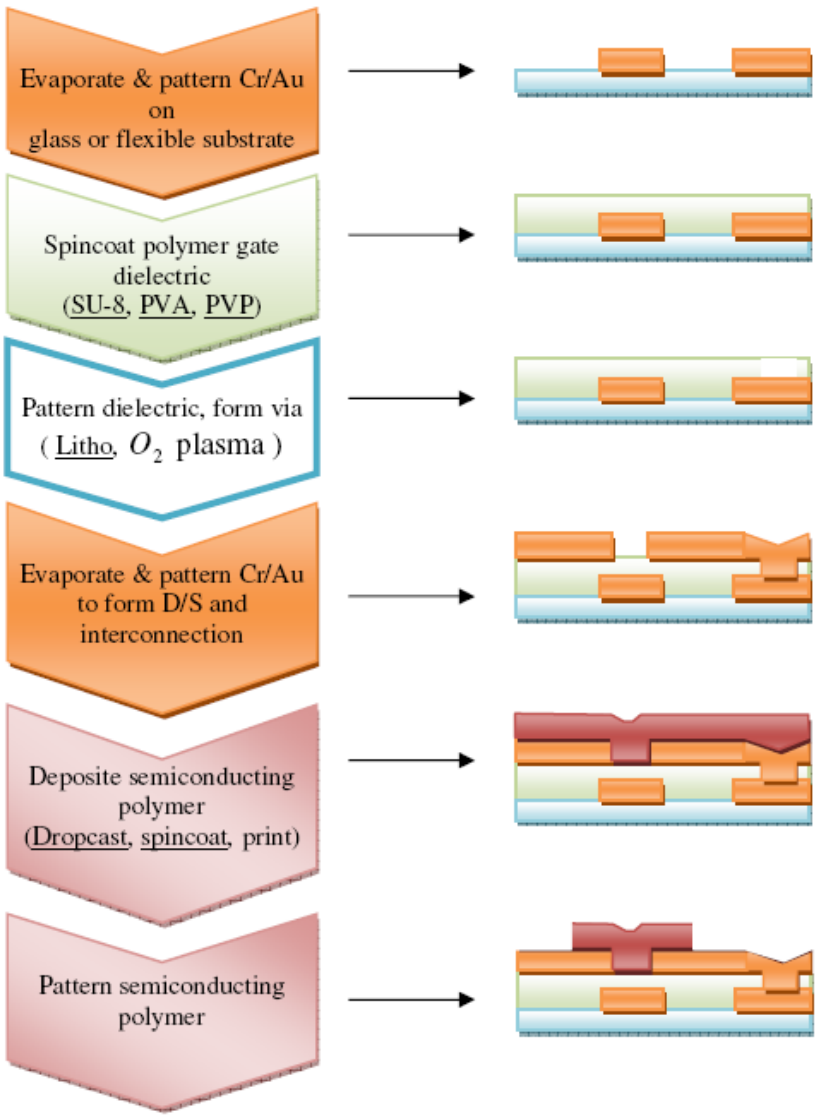


Figure 3.16. Process flow of the bottom-gate bottom contact transistors.

The process steps involved in the fabrication of BGBC polymer thin film transistors are depicted in Figure 3.16. Four inch glass wafers with 500 μm thickness are used as the substrate. Prior to the material deposition glass wafer is cleaned by a sequence of the following wet processes; 1hr soaking in 90 °C industrial detergent(Ulano Screen Degreaser Concantrate) diluted with de-ionized water followed by a rinse in de-ionized water, 10 min rinsing in acetone, 10 min rinsing in isopropyl alcohol and soaking de-ionized water. Wafer was placed in the the thermal evaporator and the vacuum pumped down to 10^{-6} Torr. At this vacuum level 5 nm chromium to serve as adhesion layer and 50 nm gold respectively is deposited on the glass substrate. Then for the patterning of the gate electrode Shipley S1828 photoresist spin coated at 2000 RPM and soft baked for 90 seconds at 90^{o}C on hotplate. After this, sample is exposed to UV light for 4 minutes through a transparency mask having 3000 dpi resolution. A picture of the transparency masks used throughout the photolithography is shown in Figure 3.17.

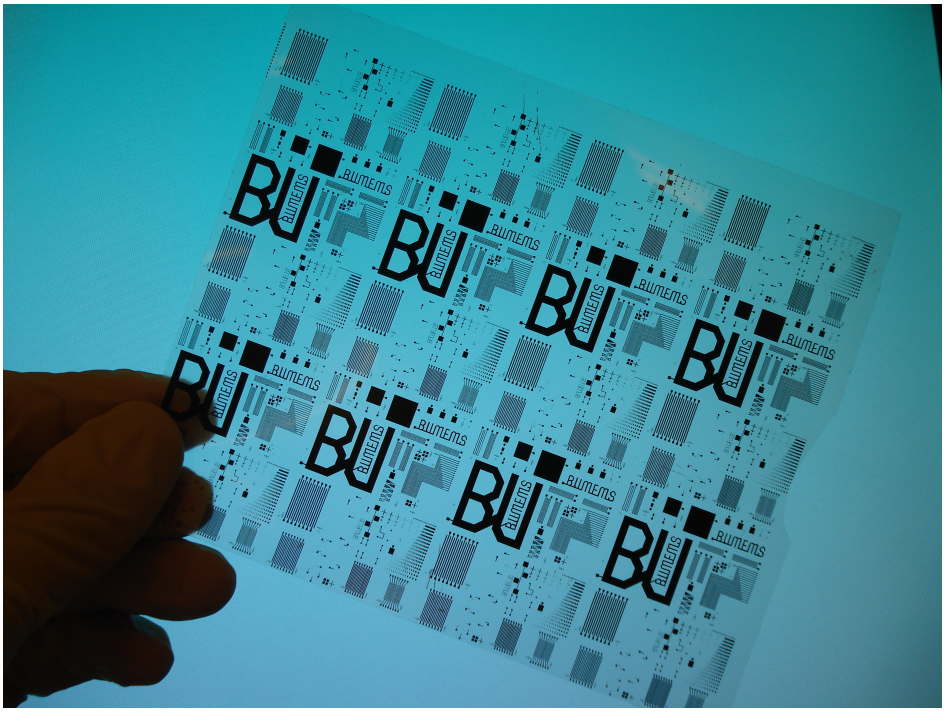


Figure 3.17. Picture of 3000 dpi resolution transparency mask.

Photoresist development is carried out in MF319 developer with gentle agitation for 5 minutes. A commercial gold etchant(Alfa Aesar) is used for gold etching. The time needed for complete removal of gold is found to be around 90 seconds. Custom made chromium etchant (%6 perchloric acid, %9 ceric ammonium nitrate, %85 di-water by weight) is employed for chromium etching. Since the chromium layer has 5 nm thickness, time required to etch is observed to be about 30 seconds.

The gate electrode formation is completed with chromium etch step and in order to strip the photoresist covering the electrode, sample is immersed in acetone for 5 minutes. However, it is observed that the photoresist removal was not successful even if sample is held in acetone at 60 °C with harsh agitation for a prolonged time. Possible causes for this difficulty in photoresist removal predicted to be either the pressure applied on the photoresist in the UV exposure step or the hardening affect of the chromium etchant on the photoresist. During the UV exposure photoresist is sandwiched between the photomask and the glass substrate, in order to increase the resolution sufficient amount of pressure is needed to make sure there is no gap between substrate and the mask. Because the residual photoresist is only found to remain on the metal pattern edges it is also likely that the chromium etchant diffuses into the photoresist during the chromium etch step and causes photoresist to get harder at that location.

If the removal of the polymeric material from the surface is problematic then dry etching is usually adopted to achieve the desired result. In our case we used DC oxygen plasma etching in a custom-made setup to burn out the residual photoresist. Plasma is generated in a vacuum chamber with Oxygen and Argon gas mixture. First vacuum is pumped down to 20 mTorr then Argon is let into the chamber until it reaches 300 mTorr pressure, by slowly increasing the DC voltage between counter electrodes to 170V until plasma generation is initiated. Then oxygen is introduced until oxygen to argon ratio becomes 1/4 thus pressure sensor displayed 400 mTorr.

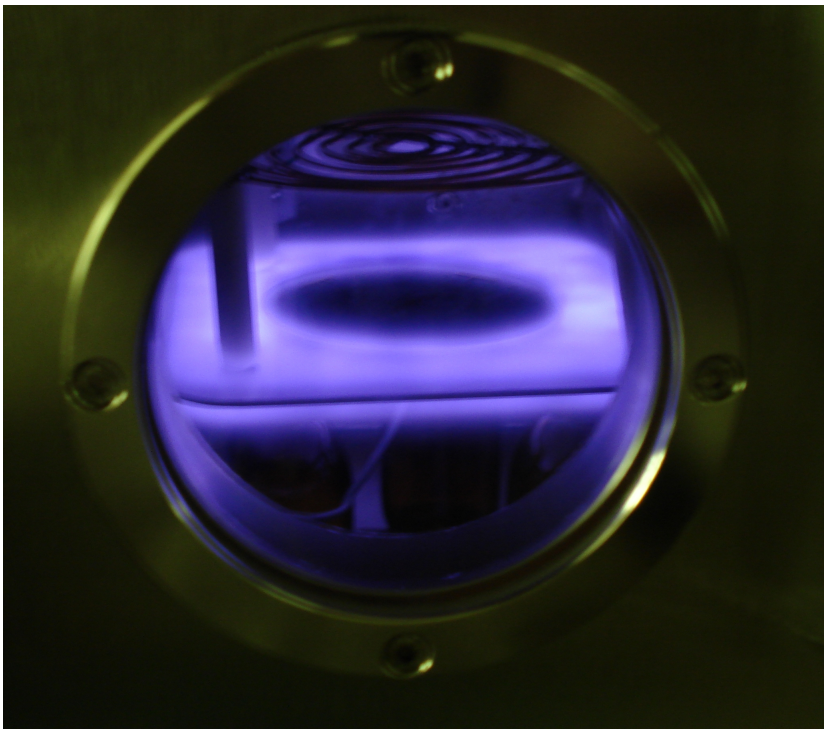
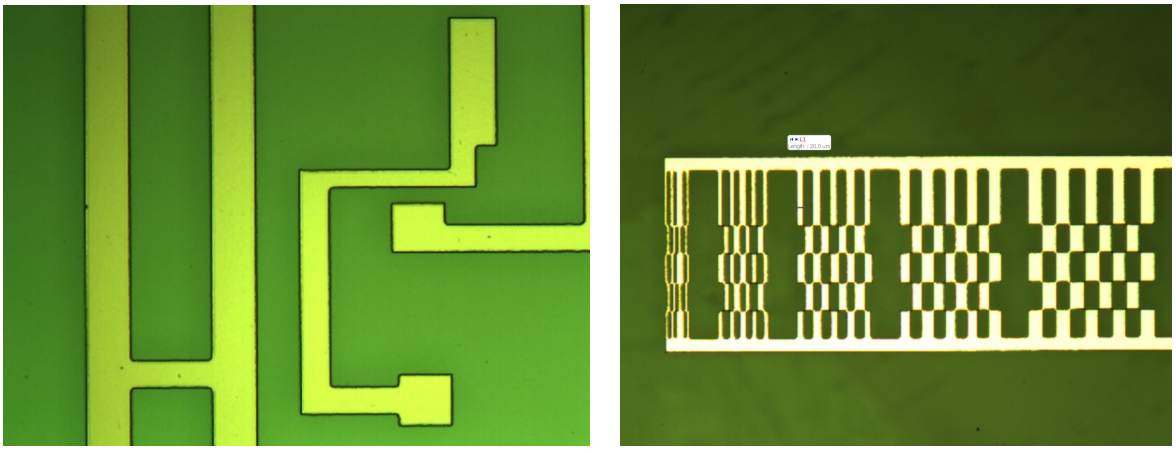


Figure 3.18. Oxygen plasma etching.

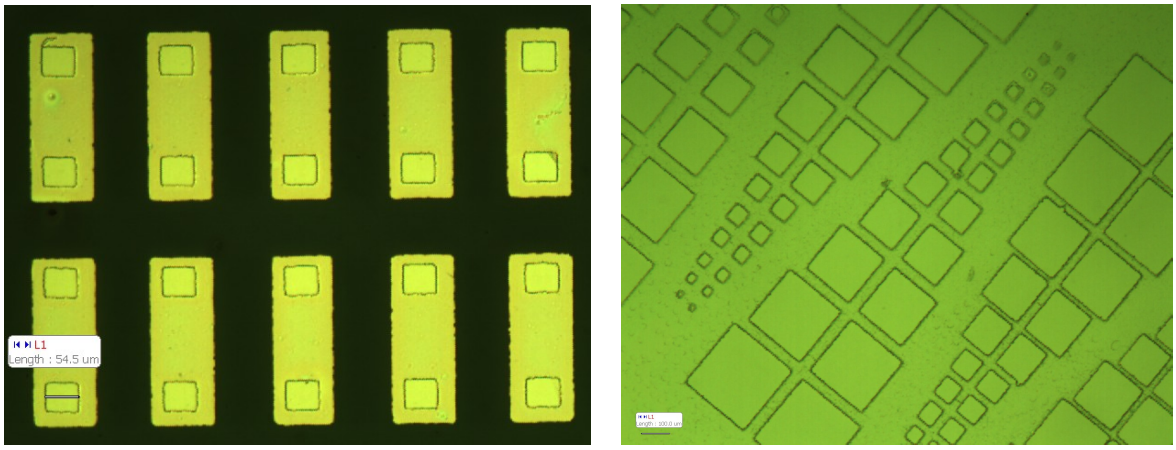
By manually adjusting the gas valves a stable plasma generation is obtained and the sample is exposed to the plasma for nearly 3 hours leading to the complete removal of the residual photoresist from the surface. The picture taken during plasma etching is in Figure 3.18. Figure 3.19 shows the resulting gate electrodes.



(a) Gate electrodes (b) Resolution test pattern

Figure 3.19. Patterned Au on glass substrate.

Following the gate electrode formation, gate insulator deposition and patterning comes next in the process. SU-8 200.5 permanent epoxy is spin-coated at 4000 RPM, soft-baked at 100 °C for 5 min. Since SU-8 forms a quite brittle film especially if coated as a thin film, temperature treatment must be done carefully. Because of that hot plate surface temperature is ramped-up and ramped-down gradually when heating and cooling, respectively throughout SU-8 processing. After cooled-down to room temperature, wafer is taken to the exposure system. 5 minute UV exposure is found to be sufficient for our case. Cross-linking of the polymer chains which gives the permanency to SU-8 on the deposited surface does not happen during the UV exposure but in the following hard-bake step. Hard-baking at 120 °C for 20 minute is sufficient to obtain a crack-free permanent gate dielectric film over the gold electrode. SU-8 film developed in Microposit SU-8 developer for 5 minutes. Wafer is rinsed in isopropyl alcohol and dried with nitrogen flow subsequently. Patterned SU-8 layer images can be seen in Figure 3.20.

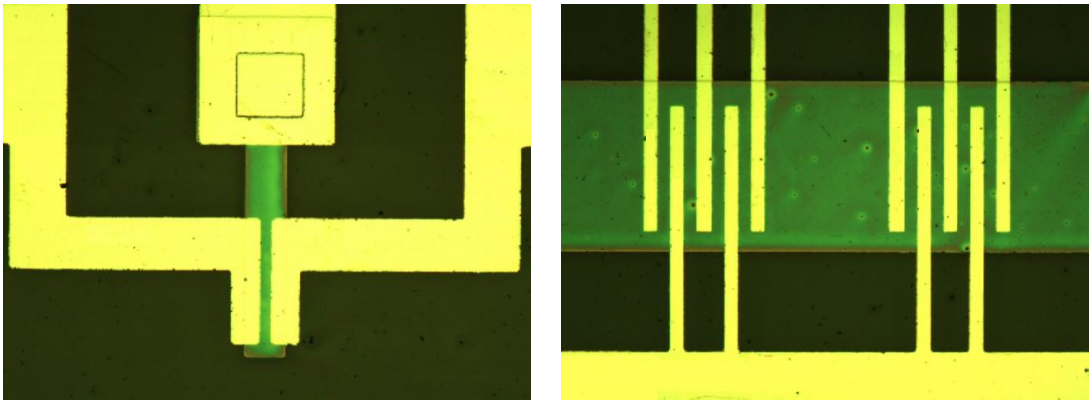


(a) Via openings (b) Patterned SU-8 on glass

Figure 3.20. SU-8 patterns.

Gold was chosen as drain and source electrode material due to its high work function of 5.1 eV which forms ohmic contacts with P3HT and hence allows injection of holes into the active layer efficiently.

Deposition and patterning of gold is performed by the same procedure described for the gate electrode fabrication. The only difference to take into account was to keep the chamber of the thermal evaporator and the target below a certain temperature while metals are being evaporated. If temperature goes above this level the underlying SU-8 film may experience dimensional distortions which may lead to the development of cracks in the dielectric layer. Microphotographs of transistors after drain/source electrode formation and prior to the active layer deposition is presented in Figure 3.21.



(a) Regular drain/source geometry (b) Interdigitated drain/source geometry

Figure 3.21. Transistors prior to the P3HT deposition.

Active layer together with gate dielectric plays the most crucial role in a polymer thin film transistor. Transistor performance is greatly influenced by the molecular orientation of the semiconducting material. The density of charge carriers electrons or holes generally increase with the molecular chain ordering or improved crystal order [48]. Molecular orientation changes considerably with the processing conditions. Film deposition using solvents with different boiling points also results in very different field effect mobilities [49][12]. Relatively higher hole mobility can be obtained if the deposition is realized from high boiling point solvents. Deposition method also leads to different mobilities. The most conventional methods for the deposition of P3HT are spin-coating, drop-casting and dip-coating. Among these methods, dip-coating and drop-casting usually forms higher mobility films than spin-coating [50].

In our work, drop-casting was chosen as the deposition method of active layer due to its simplicity. rr-P3HT solution was prepared to have 2 mg/ml concentration in chlorobenzene which has a boiling point of 131 °C. Since the P3HT was kept in a sealed bottle in ambient, some environmental doping of the polymer is expected. In order to remove the unintentional oxygen the solution is stirred at 60 °Cfor 3 hours with a constant nitrogen flow through a piece of syringe needles causing a circulation in the solution thus increasing the oxygen desorbing rate. rr-P3HT solution is drop-casted over the drain/source electrodes with a syringe. The wafer was covered with a petri dish and kept for half an hour to reduce the solvent evaporation rate which is known to increase the molecular ordering of the P3HT film.

Deposition of the active layer finalizes the fabrication procedure of bottom-gate bottom-contact thin-film transistors. Completed wafer is shown in Figure 3.22.

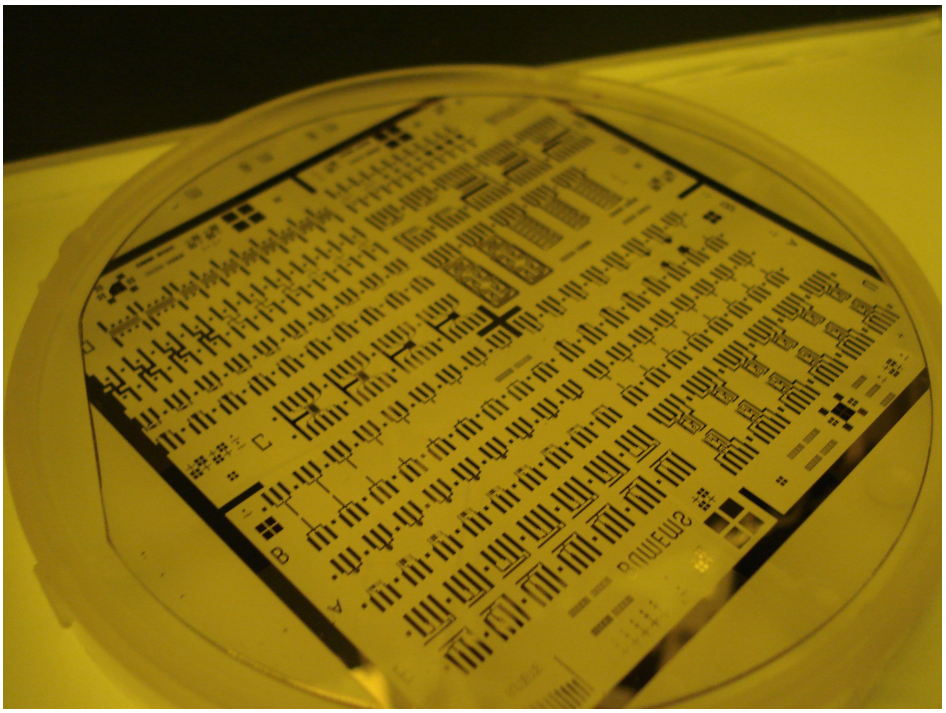


Figure 3.22. Completed four inch wafer prior to active layer deposition with patterned gate electrode, gate insulator and drain/source electrodes.

3.3.2. Measurement Results and Comments

Transistors are measured and characterized on Cascade probe station under dark in ambient air with Keithley SCS-4200 semiconductor parameter analyzer.

A picture showing one of the measured transistors can be seen in Figure 3.23. Output and transfer characteristics of the interdigitated transistors with 30 μm channel length and 1000 μm width are shown in Figure 3.24 and Figure 3.25, respectively. To see the output characteristics drain voltage is swept from 0V to -40V for three different gate voltages and the resulting drain current is plotted. From the output curves it can be observed that the gate voltage has a little effect on the accumulation of mobile carriers from the bulk. Furthermore the drain current is expected to be saturating above a certain drain to source voltage whereas it tends to be linearly increasing with drain voltage. This kind of output characteristics are found to be common in transistor employing P3HT as active layer when the devices are fabricated in ambient [3]. In general, most of the solution-processed organic polymers are unintentionally extrinsically p-type. It is argued that oxygen is acting as traps for electrons and polymer sensitivity to unintentional doping is due to its low ionization potential [51]. For P3HT PTFTs fabricated in a glove box, exposure to air for a few minutes is sufficient to produce extrinsic doping.

In transistors exposed to air, gate voltage fails to modulate the carrier concentration in the channel because the active layer already contains a significant amount of dopants thus the accumulated charge density near the insulator/P3HT interface is smaller compared to the doping induced charges. If the excessive doping of the P3HT from the environment is the case then the active layer behaves more like a resistor rather than a semiconductor.

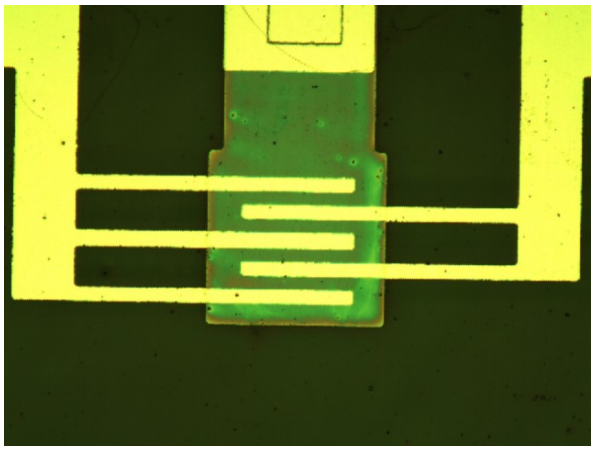


Figure 3.23. Interdigitated transistor($L = 50$ μm $W = 1000$ μm).

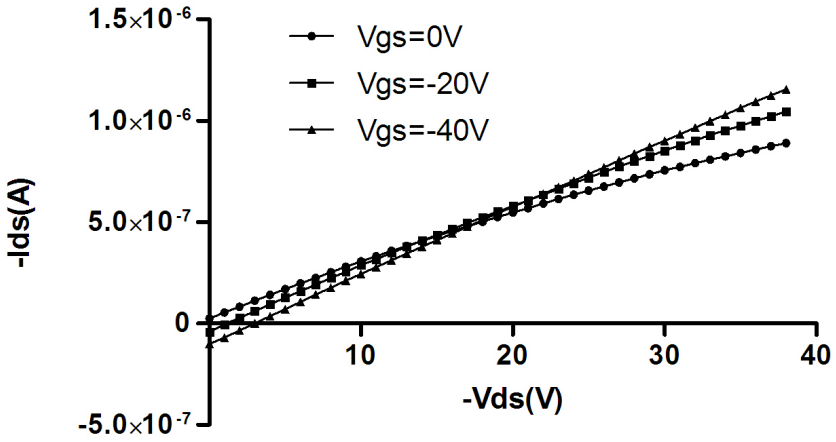


Figure 3.24. Output characteristic(interdigitated, $L = 30$ μm $W = 1000$ μm).

Transfer characteristic of the transistor is also a linear function of gate to source voltage. Even at the zero gate voltage drain current of 600 nA flows through the device. This results in a quite low on-off ratio of about 1.5 which means actually it is not possible to turn the transistor off at all.

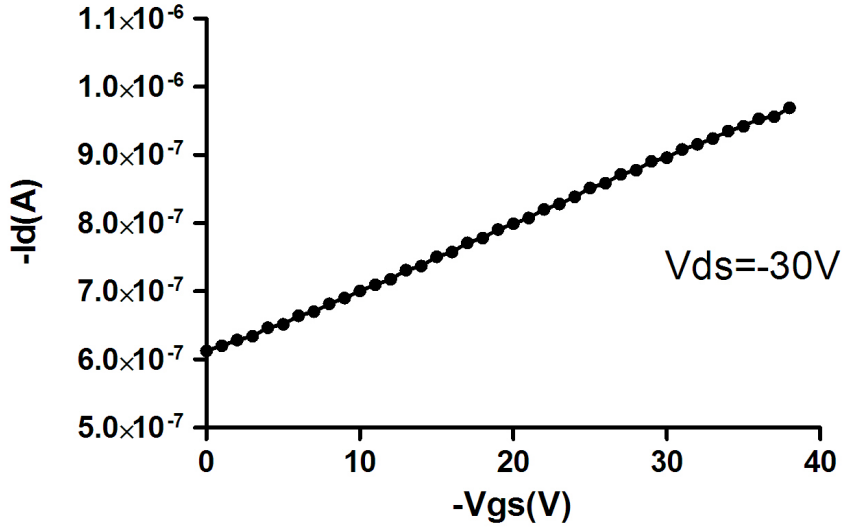


Figure 3.25. Transfer characteristic(interdigitated, $L = 30$ μm $W = 1000$ μm).

Interdigitated transistors with lower aspect ratio (L=50 μm W=1000 μm) fabricated in the same process showed similar characteristics (Figure 3.26 and 3.27). Due to longer channel length, drain current at the same drain-source voltage was smaller as well as the drain current at the zero volt gate voltage compared to the transistors having higher aspect ratio as expected.

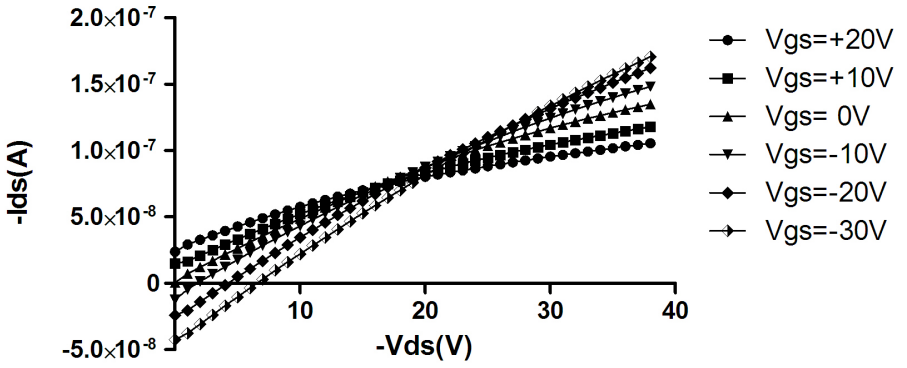


Figure 3.26. Output characteristic(interdigitated, $L = 50$ μm $W = 1000$ μm).

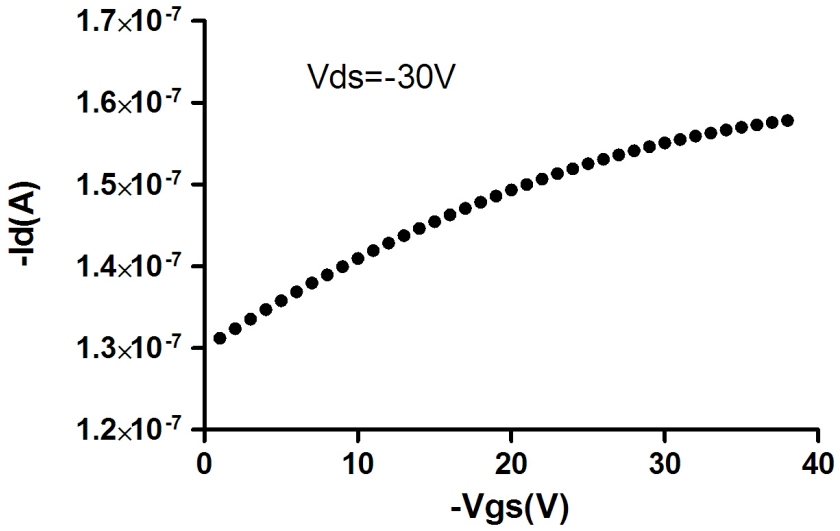


Figure 3.27. Transfer characteristic(interdigitated, L=50 μm W=1000 μm).

Independent from the PTFT device structures mentioned in Chapter 2, there are different possible drain-source electrode arrangements. Previously showed interdigitated layout is one of these and offers a reduced transistor area owing to its comb like electrode geometry. Interdigitated structure is widely used in PTFT transistors because in organic circuits transistor widths are usually on the order of several hundred micrometers to ensure a specific functionality and logic level. Another topology also used in polymer transistors is the so called corbino layout. In corbino arrangement, drain completely surrounds the source electrode thus the leakage paths through the active layer, which will be discussed in the following section, are practically eliminated [53]. Figure 3.28 shows a picture of corbino-like transistor. In this picture, drain does not completely enclose the source electrode because in that case additional fabrication steps would be required to make an electrical connection to the inner source electrode. To be more specific, after the active layer deposition step, an insulating passivation layer compatible with the semiconducting film should be deposited on top of the active layer, vias should be opened in this passivation layer and another metal layer should be deposited and patterned for electrical connection between the source electrode and another part of the circuit.

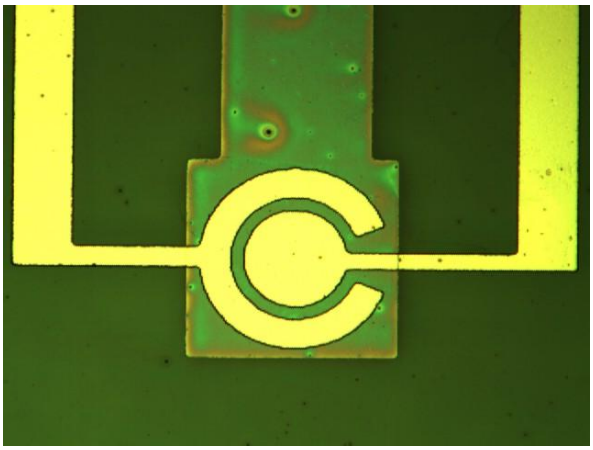


Figure 3.28. Corbino layout transistor(r1=15 μm r2=18 μm).

That said, however the corbino-like transistor seems to be doing well in the reduction of the leakage current through active layer as can be seen from the reduced offset current around the origin from output curves in Figure 3.29. Transfer characteristics is shown in Figure 3.30, a quite low on/off ratio of about two is obtained for the gate voltage sweep of 40 volts.

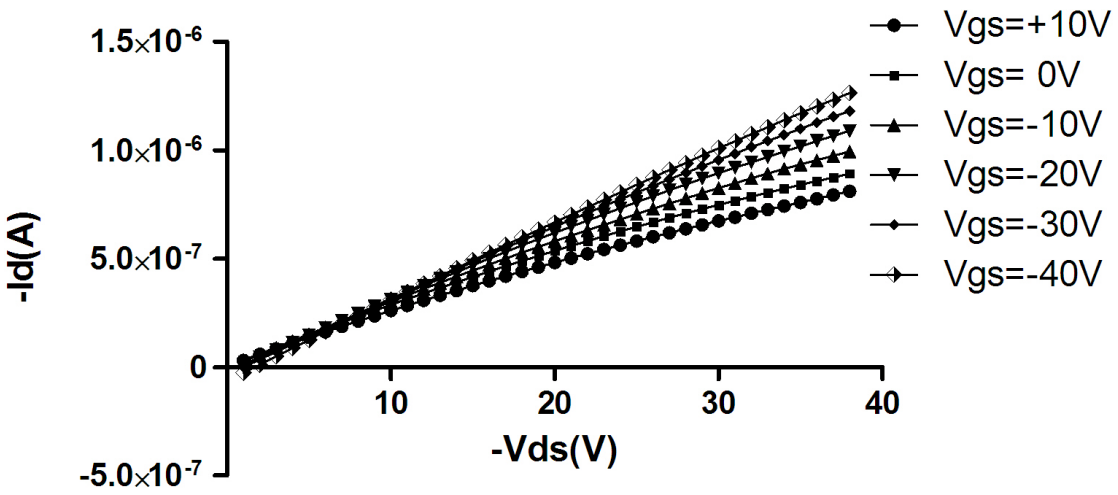


Figure 3.29. Output characteristic(Corbino, r1=15 μm r2=18 μm).

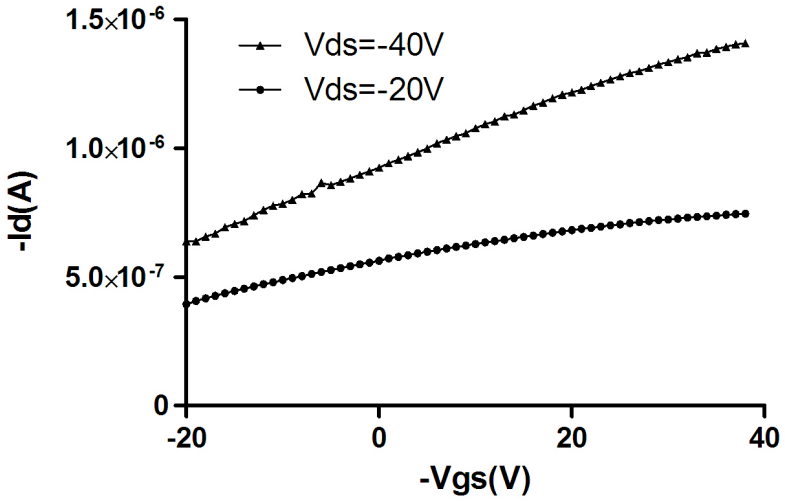


Figure 3.30. Transfer characteristic(Corbino, r1=15 μm r2=18 μm).

3.3.3. Patterning of the Active Layer and Its Effect on the PTFT Performance

The ability to pattern micro and nano structures is the essential part of the modern electronics. For the several decades, advances in the patterning techniques resulted in the higher performance electronic devices and circuits.

Therefore all organic electronic devices also require patterning. Devices based on organic semiconductors such as light-emitting diodes, organic transistors, solar cells and organic sensor systems can be fabricated on wide variety of substrates like glass, silicon wafer,metal foils, flexible transparent substrates, paper and even on clothes. Owing to this property, there is an intense interest in the large area, high throughput and hence low-cost electronics based organic materials. However in all these devices organic materials need to be deposited in thin film form (usually between 1 nm to 10 μm). This presents a considerable challenge in the handling of these devices. Since organic solids have distinct physical and chemical properties that brings some limitations on the applicability of the common processes developed for inorganic device patterning.

Discrete elements of the inorganic solids are covalently bonded to each other whereas organic solids are held together by the weak Van der Waals bonds which make them prone to be damaged during processes involving high temperatures, high energy plasma and exposure to solvents. While standard photolithography based methods have been successfully demonstrated for organic device fabrication, they are far from being low-cost processes. Therefore, several process technologies need to be developed to reliably deposit and pattern organic materials on variety of substrates and at the same time they must be viable in terms of cost, speed and area concerns.

Specifically, the search for patterning methods for the organic semiconductor is particularly important for the commercialization of the organic transistors. As an example, one of the potential application area of the PTFTs are active matrix OLEDs as mentioned earlier. In AMOLED displays, each organic LED is driven by a PTFT. Therefore, any deviation of the transistor drain current from ideal case directly affects the OLED current and hence the image quality. In order the provide a high contrast ratio, off current of the PTFTs needs to be as low as possible [52]. One of the factors leading to increased off current in these transistors is the non-patterned semiconducting layer. Digital circuits also suffer from non zero drain current, elevated off-currents results in a reduced noise margin which is the direct measure of a circuit reliability.

In this thesis two different methods are developed for the deposition and patterning of the semiconducting polymer rr-P3HT. The first method is known as micromolding in capillaries(MIMIC) and allows the deposition and the patterning of the polymer to be simultaneously. The second method is based on subtractive lithography. Polymer is lifted-off from the surface (except the active area of the transistors) in a compatible solvent.

MIMIC is a molding technique that relies on the spontaneous filling of the micro-channels of a mold with a fluid to be patterned [54][55]. This method is used to pattern drain/source electrodes and the active layer of the organic transistors previously [56][57]. Steps involved in the patterning of the rr-P3HT with MIMIC process is illustrated in Figure 3.31. The key component of MIMIC is the mold that is used to give the final shape of the deposited material. In order to assure high resolution and pattern quality, conformal contact must be established between the substrate and the mold. Therefore an elastomeric stamp such as cross-linked poly(dimethylsiloxane)(PDMS) is usually employed in the molding process.

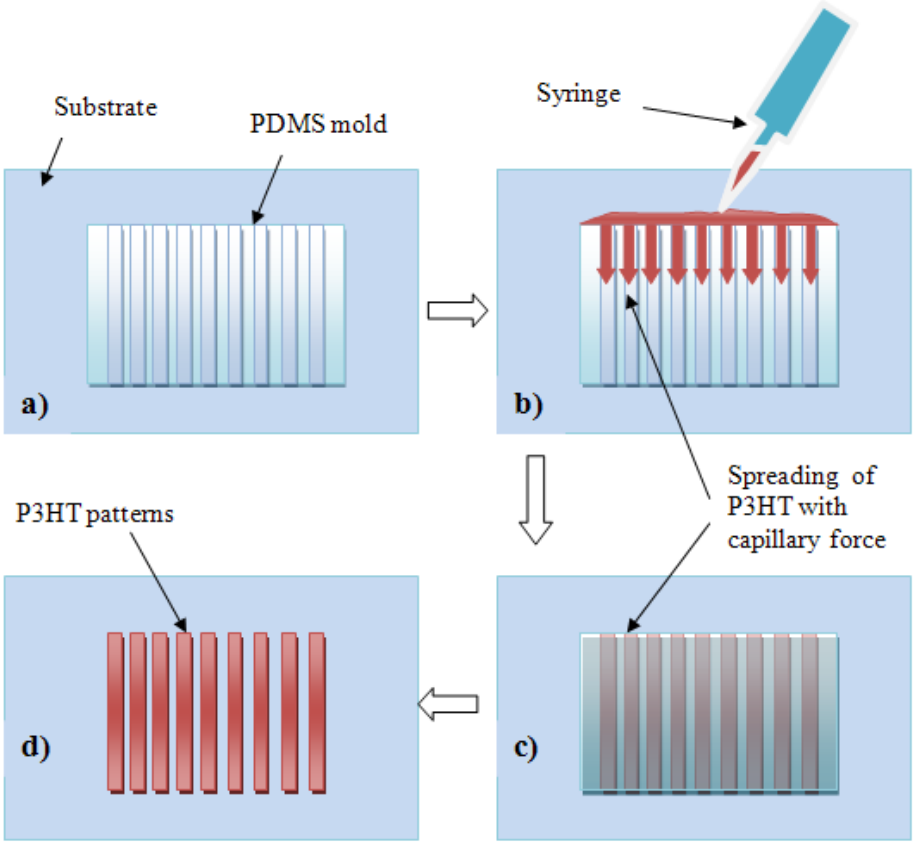
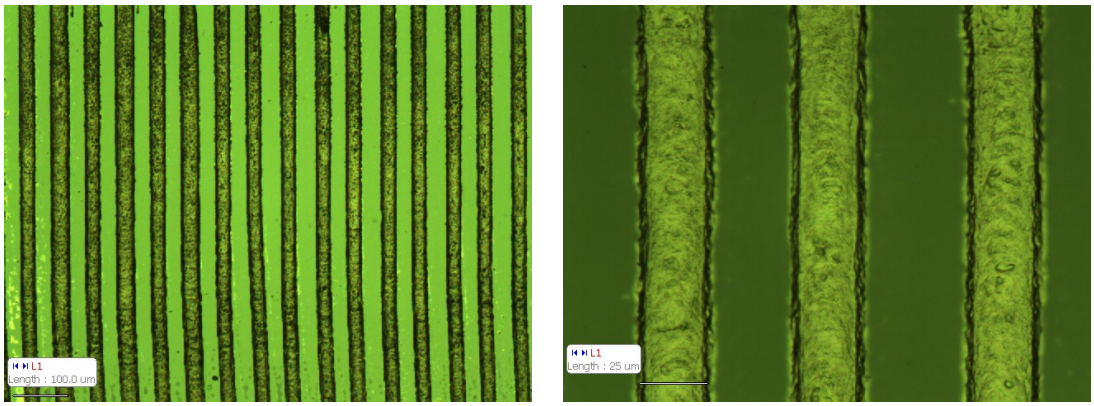


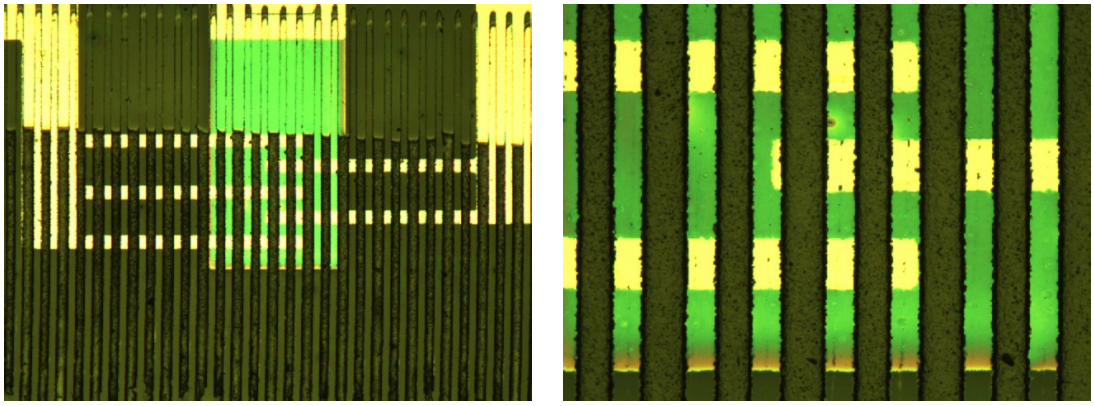
Figure 3.31. MIMIC process flow a)PDMS mold brought in contact with the substrate b)rr-P3HT in chlorobenzene is dispensed with a syringe c)capillary force drives the solution into the channels d)removal of the mold



(a) rr-P3HT lines created with MIMIC (b) A closer view

Figure 3.32. rr-P3HT patterned on glass wafer by MIMIC.

MIMIC was carried on as follows. First, rr-P3HT is dissolved in chlorobenzene to give a concentration of 2 mg/ml. PDMS mold brought into contact with the substrate. In order to limit the distortion of the PDMS caused by chlorobenzene, a uniform pressure is applied with the aid of another glass wafer from the top of the PDMS stamp. rr-P3HT solution is dispensed with a syringe at the end of the mold and waited until the channels are filled with the solution by capillary action. Patterned polymer is therefore the negative replica of the mold. Sample is left in air overnight to make sure the solvent is fully evaporated and polymer film is hardened enough for the safely removal of the mold. P3HT line patterns after mold removal are shown in Figure 3.32. Microphoto of a PTFT with patterned active layer is in Figure 3.33



(a) Interdigitated transistor($L = 50$ μm, $W = 1000$ μm) (b) Close view of the interdigitated transistor

Figure 3.33. Fully patterned interdigitated PTFT.

The second method employed to pattern polymeric semiconductor rr-P3HT is lift-off. Lift-off is a simple, easy method usually need to make metallic patterns on a substrate, especially for those noble metal thin films such as platinum, tantalum, nickel or iron which are difficult to be etched by conventional methods. The general lift-off process is: First a pattern is defined on a substrate using photoresist. A film, usually metallic, is deposited all over the substrate, covering the photoresist and areas in which the photoresist has been cleared by developing. During the actual lifting-off, the photoresist under the film is removed with solvent, usually in acetone, also taking the film with it and leaving only the film which was deposited directly on the substrate.

Lift-off being a widely utilized subtractive method in the fabrication of any kind of devices such as MOSFETs, LEDs and several MEMS components, it has been rarely used in the patterning of the polymeric films of organic electronic devices. In [58], lift-off is used to pattern drain, source and gate electrodes of an organic transistor which are deposited from poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid(PEDOT-PSS).

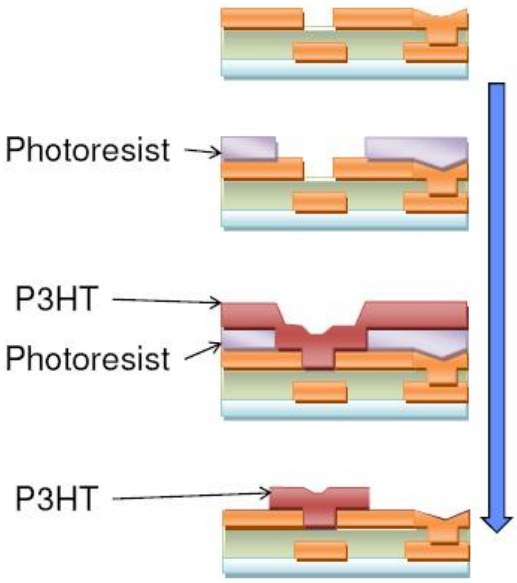


Figure 3.34. P3HT lift-off process flow.

The process flow of the lift-off method we applied for the patterning of rr-P3HT film is shown in Figure 3.34. Starting with the previously mentioned bottom-gate bottom-contact TFT topology, we have Au gate,drain and source electrodes and SU-8 2000.5 polymeric insulator pre-deposited and patterned. Then first step in the process is spin-coating of the photoresist S1828 at 2000 RPM, soft-bake at 90 °C for 1min, exposure to UV light, developing in common MF319 developer and rinsing in de-ionized water. Following photoresist patterning, rr-P3HT from 1mg/ml chlorobenzene solution is spin-coated at 1000 RPM. In this stage, compatibility of the rr-P3HT solvent with the underlying photoresist is an important factor determining the resulting film quality. Many solvents common for P3HT are found to dissolve the photoresist S1828, therefore chlorobenzene is chosen as a solvent which is known to harden the photoresist surface but no particular dissolving effect at all [59].

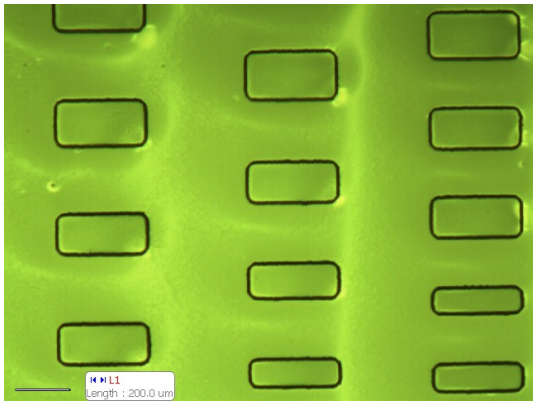
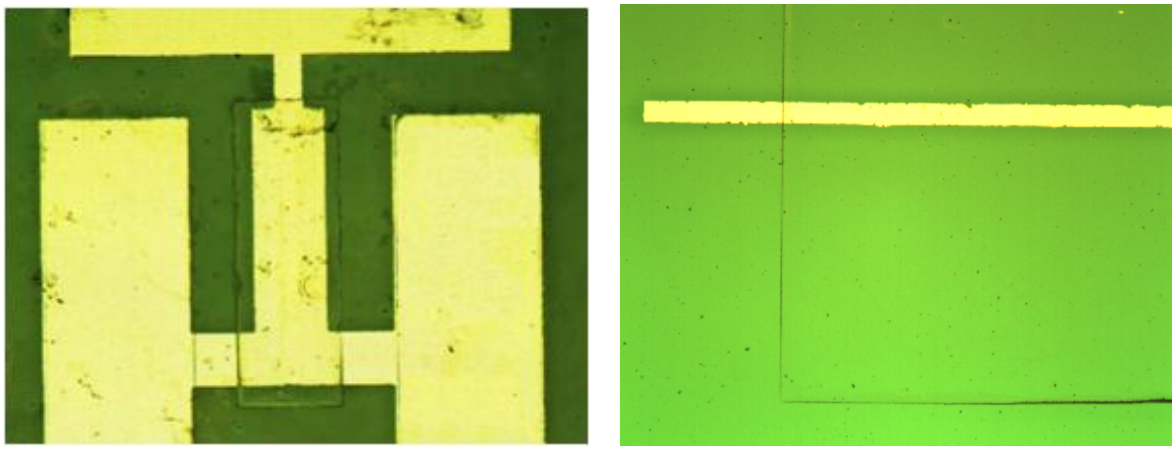


Figure 3.35. Spin-coated rr-P3HT from chlorobenzene solution (1 mg/ml).

Following rr-P3HT deposition, sample is placed on hot plate and heated at 90 °C for 2 min to ensure all the solvent is evaporated in P3HT film. In Figure 3.35 spin-coated film of rr-P3HT over pre-patterned photoresist is shown. After P3HT deposition, lift-off is performed in 2-Propanol. Usually acetone is the preferred solvent for negative photoresist removal in lift-off, however when patterning polymeric films with this method we found that the slower the dissolution rate of underlying photoresist during the removal step, the better the obtained polymer pattern resolution is.



(a) Fully patterned transistor(L=50 μm W=1000 μm)

(b) Close view of the patterned rr-P3HT

Figure 3.36. Pictures of P3HT film patterned by lift-off.

Pictures of P3HT film patterned by lift-off is shown in Figure 3.36.

As mentioned earlier, transistors with patterned active layer show superior device characteristics as compared to non-patterned transistors. If we concentrate on the 0V drain voltage point in the output characteristics of the transistors an offset voltage can be observed in contrast to an ideal device characteristics in which the drain current curves would be passing from the origin. This offset voltage at 0V drain-source voltage results either from the defects in the gate dielectric or the non-patterned active layer. Actually both effects are caused by the fact that P3HT film conducts a considerable amount of current even if the channel is not accumulated. In the first situation, a low resistance path exists over the defect location between the gate and the source/drain so that when the drain-source voltage difference is at 0V and the gate voltage is at some voltage level other than 0V, a non-negligible current flows through this parasitic resistor. An explanatory schematic of this kind of non-ideality has already been mentioned in section 3.2 of this chapter.

In the second case, non-patterned active layer may cause two kinds of leakage paths; one is through the periphery of the transistor and the other one through the via (Figure 3.37). Assuming the gate dielectric film is defect-free and robust, non-patterned active layer surrounding the effective transistor area forms a resistor between drain and source contacts giving rise to the leakage current even when the gate voltage is below 0 V (for p-type PTFTs). This leakage path is shown with the dashed line numbered 1 in Figure 3.37. However, this kind of leakage should not be causing an offset around the origin in the Id-Vds curves because in principle there should be no voltage difference and hence no current flow between the two parasitic resistor terminals(drain-source) when the drain-source voltage is 0V. That said, we can focus on the leakage path 2 in the figure for the explanation of the offset voltage. In general, most of the PTFT fabrication technologies contain only two levels of metal layers. One layer for the gate electrode and another one for the drain/source electrodes. In the case of BGBC PTFT structure is employed, active layer is deposited on the second metal layer which has a direct electrical connection to the first metal layer through the via. Therefore, a leakage path is established between gate and the drain/source electrodes as shown with path 2 in Figure 3.37. We conclude that, this second leakage path must be responsible for the offset voltage, provided that the gate insulator is defect-free.

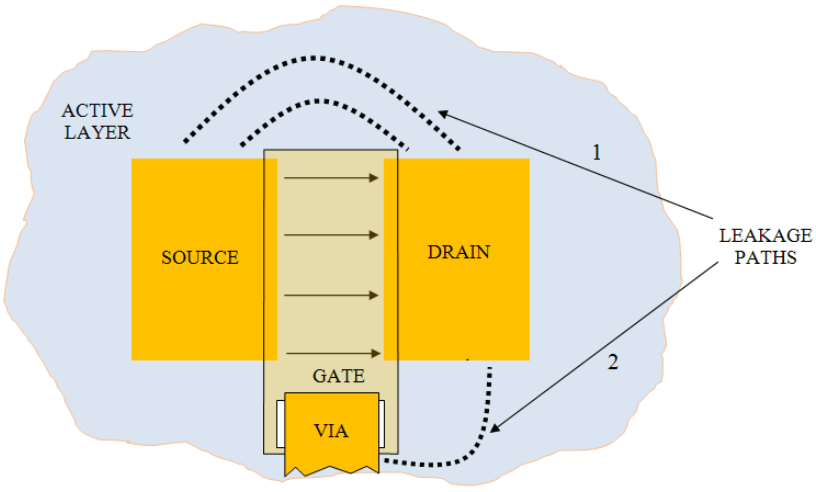
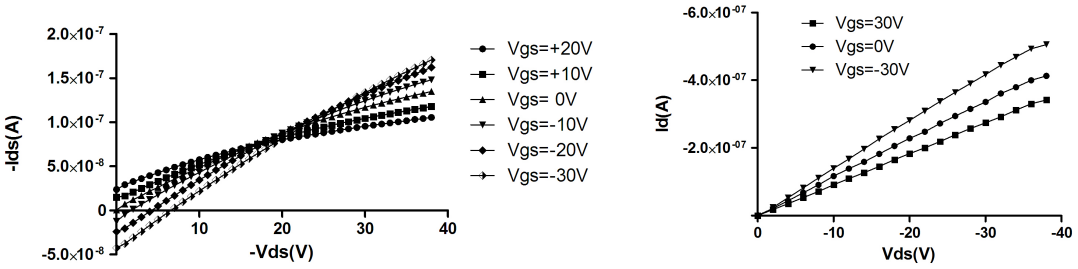


Figure 3.37. Leakage paths due to un-patterned active layer.



(a) Before P3HT patterning (b) After P3HT patterning(MIMIC)

Figure 3.38. Output characteristics of an interdigitated PTFT before and after active layer patterning (L=50 μm W=1000 μm).

Figure 3.38 shows device characteristics of a PTFT with un-patterned and patterned active layer. Patterning method is MIMIC. You can see that there is no offset in the Id-Vds graph of the patterned device. Similarly, Figure 3.39 shows device characteristics results of the PTFT having active layer patterned by lift-off. Again, the offset is not observed.

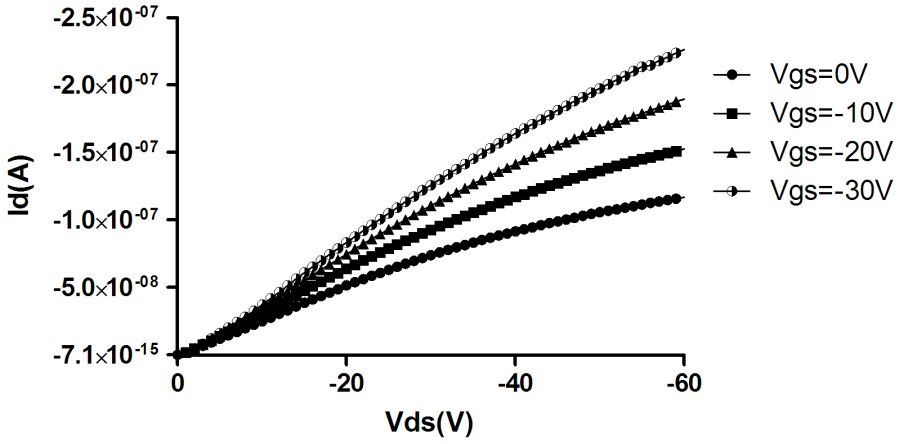


Figure 3.39. Output curves of the fully patterned transistor (Lift-off, L=50 μm W=1000 μm).

3.4. PTFTs with Silver Epoxy Drain/Source Electrodes

In the research of organic electronic devices, various factors need to be examined for the optimization of the device performance. Before the process design for batch fabrication explorations must be performed on discrete devices which provide valuable insights for better understanding of the device behavior and the several variables affecting these characteristics. Therefore, a simpler and faster fabrication method is employed for measuring and characterization of discrete polymer TFTs at lab scale. This method eliminates the metal evaporation efforts required to deposit and pattern the drain and source electrodes in the fabrication of discrete bottom gate coplanar PTFTs thus makes the characterization and testing of these devices faster and simpler.

Illustrated cross-sectional view of the discrete transistors patterned with the suggested method is depicted in Figure 3.40. The substrate on which the discrete transistors fabricated can be any kind of substrate pre-coated with an electrically conducting film. In this thesis work silicon wafer, glass wafer, ITO coated glass and ITO coated PET are used as substrate. The polymeric gate dielectric layer consisted of either SU-8 2000.5 and poly(4-vinyl phenol)(PVP) or poly(vinyl alcohol)(PVA). Gate dielectric material is deposited by spin-coating and converted to a permanent layer by subsequent cross-linking and curing processes. Patterning of the dielectric layer is avoided in order to prevent possible defect generation.

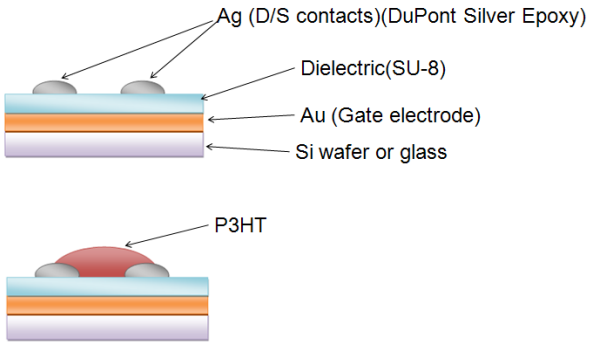


Figure 3.40. Cross-section of the PTFTs with Silver Epoxy Drain/Source Electrodes.

PVP dissolved in propylene glycol 1-monomethyl ether 2-acetate (PGMEA) to give a concentration of 7 wt % . Poly(melamine-co-formaldehyde) is used as the cross-linking agent for PVP and PGMEA/PVP weight ratio of 1/4 is chosen. Spin-coated at the speed of 2000 RPM and cross-linked on hotplate at 140 °C for 30min and additional 30 min at 200 °C at 1Torr vacuum. Process details for SU-8 deposition are the same as used for fully patterned transistor in chapter 3 section 2.

PVA is another polymeric gate dielectric commonly used in PTFTs. PVA (Aldrich) is dissolved in de-ionized water to obtain a concentration of 5 mg/ml. Solution in a glass bottle, is continuously stirred at 140 °C on hotplate for 3-4 hours to achieve homogenity. Ammonium di-Chromate crosslinking agent to PVA weight ratio is 1/5. Cross-linking is achieved by first UV exposure of 5 minute and subsequent hard-baking at 140 °C on hotplate. Drain and source electrodes of the TFTs are drop-casted from conductive silver paste (DuPont 5000) under microscope. Finally, 2mg/ml rr-P3HT solution in chlorobenzene is drop-casted on Ag electrodes and sample is covered by a petri dish and left in ambient for solvent evaporation. Figure 3.41 shows the I-V graph of the Ag-P3HT-Ag lateral structure. From this graph, we conclude that the Ag-P3HT contact is ohmic in nature since the current increases linearly in both negative and positive voltage sweep directions around the origin.

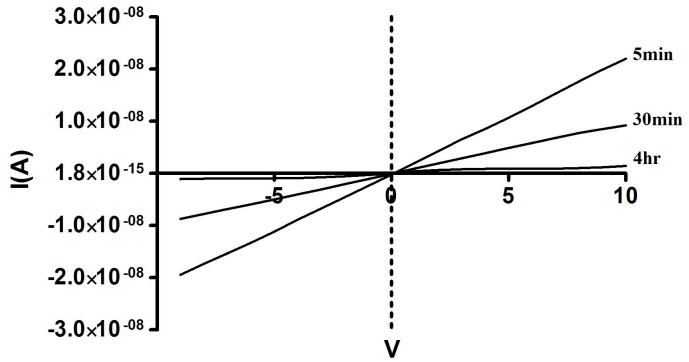


Figure 3.41. I-V sweeps of rr-P3HT film between lateral Ag electrodes as time progresses in vacuum.

Figure 3.42 and Figure 3.43 are the output and transfer characteristics of the PTFT, respectively, having double layer gate dielectric consisting of PVP and SU-8.

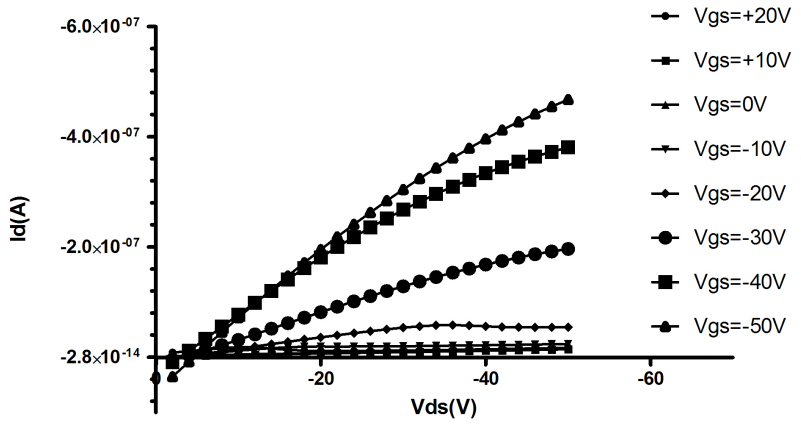


Figure 3.42. Output characteristics of PTFT with Ag drain/source ($L = 200$ μm, $W = 800$ μm).

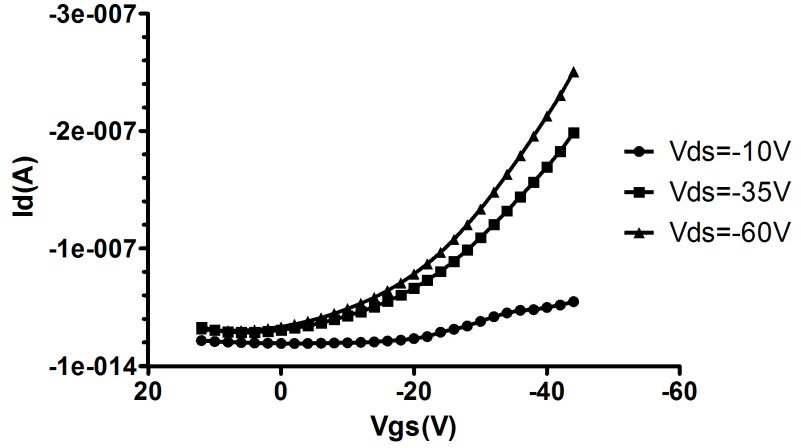


Figure 3.43. Transfer characteristics of PTFT with Ag drain/source ($L = 200$ μm, $W = 800$ μm).

Discrete transistors fabricated using this simple process showed improved performance. Drain current on/off ratio of around 8 is observed. Field-effect mobility extracted to be $0.036 cm^2/Vs$ from the transfer characteristic in saturation region ($|V_{DS}| > |V_{GS} - V_T|$) of the transistor. Transfer curves also show that the accumulated channel still exists event at zero gate voltage.

3.5. Concluding Remarks

In this chapter, PTFT processing-related issues have been discussed.

A self-aligned PTFT processing sequence, allowing transparent flexible substrates and polymeric gate insulator as developed in this work, has been introduced. With the developed method, we are able to fabricate bottom-gate bottom-contact PTFTs with gate electrode self-aligned to the drain/source electrodes, independent of the organic semiconductor. Self-aligned processing method relies on the backside exposure, therefore minimum channel length transistor that can be fabricated with this method is solely limited by resolution of the exposure equipment.

Following self-aligned process, standard PTFT processing technology has been realized on glass substrate. Polymeric gate insulator and the organic semiconductor exploited are SU-8 2000.5 and rr-P3HT, respectively. Although having a defective gate dielectric, fully patterned PTFTs with interdigitated, corbino and standard layout are fabricated. Two methods for the patterning of the polymeric active layer are proposed. MIMIC is used to obtain P3HT patterns with several micrometer thickness. Lift-off, however, is found to be suitable for the patterning of relatively thin (20 to 100 nm) P3HT films. Moreover, several parasitic leakage mechanisms resulting from defects and non-patterned active layer are discussed next. Leakage currents emanating from the non-patterned active layer are eliminated successfully by P3HT patterning with both MIMIC and lift-off.

A simple method for fabricating discrete transistors with silver epoxy drain/source electrodes is proposed. It appeared that this is actually a relatively fast, yet powerful method which allows various test to be carried on PTFTs easily because of the relatively safer handling and faster electrical connection advantages of discrete transistors.

4. EFFECT OF HEAT AND LIGHT EXPOSURE ON THIN FILM P3HT

4.0.1. Conductivity of P3HT films

Several of the proposed applications of PTFTs involve the exposure of the devices to heat and illumination, either by design or unintentionally. Moreover, thermal and optical exitations of a thin film can provide information about the electronic states within a material. By studying the thermal, electronic and optical properties of individual P3HT thin films, we can provide a more complete picture into the electrical operation of P3HT PTFTs in conjunction with their processing conditions. Therefore, it is important to understand the physical mechanism going on under these circumstances and how these external factors affect the electrical performance of the PTFT.

Silver-P3HT-silver lateral resistor structure is used to gain insight into the temperature and illumination at different wavelengths on the electrical properties of the P3HT film deposited by different methods. Ag electrodes(DuPont Silver Paste 5000) at distance of $100-200$ μm were deposited by a sharp needle on clean microscope slide glass substrates and cured at 150 °C for 30 min in order to eliminate any nonideality that may be caused by the Ag electrodes at during temperature sweep. Subsequently, P3HT thin films of about $100-200$ nm thickness were prepared by drop-casting a chlorobenzene-based solution of rr-P3HT, in an ambient atmosphere. Sample was placed on a hot plate in vacuum chamber. Optical illumination at four different wavelengths was achieved by high-power GaIn LEDs (Helion) placed at 10 cm proximity to the sample.

Electrical conductivity is the primary parameter affected by doping, temperature and light exposure, therefore conductivity variations under respective test conditions are plotted. Conductivity is given by the formula:

$$\sigma = \frac{L}{Wt}\frac{I}{V} \qquad (Scm^{-1}) \tag{4.1}$$

Before the temperature and optical excitation tests, the P3HT film was cured for the desorption of the oxygen found in the film. Conductivity variation during vacuum treatment at 20 mTorr is shown in Figure 4.1. Samples were exposed to air during fabrication steps and therefore the semiconducting polymer layer had a high initial conductivity. Film conductivity decreased from 2.2x10^{-5}(Scm^{-1}) to 0.5x10^{-6}(Scm^{-1}) following an exponential behavior. After about 10 hours of vacuum treatment majority of the oxygen is desorbed and both prolonged vacuum and thermal treatment did not result in a significant conductivity change. So that we conclude the residual dopant concentration is effectively decreased to a minimum level.

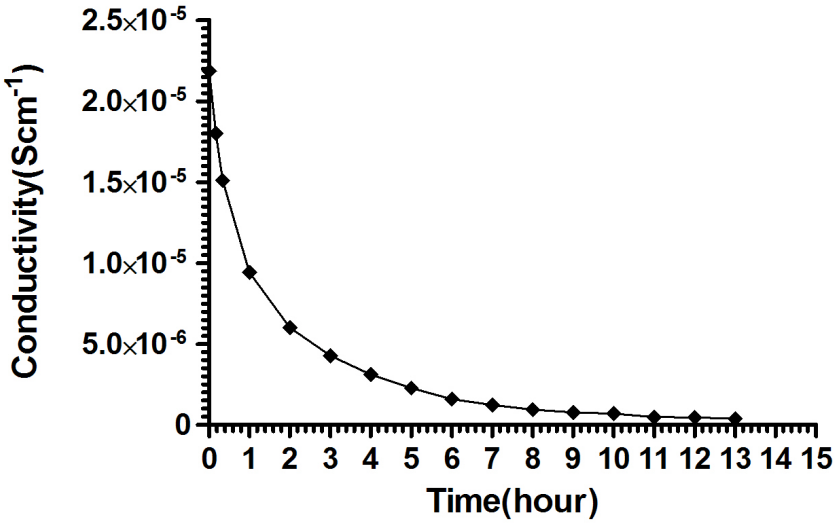


Figure 4.1. Variation of the conductivity with treatment in vacuum.

After the elimination of dopants in the P3HT film and hence their possible effect on film conductivity, the vacuum is ceased and argon gas is led into the chamber until a positive pressure level is reached. Temperature is swept from room temperature(30 °C) to 140 °C and the results are plotted in Figure 4.2. Conductivity is found to exponentially increasing with with temperature. However, after about 140 °C irreversible degradation of the P3HT film is observed.

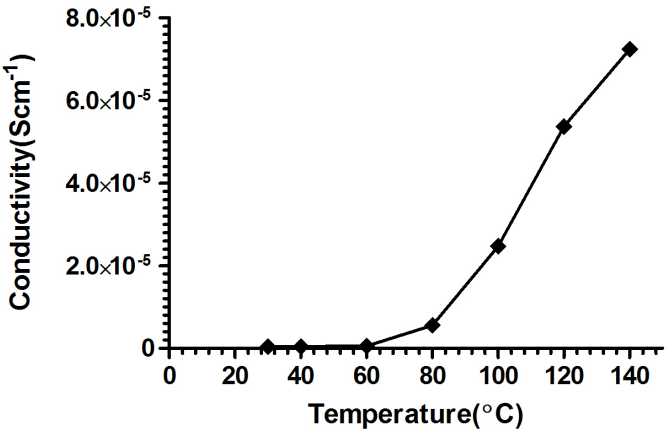


Figure 4.2. Variation of the conductivity with temperature.

The electrical characteristics of P3HT film can be affected by light(photons) if it is absorbed by the organic semiconductor. The photoelectric effects within organic materials, which is not yet fully understood, is often different from what occurs in inorganic semiconductors, because of the strong electron-phonon interactions. One of the main differences is that photo-exitation in those materials does not readily lead to the direct generation of free charge carriers, but to bound electron-hole pairs called excitons. These excitons must be dissociated before the charge can be transported between electrodes. These bound pairs may diffuse to the traps and impurities where they can be separated.

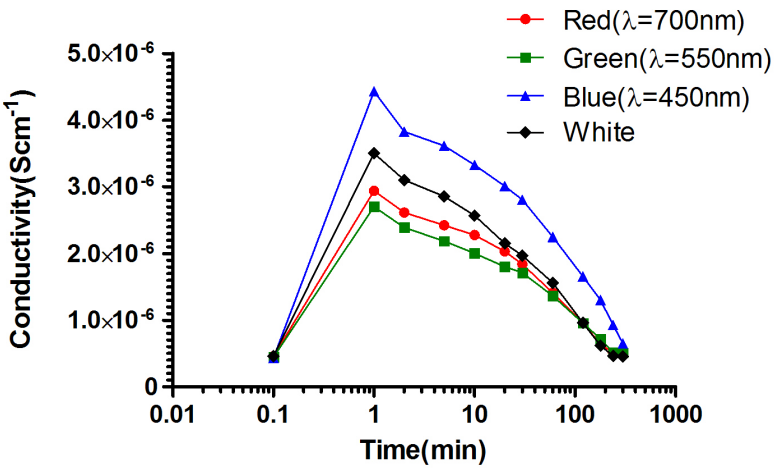


Figure 4.3. Variation of the conductivity with light exposure.

Optical illumination related conductivity test is performed following the temperature sweep test after waiting for the sample to cool down in argon gas environment. Figure 4.3 is the result of the illumination tests. Conductivity increase is known to be directly related to the photo-generated electron-hole pair concentration. Since the P3HT has an optical absorbtion maxima around 550 nm, the largest deviation of conductivity is expected during the green light exposure, however green light resulted in the minimum change in conductivity. Following the green light, red, white and blue light caused the increasing level of variations in conductivity, respectively.

4.1. Concluding Remarks

In this chapter, vacuum, heat and light exposure tests are carried on drop-casted P3HT films. Vacuum treatment is found to be an effective way of de-doping the P3HT film. Heat effect on P3HT film causes conductivity to increase exponentially with temperature. Optical excitation also increases conductivity. Blue light is found to have the major effect on conductivity compared to white, red and green light.

5. CONCLUSIONS

The main focus of this thesis has been to develop simple fabrication techniques and provide a characterization and testing methodology for a through analysis of polymer thin film transistor performance.

In Chapter 2, a number of transistor operation related issues and PTFT characterization has been discussed.

In Chapter 3, we introduced a self-aligned polymer thin film transistor fabrication technique based on back-side exposure on transparent substrates. The developed fabrication method uses lithography, wet etching and metal evaporation, which are common in IC and MEMS fabrications. Furthermore, the smallest achievable self-aligned transistor size is limited to the resolution of lithography. Providing the advantage of the elimination of the critical overlay alignment step, this method allows self-alignment for short-channel devices since the channel length is determined solely by the gate electrode through backside exposure. Therefore, backside exposure self-alignment method will be a viable option for the scaled technologies of polymer electronics in the future. Following the self-aligned fabrication we also investigated the regular fabrication flow for fully-patterned bottom-gate bottom-contact PTFTs. Transistor layouts of different topologies are analyzed and concluded that the layout in which the drain electrode surrounds the source electrode gives the best performance in terms of parasitic leakage current through the semiconducting layer. One technological challenge in PTFT processing that was particularly investigated, is the patterning of the polymeric semiconductor. We employed both micro-molding in capillaries(MIMIC) and lift-off techniques to pattern the P3HT film deposited from solution. MIMIC allows a thicker($3-4\mu$m in our case) layer of P3HT to be patterned whereas lift-off is more suitable for thin film($20-100n$m) of active layer patterning.

We discussed several leakage mechanisms resulting from the un-patterned active layer and showed the improved transistor performance with leakage elimination for each of the proposed active layer patterning methods. A relatively faster and simpler fabrication of discrete PTFTs using silver epoxy based drain and source electrodes are also demonstrated. With this simple method various tests on discrete transistors can be carried on easily and reliably.

In Chapter 4, conductivity variation of P3HT thin film under heat and light exposure is investigated.

5.1. Future Outlook

This thesis has explored different fabrication techniques for polymer thin film transistors, and for integrating these in simple digital circuits. From this point on, basically two paths may be followed in the light of this work:

∗ A possible route that can start from this work is that towards complex digital and analog circuits. The results from Chapter 3 reveals that the challenge that remains is the defect-free deposition and patterning of polymeric layers and hence the uniformity of the transistors. At the same time, a precise PTFT model is required for the simulation of designed circuits.

∗ Another path to be followed could be to exploit discrete PTFTs along with suitable micro devices to work as a sensor system. In this context, one possible option would be to develop a biosensor consisting of array of PTFTs with an integrated polymer microfluidic channel. If successful, this kind of microsystem would lead to a cheap way of analyzing a solution containing an analyte which has an observable effect on the PTFT active layer.

APPENDIX A: TEST LAYOUT

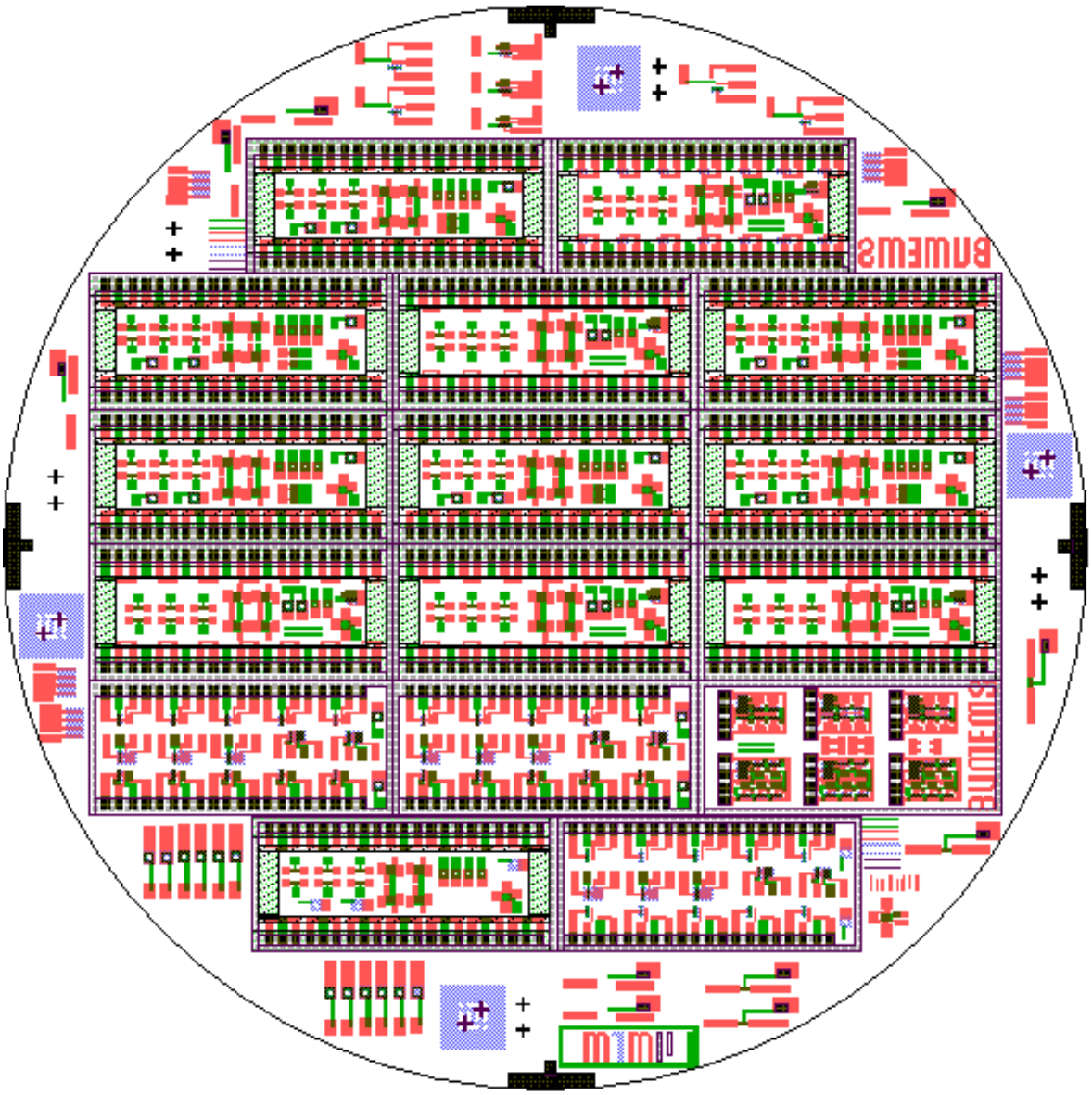


Figure A.1. Test layout containing various transistors, contact chains, Kelvin bridges, capacitors, invertors and ring-oscillators.

REFERENCES

1. Street, R.A. and A. Salleo ,"Contact effects in polymer transistors", *AIP Applied Physics Letters*, Vol. 81(15), pp. 2887, 2002.

2. Kymissis I., C.D. Dimitrakopoulos and S. Purushothaman ,"High-performance bottom electrode organic thin-film transistors", *IEEE Transactions on Electron Devices* , Vol. 48, pp. 1060, 2001.

3. Brazis P.W., D. Gamota , K. Kalyanasundaram and J. Zhang (editors), *Printed Organic and Molecular Electronics*, Kluwer Academic Publishers, 2004.

4. Advanced Information for the Nobel Prize in Chemistry, 2000: "Conductive Polymers", The Royal Swedish Academy of Sciences, 2000.

5. Meijer E.J. and E. Cantatore, "Transistor Operation and Circuit Performance in Organic Electronics", *IEEE Transactions on Electron Devices* , Vol. 48, pp. 1060, 2003.

6. Natali D., L. Fumagalli and M. Sampietro, "Modeling of organic thin film transistors: Effect of contact resistances", *AIP Journal of Applied Physics*, Vol. 101, pp. 014501, 2007.

7. Sheraw C.D., L. Zhou, D.J. Huang, D.J. Gundlach, T.N. Jackson, M.G. Kane, M.S. Hill, J. Campi, B.K. Greening, J. Francl and J. West, "Organic Thin-Film Transistor Driven Polymer Dispersed Liquid Crystal Displays on Flexible Polymeric Substrates", *AIP Applied Physics Letters* , Vol. 80, pp. 1088, 2002.

8. Afzali A., C.D. Dimitrakopoulos and T.L. Breen, "High-Performance, Solution-Processed Organic Thin Film Transistors from a Novel Pentacene Precursor", *Journal of American Chemical Society* , Vol. 124, pp. 8812, 2002.

9. Afzali A., C.R. Kagan and G.P. Traub, "Operational and Environmental Stability of Pentacene Thin-Film Transistors", *AIP Applied Physics Letters*, Vol. 93(8), pp. 1500-1510, 2005.

10. Sirringhaus H., P.J. Brown, R.H.Friend, M.M.Nielsen, K. Bechgaard, B.M.W. Langeveld-Voss, A.J.H. Spiering, R.A.J. Janssen, E.W. Meijer, P. Herwig, D.M. de Leeuw, "Two-Dimensional Charge Transport in Self-Organized, High-Mobility Conjugated Polymers", *Nature* , Vol. 401, pp. 685, 1999.

11. Dickey K.C., J.E. Anthony and Y.L. Loo, "Improving Organic Thin-Film Transistor Performance Through Solvent-Vapor Annealing of Solution-Processable Triethylsilylethynyl Anthradithiophene", *Advanced Materials*, Vol. 18, pp. 1726, 2006.

12. Chang J.F., B. Sun, D.W. Breiby, M.M. Nielsen, T.I. Sölling, M. Giles, I. McCulloch and H. Sirringhaus,"Enhanced Mobility of Poly(3-hexylthiophene) Transistors by Spin-Coating from High-Boiling-Point Solvents", *Chemistry of Materials* , Vol. 16, pp. 4772, 2004.

13. Kline R.J., M.D. McGehee, E.N. Kadnikova, J. Liu, J.M.J. Frechet and M.F. Toney, "The Dependence of Regioregular Poly(3-hexylthiophene) Film Morphology and Field-Effect Mobility on Molecular Weight", *Macromolecules*, Vol. 38, pp. 3312, 2005.

14. De Boer R.W.I., M.E. Gershenson, A.F. Morpurgo and V. Podzorov, "Organic Single-Crystal Field-Effect Transistors", *Physica Status Solidi (a)*, Vol. 201(6), pp. 1302, 2004.

15. Butko V.Y., X. Chi, D.V. Lang and A.P. Ramirez, "Field-Effect Transistor on Pentacene Single Crystal", *AIP Applied Physics Letters*, Vol. 83, pp. 4773, 2003.

16. Butko V.Y., X. Chi and A.P. Ramirez, "Free-Standing Tetracene Single Crystal Field Effect Transistor", *Solid State Commun.*, Vol. 128, pp. 431, 2003.

17. Podzorov V., Pudalov V. M., and Gershenson M. E., "Field-Effect Transistors on Rubrene Single Crystals with Parylene Gate Insulator", *AIP Applied Physics Letters*, Vol. 82, pp. 1739, 2003.

18. Menard E., V. Podzorov, S.H. Hur, A. Gaur, M.E. Gershenson and J.A. Rogers, "High-Performance n and p-type Single-Crystal Organic Transistors with Free-Space Gate Dielectrics", *Advanced Materials*, Vol. 16, pp. 2097, 2004.

19. Anthopoulos T.D., C. Tanase, S. Setayesh, E. Meijer, J.C. Hummelen, P.W.M. Blom and D.M. de Leeuw, "Ambipolar Organic Field-Effect Transistors Based on a Solution-Processed Methanofullerene", *Advanced Materials*, Vol. 16, pp. 2174, 2004.

20. Waldauf C., P. Schillinsky, M. Perisutti, J. Hauch and C.J. Brabec, "Solution-Processed Organic n-Type Thin-Film Transistors", *Advanced Materials*, Vol. 15, pp. 2084, 2003.

21. Anthopoulos T.D., D.M. de Leeuw, E. Cantatore, P. van Hof, J. Alma and J.C. Hummelen, "Solution Processible Organic Transistors and Circuits Based on a C70 Methanofullerene", *AIP Journal of Applied Physics*, Vol. 98, pp. 54503, 2005.

22. Chikamatsu M., S. Nagamatsu, Y. Yoshida and K. Kikuchi, "Solution-Processed n-Type Organic Thin-Film Transistors with High Field-Effect Mobility", *AIP Applied Physics Letters*, Vol. 87, pp. 203504, 2005.

23. Sakamoto Y., T. Suzuki, M. Kobayashi, Y. Gao, Y. Fukai, Y. Inoue, F. Sato and S. Tokito, "Perfluoropentacene: High-Performance p-n Junctions and Complementary Circuits with Pentacene", *Journal of American Chemical Society*, Vol. 126, pp. 8140, 2004.

24. Ando S., J. Nishida, H. Tada, Y. Inoue, S. Tokito and Y. Yamashita, "n-Type Organic Field-Effect Transistors with Very High Electron Mobility Based on Thiazole Oligomers with Trifluoromethylphenyl Groups", *Journal of American Chemical Society*, Vol. 127, pp. 5336, 2005.

25. Facchetti A., M. Mushrush, M.H. Yoon, G.R. Hutchison, M.A. Ratner and T.J. Marks, "Building Blocks for n-Type Molecular and Polymeric Electronics", *Journal of American Chemical Society*, Vol. 126, pp. 13874, 2004.

26. Ohnuki H., K. Ikegami, T. Ida and M. Izumi, "Field-Effect Transistors Using LangmuirBlodgett Films of Neutral Long-Chain TCNQ", *Colloids and Surfaces*, Vol. 257-258, pp. 381, 2005.

27. Meixner R.M, H.H. Gobel , H. Qiu, C. Ucurum, W. Klix, R. Stenzel, F.A. Yildirim, W. Bauhofer and W. Krautscneider, "A Physical Based PSPICE Compact Model for Poly(3-Hexylthiophene) Organic Field-Effect Transistors", *IEEE Transactions on Electron Devices* , Vol. 55(7), pp. 9383, 2008.

28. Sönmez A.O., "Flexible Polymer Display Technologies", M.S. Thesis, Boğaziçi University, 2007.

29. Madou M., *Fundamentals of Microfabrication: The Science of Miniaturization* , CRC Press, Boca Raton, 2002.

30. Gundlach D.J., L. Zhou, J.A. Nichols, T.N. Jackson, P.V. Necliudov, M.S. Shur ,"An Experimental Study of Contact Effects in Organic Thin Film Transistors" *AIP Journal of Applied Physics*, Vol. 100(024509), 2006.

31. Cantatore E., T.C.T. Geuns, G.H. Gelinck, E. van Veenendaal, A.F.A. Gruijhuijsen, L. Schrijenemakers, S. Drews, D.M de Leeuw, "A 13.56 MHz RFID System Based on Organic Transponders", *IEEE Journal of Solid-State Circuits*, Vol.42(1), 2007.

32. Jain *et al.*, "Flexible Electronics and Displays :High Resolution: Roll-to-Roll, Projection Lithography and Photoablation Processing Technologies for High Throughput Production", *Proceedings of the IEEE*, Vol. 93(8), pp. 1500-1510, 2005.

33. Laker K.R., W.M.C. Sansen, "Design of Analog Integrated Circuits and Systems", McGraw-Hill, 1994.

34. Bao Z., J. Jocklin, "Organic Field-Effect Transistors", CRC Press, pp.501-503, 2007.

35. Li *et al.*, "Polymer Thin Film Transistors with Self-Aligned Gates Fabricated Using Ink-Jet Printing", *AIP Applied Physics Letters*, Vol. 90(17), pp. 172103-1-3, 2007.

36. Stutzmann *et al.*, "Self-Aligned, Verticle Channel, Polymer Field Effect Transistors", *Science* , Vol. 299(5614), pp. 1881-1884, 2003.

37. Kawase *et al.*, "Inkjet Printing of Polymer Thin-Film Transistors", *Thin Solid Films*, Vol.438-439, pp. 279-87, 2003.

38. Thomasson B.D. , T.N. Jackson, "Fully Self-Aligned Tri-Layer a-Si:H Thin-Film Transistors with Deposited Doped Contact Layer", *IEEE Electron Device Letters*, Vol. 19(4), pp. 124-126, 1998.

39. Cheng *et al.*, "Self-Aligned Amorphous -Silicon TFTs on Clear Plastic Substrates", *IEEE Electron Device Letters*, Vol. 27(3), pp. 166-168, 2006.

40. Datasheet retrieved from *http* : *//www.microchem.com.*

41. Jiguet *et al.*, "SU-8 Nanocomposite Photoresist with Low Stress Properties for Microfabrication Applications", *Microelectronic Engineering*, Vol. 83(3), 2006.

42. Mata *et al.*, "Fabrication of Multi-Layer Su-8 Microstructures" , *IEEE Electron Device Letters*, Vol. 27(3), pp. 166-168, 2006.

43. Keller *et al.*, "Processing of Thin SU-8 films", *Journal of Micromechanics and Microengineering*, Vol. 18, 125020 2008.

44. Salleo A. and M. L. Chabinyc, "Organic Electronics: Materials, Manufacturing and Applications", Wiley-VCH, Weinheim, pp. 108-129, 2006.

45. Meijer *et al.*, " Dopant Density Determination in Disordered Organic Field-Effect Transistors", *AIP Journal of Applied Physics*, Vol. 93, pp. 4831, 2003.

46. Backlund *et al.*, "Operating Principle of Polymer Insulator Organic Thin-Film Transistors Exposed to Moisture", *AIP Journal of Applied Physics* Vol.98, pp. 074504, 2005.

47. Rep *et al.*, "Doping dependent charge injection into regioregular poly(3-hexylthiophene)", *Organic Electronics*, Vol. 4 ,pp. 201-207, 2003.

48. Jain A.C., M. Willander, V. Kumar, "Conducting Organic Materials and Devices", *Semiconductors and Semimetals* Vol. 81, pp. 131 Elsevier, 2007.

49. Bao Z., A. Dodabalapur and A. J. Lovinger, "Soluble and Processable Regioregular poly(3-hexylthiophene) for Thin Film Field-Effect Transistor Applications with High Mobility", *AIP Applied Physics Letters* Vol. 69, pp. 4108, 1996.

50. Verilhac J.M., G. LeBlevennec, D. Djurado, F. Rieutord, M. Chouiki, J.P. Travers, A. Pron, "Effect of Macromolecular Parameters and Processing Conditions on Supramolecular Organisation, Morphology and Electrical Transport Properties in Thin Layers of Regioregular poly(3-hexylthiophene)", *Synthetic Metals* Vol. 156, pp. 815-823, 2006.

51. Brown A.R., C.P. Jarret , D.M. de Leeuw , M. Matters, "Field-Effect Transistors Made from Solution-Processed Organic Semiconductors" *Synthetic Metals* Vol. 88, pp. 37-55, 1997.

52. Huitama H.E.A., G.H. Gelinck, J.B.P.H van der Putten, K.E. Kuijk, K.M. Hart, E. Cantatore, D.M. de Leeuw, "Active-Matrix Displays Driven by Solution Processed Polymeric Transistors" *Advanced Materials* Vol. 14(17), pp. 1201-1204, 2002.

53. Klauk H., D.J. Gundlach, J.A. Nichols and T.N. Jackson, "Pentacene Organic Thin-Film Transistors for Circuit and Display Applications", *IEEE Transactions on Electron Devices* Vol.46(6), pp. 1258-1263, 1999.

54. Kim E., Y. Xia, G.M. Whitesides, "Micromolding in capillaries:Applications in material science", *J. Am. Chem. Soc.* Vol. 118, pp. 5722, 1996.

55. Xia Y., E.Kim and G.M. Whitesides, "Micromolding of polymers in capillaries:Applications in microfabrication", *Chem. Mater.* Vol. 8, pp. 1558, 1996.

56. Rogers J.A., Z. Bao and V.R. Raju, "Nonphotolithographic Fabrication of Organic Transistors with Micron Feature Sizes" *App. Phys. Lett.* Vol. 72, pp. 2716, 1998.

57. Beh W.S., I.T. Kim , D. Qin, Y. Xia and G.M. Whitesides, "Formation of Patterned Microstructures of Conducting Polymers by Soft Lithography and Applications in Microelectronic Device Fabrication", *Advanced Materials* Vol.11(12), pp. 1038, 1999.

58. Halik *et al.*, "Polymer Gate Dielectric and Conducting Polymer Contacts for High Performance Organic Thin-Film Transistors", *Advanced Materials* Vol.14, pp. 1717, 2002.

59. Halverson *et al.*, "The Mechanism of Single-Step Liftoff with Chlorobenzene in a Diazo-Type Resist", *IBM J. Res. Develop* Vol. 26(5), pp. 590, 1982.