MICROPROCESSOR CONTROLLED single phase to single phase CYCLOCONVERTER

by

M. SERDAR BAŞ

Submitted to the faculty of the school of engineering in partial fulfillment of the requirements for the degree of MASTER OF SCIENCE in ELECTRICAL ENGINEERING

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TABLE OF CONTENTS

ACKNOWLEDGEMENT

This thesis has been prepared for the partial fulfillment of the requirement of Bosphorus University, School of Engineering, for the degree of Master of Science.

I wish to express my gratitude and sincere thanks to Dr. Okyay Kaynak, my thesis supervisor, for his kind interest and guidance in the accomplishment of this work; to Ender Erdem for his encouragement and support.

ABSTRACT

The object of this thesis is to design and construct a microprocessor-controlled cycloconverter. The microprocessor is used to generate the gating signals for a single phase to single phase cycloconverter, the thyristors of which are triggered according to a policy in order to minimize the harmonics of the output current ("optimum firing scheme") for a particular output voltage and frequency. The software for the microprocessor and the hardware for the interface are developed.

For the realization of the optimum firing scheme a different approach from those in published literature is adopted in this thesis in the sense that no attempt is made to replace all the functions of the conventional control circuitry by the microprocessor, but rather an economical and simple design is tried to be arrived at by combining the advantages of both.

ÖZET

Bu tez çalışmasında mikroişleyici kontrollu frekans dönüştürücüsünün tasarımı ve yapımı gerçekleştirilmiştir. Bu kontrolde belli bir yük voltajı ve frekansı için tristörlerin akımda meydana gelecek harmoniklerin tesirini minimuma indiren bir politikayla tetiklenmesi esas tutulmuştur. Bunun için gerekli devre hazırlanmış, mikroişleyici programı geliştirilmiştir.

Bu tezde yeni bir metod kullanılmıştır; şöyle ki ne alışılagelmiş kontrol devrelerine ne de mikroişleyici ile kontrole tamamen bağlı kalınmış, ancak her ikisi de birleştirilerek kullanılmıştır.

INTRODUCTION

The solid-state cycloconverter is an important power converter performing useful direct frequency changing, but its application has so far been limited to specialised areas mainly because of the complexity of its power and control circuits.

The cycloconverter is an assembly of SCR's in which a set of low fequency 3-phase voltages is synthesized from portions of a set of line frequency, 3 phase voltages. It is necessary to control the phase of the thyristor firing pulses by a considerably complicated manner to obtain the desired sinusoidal output voltage. In the family of power conditioning systems the cycloconverter has probably the most complex control circuit requirements. In this respect it is here that the microprocessors are most likely to replace the hardwired logic systems.

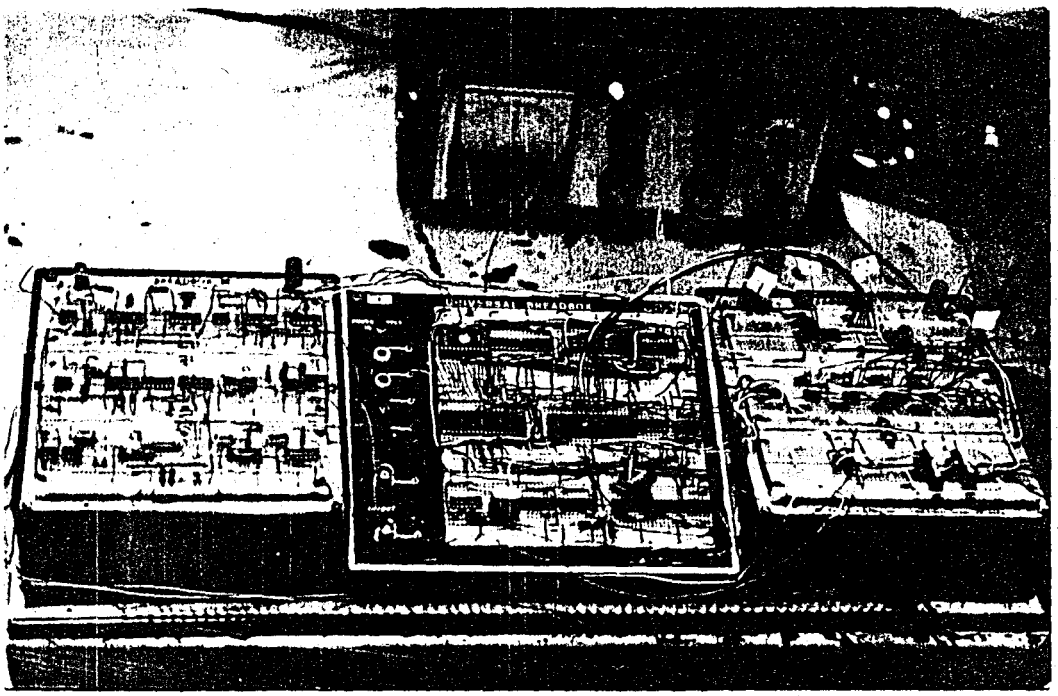
As this work was very preliminary and in order to keep the problem within manageable limits it was decided to use a single phase to single phase cycloconverter.

Before deciding on the method to be used for this work, a thorough search of papers already published was

carried out: There are only five papers related to this subject dating from August 1977. Namely, this is about when the micro-processors are started to be used in dedicated applications.

Since their inception, digital computers have continuously become more efficient, expanding into new applications with each major technological improvement. The advent of minicomputers enabled the inclusion of digital computers as a permanent part of various process control systems. Unfortunately, the size and cost of minicomputers has limited their use in dedicated applications. Nowadays the system designer has a new alternative: Microcomputer.

In chapter I, a brief summary of the principles of cycloconverters and various cycloconverter arrangements are given. Chapter II introduces works on microcomputer controlled cycloconverters -from August 1977 until now- their method of control and the results. Chapter III introduces the method used in this thesis, explaining the hardware and interface circuits, as well as the flowchart of the program used. In the last chapter, the experimental results are given under loads with different power factors. With the experience gained during the course of this project remarks are made for further work on this subject.



Experimental set-up of the single phase to single phase cycloconverter control circuitry using Z-80 based micro-computer

CHAPTER I

PRINCIPLES OF CYCLOCONVERTERS

I.1 CYCLOCONVERTER ARRANGEMENTS (R,7)

The cycloconverter transforms a high-frequency supply to a low frequency supply without the need to have an intermediary d.c. supply. Cycloconverters can be used for any low-frequency application, variable or fixed.

Cycloconverter is basically a combination of various groups of thyristor converters (Figure 1.1). The load-voltage waveforms are shown for converter delay angles varying from 0° to 180°.

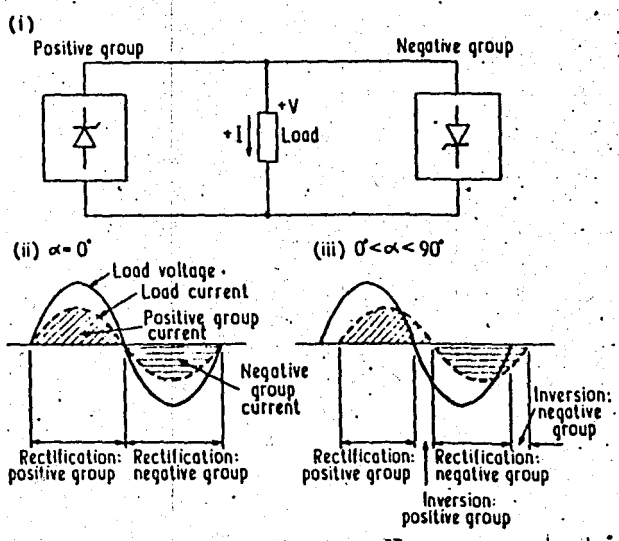


Figure 1.1 Group Representation of a cycloconverter

The function of the two converters is seen to change from full rectification to full inversion, in varying stages. It is clear that each converter must therefore be able to rectify and regenerate within any half cycle. Since only one converter carries the load current at any instant, it is possible to fire only this system when required. However, there are often advantages to firing both converters simultaneously, but with their delay angles such that their sum always equals 180°.

Figure 1.2 shows a circuit made up from two push-pull converters*. Push-pull systems use half as many thyristors as a bridge circuit, but these have to be rated at twice the load voltage.

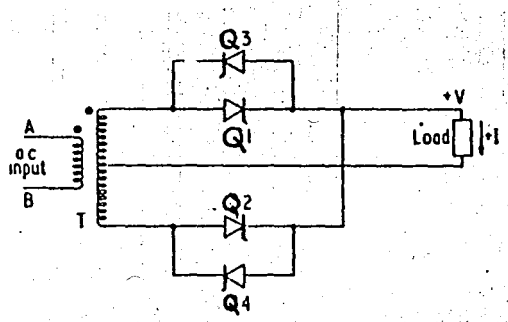


Figure 1.2 Push-pull two pulse cycloconverter

The higher the pulse number of the converter the lower the load ripple voltage (and also the harmonics). To help to keep the harmonics low, a polyphase supply is used.

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*push-pull circuit: A circuit containing two like elements which operate in 180° phase relation to produce additive output components of the desired wave and cancellation of certain unwanted products.

Therefore single-phase cycloconverters are rarely used in practice.

Figure 1.3 shows a 3-pulse push-pull cycloconverter circuit which is supplying a balanced 3-phase load. To obtain a single-phase output only one converter may be used and the load returned to the neutral point of the transformer secondary. The 3-pulse circuit can be extended to six pulses either by using a double-star transformer secondary or by an interphase transformer connection. This latter system is given in Fig. 1.4 where only one phase of the converter is shown in detail. If a single-phase output is required, only one converter is used and the load output is returned to the transformer neutral point.

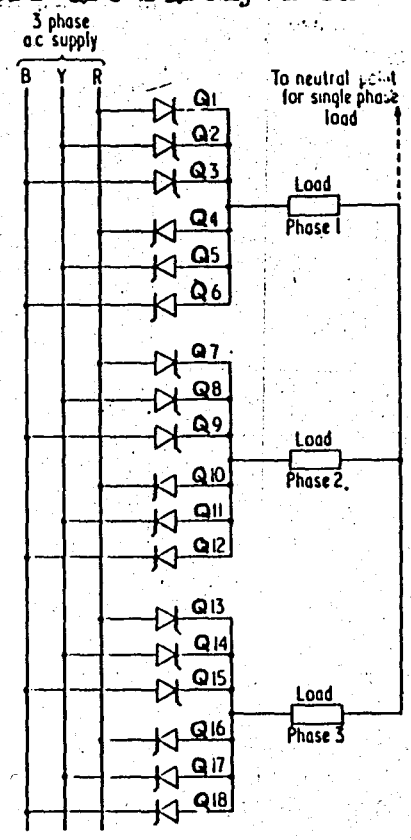


Figure 1.3 Push-pull three pulse cycloconverter

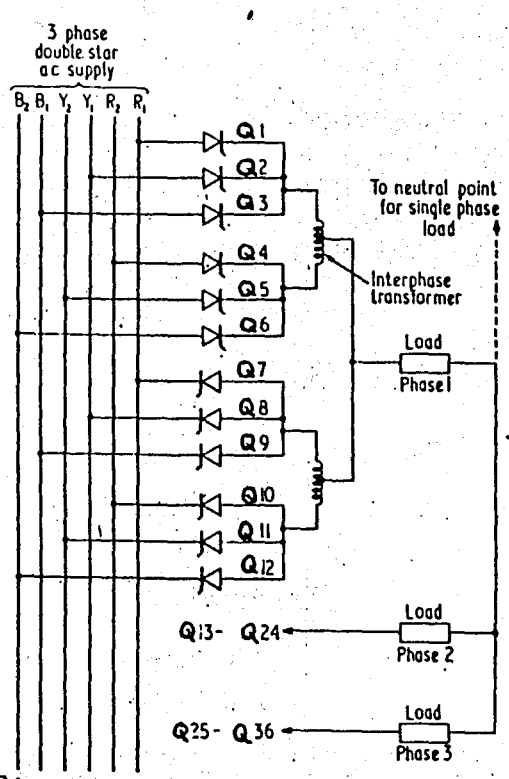


Figure 1.4 Push-pull six pulse cycloconverter

The circuits described so far can be referred to a symmetrical cyclo-converters since each phase of a three-phase output is made up from a single-phase unit.

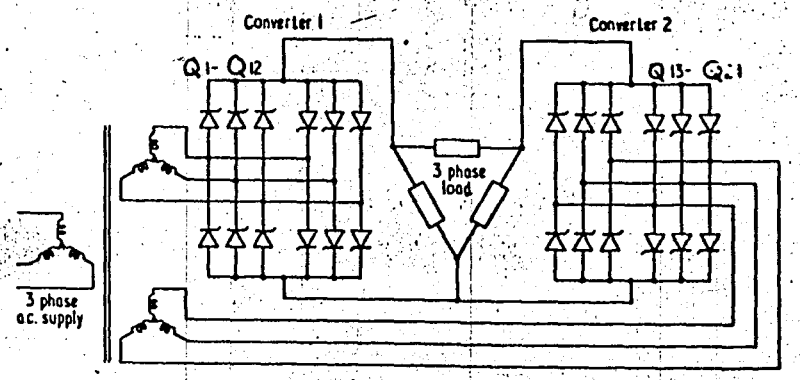


Figure 1.5 Bridge six pulse, two converter cycloconverter

This is not always necessary. For instance, figure 1.5 shows a three-phase load supplied from an asymmetrical cyclo-converter which has only two single-phase modules. It is now difficult to maintain a balanced supply to the three-phase load. In spite of this, however, this system is often economical to use in low-power circuits where good performance is not needed.

I.1.1 ENVELOPE CYCLOCONVERTERS:

In discussions so far the operation of a cycloconverter has been illustrated with reference to its phase-control mode . This is the most common technique and gives a system in which the load voltage and frequency can be readily controlled. However, in certain applications, especially where the ratio of input to output frequency is fixed, envelope converters can prove simpler and more economical.

Figure 1.6(i) shows the output from a single-phase supply in which the ratio of input to output frequency is three. The converter thyristors are operated at the beginning of every half cycle, so that they follow the envelope of the a.c. supply waveform. Voltage control is now obtained by a correct choice between primary and secondary ratios on the input transformer. Clearly the load voltage has a very high harmonic content. This can be reduced as in figure 1.6(ii) by using a 6-pulse cycloconverter. Once again the load voltage follows the envelope of the various phase voltages and the output voltage is almost rectangular in shape. Since most cycloconverters have an input transformer it is possible to vary the ratio of their secondaries with respect to one another. For instance, figure 1.7 shows the output voltage obtained from a system in which phase 1 has 33% , phases 2 and 6 have 73%, and phases 3 and 5 have 93% of the voltage of that of phase 4. The operation is once again of the envelope type where the load voltage commutates naturally from phase to phase, so that it is always equal to that of the most positive phase.

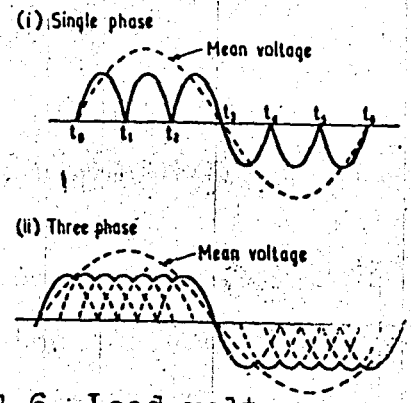


Figure 1.6 Load voltage waveforms from synchronous envelope cycloconverters

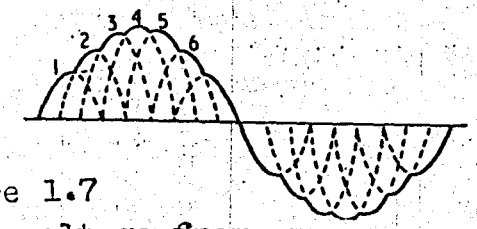


Figure 1.7
Output voltage from an alternative form of synchronous envelope cycloconverter

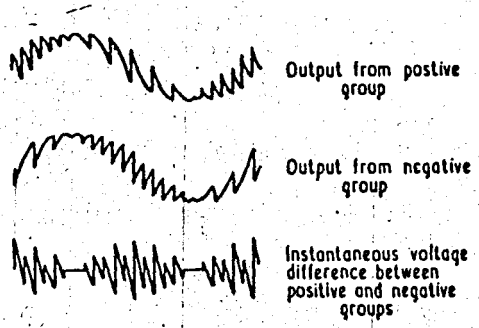
Envelope converters are of course incapable of variable frequency operation. Furthermore, since the converter thyristors operate like diodes during any half cycle, they cannot regenerate back load current to the supply. Therefore envelope cyclo-converters are incapable of handling inductive loads since they cannot absorb any reactive power. For stable operation it is necassary to connect a capacitor in parallel across the load, so as to raise its overall power factor. This disadvantage is, of course, not met with phase-controlled converters, in which the firing angle can be shifted readily to meet any required direction of load-current flow.

I.1.2 PHASE-CONTROLLED CYCLOCONVERTERS

The load frequency can be controlled by the frequency of the oscillations of the firing point about 90°. Each phase of the cycloconverter is made up of basic single-phase converter bloks and by adjusting the firing angles of positive (α_p) and negative (α_n) systems so that $\alpha_p + \alpha_n$ is always equal to 180°, the mean output voltage from the two groups is equal so that there is no net transfer of power round the two converters.

Figure 1.8

Instantaneous voltage difference between positive and negative groups of a cycloconverter



However, figure 18 shows that even though the mean outputs from the two converters are equal, there are instantaneous voltage differences which can give rise to a large circulating current around the loop, unless this is limited by series reactors. The flow of circulating current can of course be suppressed totally by ensuring that only one converter conducts at any time. This is by far the most satisfactory arrangement since the circulating currents can often become exremely large. It does, however, result in a much more complex thyristor control system in which the load current must be sensed and used to block one or other group of converter, depending on the current direction. Another disadvantage of the non-circulating current mode is that the load voltage distortions can become much higher on light loads when the current becomes discontinuous. The one disadvantage of circulating current operation is the rather large current flow between the two converter groups, which results in increased device rating and reduced efficiency.

Non-circulating current converters prevent this by blocking one of the converters at all times so that there can be no interchange of power between the two groups. The price to be paid is greater circuit complexity and higher load voltage harmonics, although this is only important when the ratio of input to output frequency is low.

Other factors affect the load harmonics as well. These are directly dependent on the pulse number of the converter, the ratio of input to output frequency, the level of the output voltage, the load power factor and the technique used to control the load voltage.

I.1.3 STEP-UP CYCLOCONVERTERS

The usual form of operation for a cycloconverter is in the step-down mode, where the output frequency is less than that of the input. When the cycloconverter is running in its step-down mode it is naturally commutated. The leading kVA required to turn-off conducting thyristors is derived from the higher frequency side, which in this case is the a.c. supply. There is of course, no reason why a cycloconverter cannot run with an output frequency greater than that of the input. It is now called step-up cycloconverter or cyclo-inverter. In this instance the turn-off energy required by the conducting thyristors must again be derived from the high-frequency side i.e. the load. If the load has a leading power factor then the requirement will be met. If not then a capacitor must be connected across it to reproduce this condition artificially.

I.2 OPERATIONAL ASPECTS OF CYCLOCONVERTERS (R,5)

I.2.1 SINGLE PHASE TO SINGLE PHASE CYCLOCONVERTER

As already explained, cycloconverters employ line commutation to provide an alternating output voltage of angular frequency w_o from an alternating voltage source of greater angular frequency w_s. In the case of single phase to single phase cycloconverter (shown in figure 1.9)

$$w_s \geq 9\, w_o \quad \text{rad/sec} \qquad 1.1$$

The transformer in figure 1.9(a) may be replaced in the circuit by the two voltage sources of (b), and this may be rearranged to give the equivalent circuit of (c).

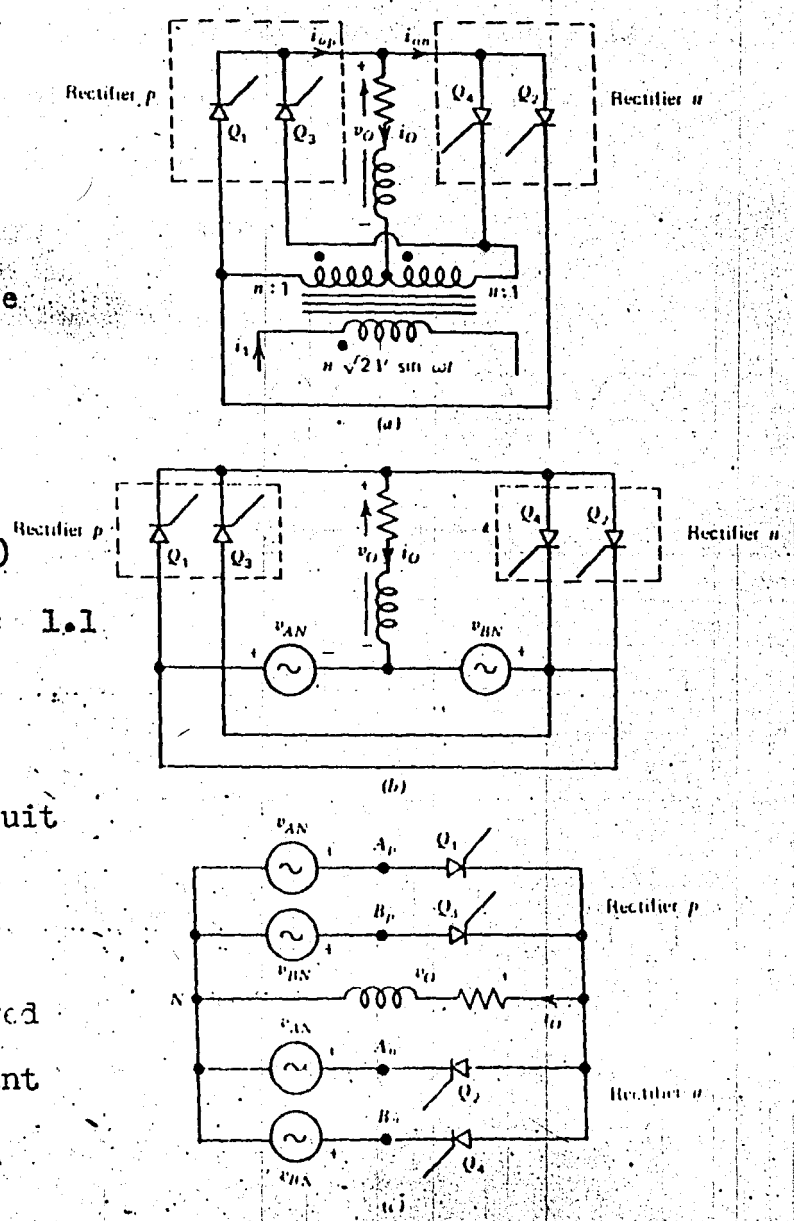


Figure 1.9 Single phase to single phase cycloconverter

I.2.1a OPERATION WITH DISCONTINUOUS-OUTPUT CURRENT

The cycloconverter can operate with continuous or discontinuous output current. In the ac load circuit of figure 1.9(c), there is no source of emf, and discontinuous current operation will ensue if the initial current is zero, and

$$\phi \leq \pi \leq \pi \quad \text{rad} \qquad 1.2$$

where $\tan\phi = w_s L/R$ rad 1.3

Figure 1.10 shows two blanking signals P and N. Only, if signal P is applied do the gating signals to rectifier P appear. Conversely, only if signal N is

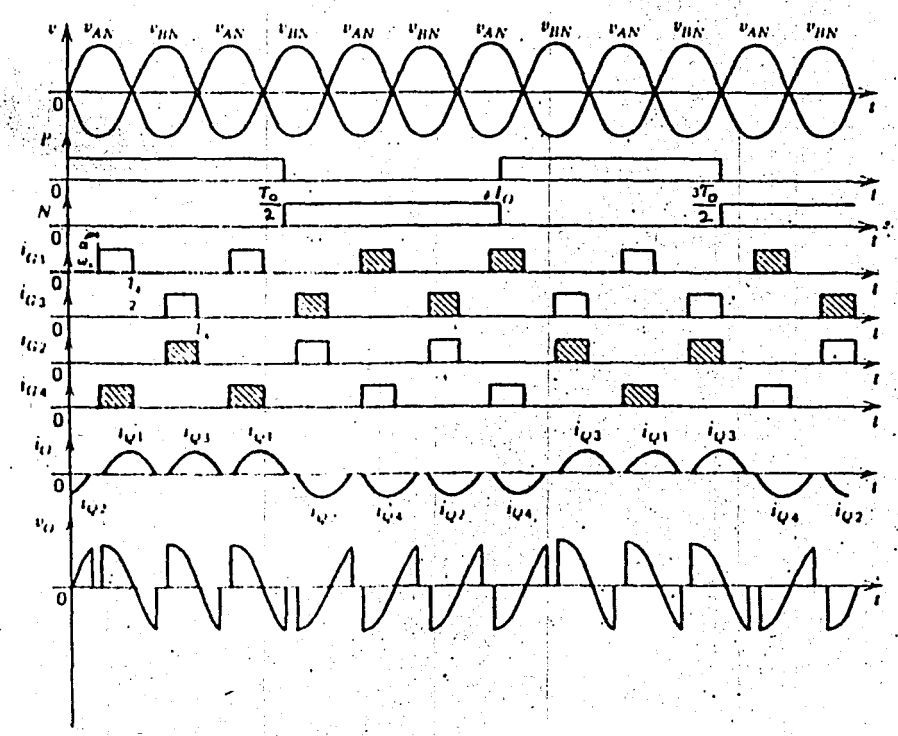


Figure 1.10 Discontinuous current operation of fig.1.9

applied do the gating signals to rectifier N appear. Omitted gating signals are shown shaded in the figure. The output frequency of the cycloconverter is thus established by the frequency of the blanking signals of periodic time T_o and duration $T_o/2$ sec.

The waveforms of i_o and V_o shown in figure 1.10 are very far from sinusoidal; however, it can be seen that the periodic time of the fundamental component of each will be T_o. It will also be noted that the two "half waves" of the current and voltage are not identical.

In the negative half wave there are 4 pulses of current, whereas in each of the positive half waves illustrated, there are only three. Clearly a waveform such as this has a negative direct component of current. However, if the time axis were sufficiently extended, it would be found that after the completion of a few cycles of the output variables, this situation would be reversed, with 4 positive pulses of output current alternating with only 3 negative pulses. Such a waveform would have a positive direct component of current. This "alternating direct component" in fact forms a subharmonic component of the output variables and it is to restrict the amplitude of this subharmonic that the constraint of inequality 1.1 is imposed.

Operation with discontinuous output current in RL load circuits necessarily implies operation at low amplitudes of fundamental components of current and voltage; that is the converter is operating at low output power.

.2.1b OPERATION WITH CONTINUOUS OUTPUT CURRENT

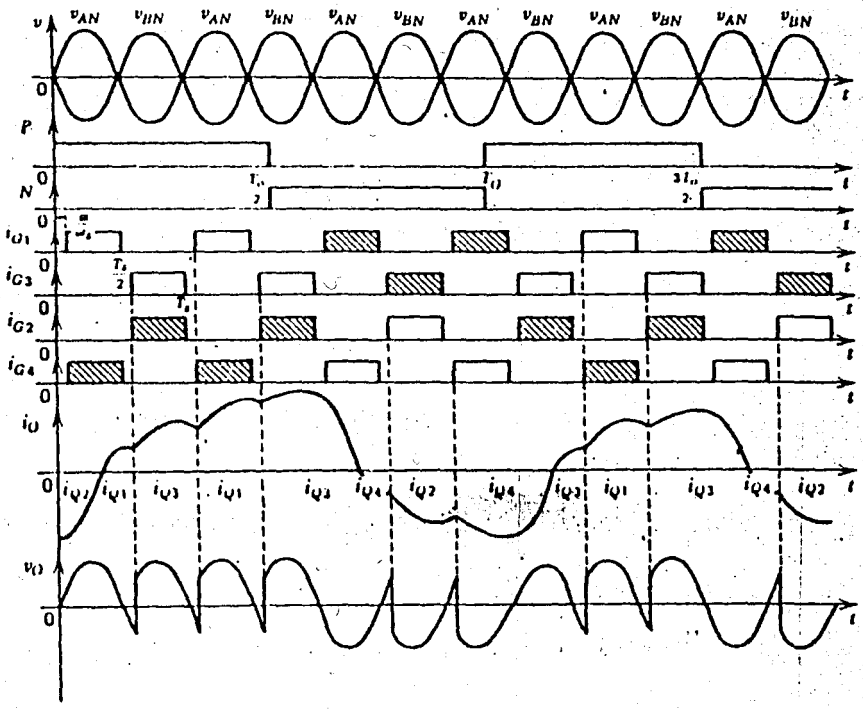


Figure 1.11 Continuous current operation of fig.1.9

Figure 1.11 shows the waveforms for the operation of the cycloconverter with continuous output current. This is the case when the initial current is zero and

$$0 \leq \pounds < \phi \quad \text{rad} \qquad 1.4$$

Continuous output current implies operation at high amplitudes of fundamental components of current and voltage waveforms; that is, the converter is operating at high output power. The maximum power output is achieved when $\alpha = 0$.

From the point of view of output harmonic content, continuous current output may appear from Figures 1.10 & 1.11 to be something of an improvement over discontinuous current. However, the real solution to the problem of harmonics lies in varying the delay angle α throughout each half cycle of the output waveforms and the manner in which this is done is the subject of the following section.

2.1c REDUCTION OF OUTPUT HARMONICS

In cycloconverters operating with continuously variable output frequency, it is often important to reduce the harmonics in the output current at low frequency (e.g. to reduce torque pulsations in ac drives). If the cycloconverter were able to provide a purely sinusoidal output voltage waveform, then a purely sinusoidal current would flow in any linear load circuit. However, the output voltage waveform is necessarily made up of segments of the source voltage waveforms. Nevertheles it is possible to arrange that these segments shall be

such as to produce the minimum current harmonics, so giving a close approximation to a sinusoidal output current. The following discussion of how this is achieved deals with the continuous current operating condition, since this is the important and common situation.

Since it is desired that the waveform of the actual output voltage shall be such as to produce as nearly as possible the effect of a sinusoidal output voltage the delay angle at which each thyristor in the rectifiers is turned on is controlled with reference to an ideal output voltage wave that may be defined as

$$v_o^* = \sqrt{2} \cdot V^* \sin w_o t \quad \text{volts} \qquad 1.5$$

The source voltages in figure 9 may be defined as

$$v_{AN} = \sqrt{2} \cdot V \cdot \sin w_s t \quad \text{volts} \qquad 1.6$$

$$v_{BN} = -\sqrt{2} \cdot V \cdot \sin w_s t \quad \text{volts} \qquad 1.7$$

In figure 12, one cycle of v_o^* is shown. A second curve is also shown in broken line representing the ideal output current i_o^* produced by v_o^* in a load circuit with a leading power factor. For the first part of the cycle both v_o^* and i_o^* are positive, and rectifier P is operating as a rectifier.

For any instant during the cycle of v_o^* there is a corresponding delay angle £ which, if applied continuously to the thyristors of the rectifier delivering current,

would give an average output voltage equal to the value of v_o at that instant. It can easily be shown that the necessary angle $\pounds$ is given by

$$v_o^* = \frac{2\sqrt{2}\,V}{\pi} \cos \pounds \quad \text{volts} \qquad 1.8$$

where $\pounds = w_s t - 2n\pi$ rad 1.9

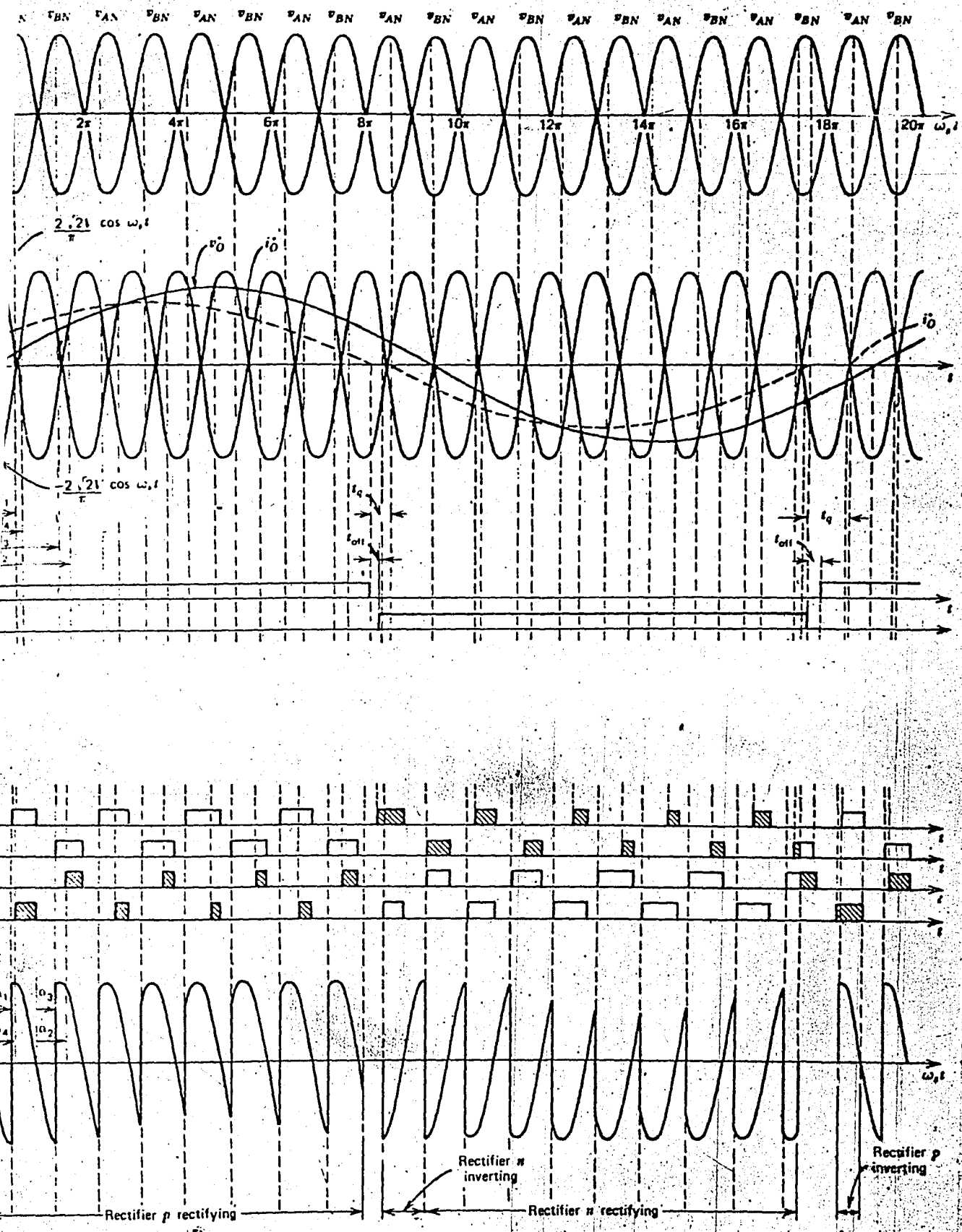
In equation 1.9 , n is an integer giving the number of complete cycles of source voltage that have elapsed since t = 0. To achieve an output voltage that will have the desired effect, it is therefore necessary to arrange that during the first cycle of source voltage thyristor Q_1 in figure 1.9 is turned on at instant t_1, when

$$v_{o1}^* = \frac{2\sqrt{2}\cdot V}{\pi} \cos w_s t_1 \qquad 1.10$$

A curve of the function $(2\sqrt{2}\cdot V/\pi)\cos w_s t$ is shown in figure 1.12. The first intersection of this curve with that of v_o defines the instant t_1 which satisfies equation 1.10 and determines the value of $\pounds_1$, the delay angle at which gating signal i_{G1} commences. The gating signal is shown in figure 1.12. Thyristor Q_1 is turned on at $w_s t_1 = \pounds_1$, so that voltage v_{AN} appears across the load circuit, and the succeeding segment of the wave of output voltage v_o is described by equation 1.6 This output voltage wave also is shown in figure 1.12. Necessarily

$$0 < w_s t_1 < \pi \quad \text{rad} \qquad 1.11$$

At instant t_3 , thyristor Q_3 must be turned on and the



e 1.12 Reduction of output harmonics- Determination of $\mathcal{L}$ ($w_s = 9.5w_o$)

desired output voltage is

$$v_{o3}^{*} = \frac{2\sqrt{2}\cdot V}{\pi} \cos \pounds_3 \quad \text{volts} \qquad 1.12$$

If $\pounds_3$ is the delay angle of thyristor Q_3 measured from the instant of commencement of the positive half cycle of voltage v_{BN} , then

$$w_s t_3 = \pounds_3 + \pi \quad \text{rad} \qquad 1.13$$

and

$$v_{o3}^{*} = \frac{2\sqrt{2}\,V}{\pi} \cos(w_s t_3 - \pi)$$

$$= -\frac{2\sqrt{2}\cdot V}{\pi} \cos w_s t_3$$

A curve of $-(2\sqrt{2}\cdot V/\pi) \cos w_s t$ is also shown in figure 1.12. From equation 1.13 , necessarily

$$\pi < w_s t_3 < 2\pi \quad \text{rad} \qquad 1.15$$

Thus the first intersection of the curve v_o with that of $-(2\sqrt{2}\cdot V/\pi)\cos w_s t$ within the range specified in inequality 1.15 defines the instant t_3 that satisfies equation 1.14 and determines the value of $\pounds_3$, the delay angle at which gating signal i_{G3} commences. This gating signal also is shown in figure 1.12. Thyristor Q_3 is turned on at $w_s t_3 = \pounds_3$, so that voltage v_{BN} appears across the load circuit, and the succeeding segment of the wave of output voltage v_o is described by equation 1.7 . The succeeding values of $\pounds_1$ and $\pounds_3$ may be determined from the corresponding intersections during each cycle of the source voltages.

During the first part of the cycle of v_o in figure 1.12, while $i_o^* > 0$ and thyristors Q_1 and Q_3 are being alternatively turned on, the gating sinals for thristors Q_4 and Q_2 are also being generated, but do not reach the thyristors, owing to the absence of signal N. The gating signals must commence at delay angles $\pounds_4$ and $\pounds_2$ such that, if they were indeed applied to rectifier N, they would yield an average output voltage equal to that of v_o at that instant of their application. This would constitute a negative voltage for rectifier N, and would signify inverter operation. During the first cycle of the source voltages the gating signal for thyristor Q_4 will commence when

$$v_{o4}^* = -\frac{2\sqrt{2}\,V}{\pi}\cos w_s t_4 \qquad 1.16$$

at an intersection for which

$$0 < w_s t_4 < \pi \quad \text{rad} \qquad 1.17$$

Correspondingly, the gating signal for thyristor Q_2 will commence when

$$v_{o2} = \frac{2\sqrt{2}\,V}{\pi}\cos w_s t_2 \qquad 1.18$$

atan intersection for which

$$\pi < w_s t_2 < 2\pi \quad \text{rad} \qquad 1.19$$

These signals are shown shaded in figure 1.12.

When the positive half wave of current ceases in figure 1.12, the waveform of v_o is interpreted, and signal P is removed. After an interval that must be at least as long as t_{off} for the thyristors, signal N commences, and gating signal i_{G2} and i_{G4} are applied to the thyristors.

After an interval $t_q > t_{off}$ negative current begins to flow from rectifier N acting as an inverter. This condition of operation persists until v_o^* goes negative, from which point on rectifier N acts as a rectifier. The modes of operation through the output cycle of the two controlled rectifiers that form the cycloconverter are indicated in figure 1.12. The maximum output voltage amplitude v_{om} is achieved when, from equation 1.5 & 1.8

$$v_{om}^* = \frac{2\,V}{\pi} \quad \text{volts} \qquad 1.20$$

1.2.2 THREE PHASE TO SINGLE PHASE CYCLOCONVERTER

The circuit diagram of a 3-phase to single phase cycloconverter is shown in figure 1.13. The pairs of terminals marked a and a' , b and b' , c and c' are joined together and connected to the three-phase supply. The major advantage of the three-phase as opposed to the single phase source of the same frequency lies in the increased rate of sampling that the three-phase source makes possible. In other words, during any given period, there are three times as many pulses of output current from the three-phase supplied converter. This means that, for a given level of subharmonic in the current wave, the output frequency for the three-phase excited converter. In the three-phase case therefore, typically

$$w_s \geq 3\, w_o \quad \text{rad/sec} \qquad 1.21$$

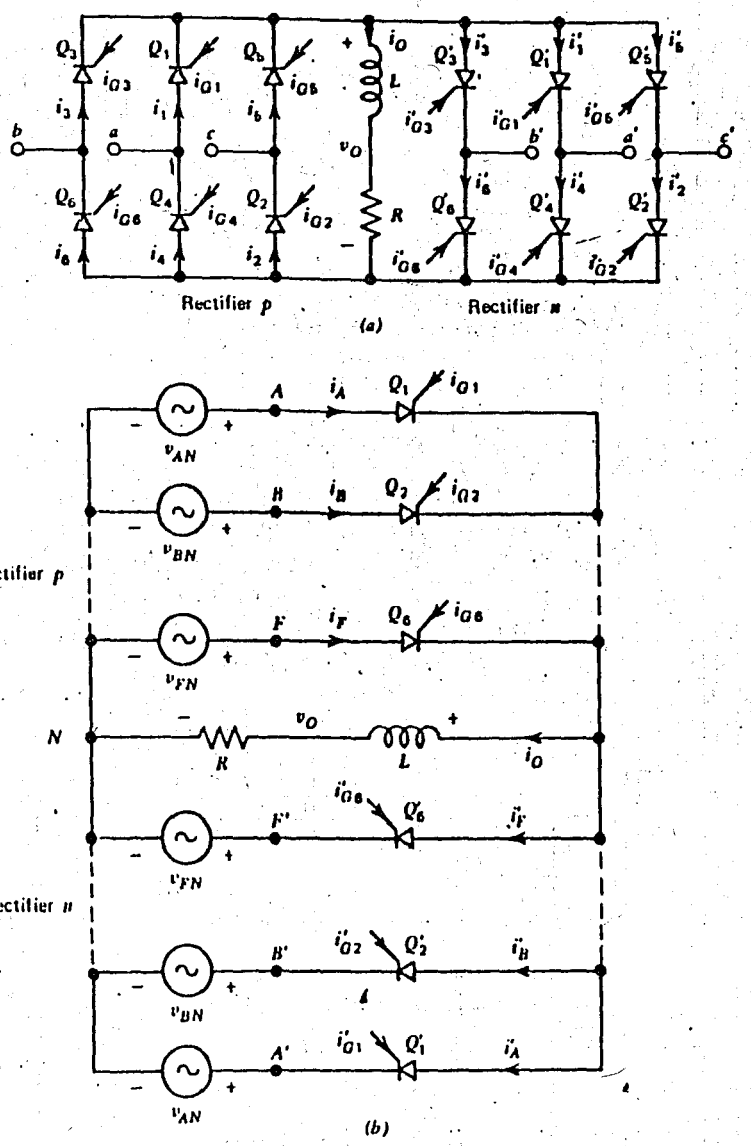


Figure 1.13 Three phase to single phase cycloconverter

As in the case of the single phase excited converter, an output current wave with low harmonic content can be achieved by modulation of the delay angles of all the thyristors in the converter.

In figure 1.14 the gate triggering signals are derived and the resulting output voltage waveform given. The waveforms obtained are for a leading power factor load.

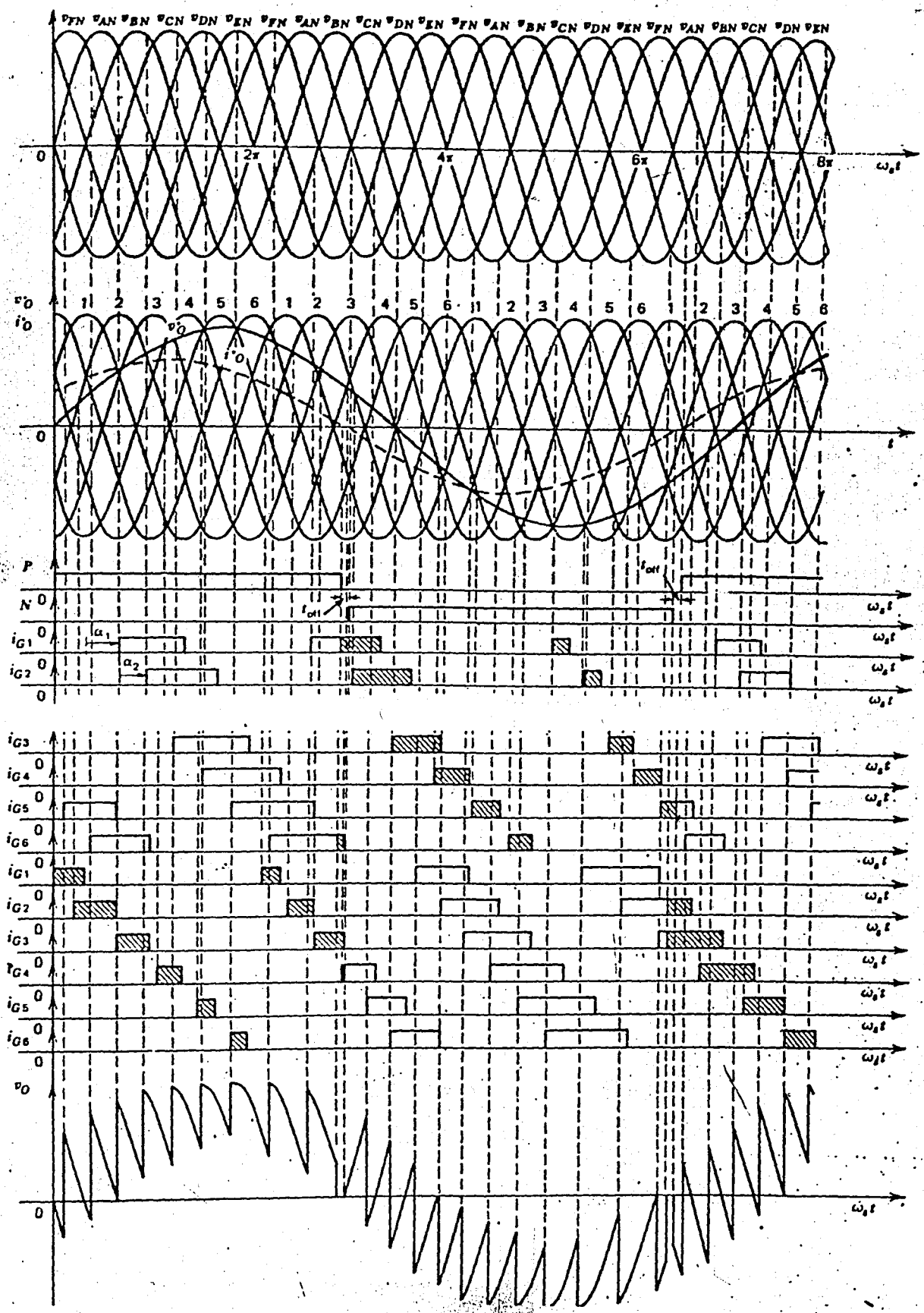


Figure 1.14 Reduction of output harmonics- Determination of δ
(Three phase to single phase)

CHAPTER II

WORKS PUBLISHED ON MICROPROCESSOR CONTROL OF CYCLOCONVERTERS

In this chapter, the works published up to date are presented and discussed. The titles of the papers are used as section headings.

II.1 A MICROPROCESSOR CONTROL OF A THREE-PULSE CYCLOCONVERTER (R,13)

On the IEEE-IECI-77 Conference, a method of controlling a three-phase cycloconverter was presented. Here the microprocessor calculates in real-time the SCR triggering instants as a function of the required output frequency and amplitude.

The cycloconverter is controlled by switching the SCR's ON and OFF according to a time schedule, described in various texts and papers (R,1-4). The criterion used to determine the triggering instants is the intersection of a reference voltage wave with a modulation voltage wave as explained in chapter I. Sinusoidal waves are used to maximize the fundamental component of the output voltage.

In this paper Harry H. Chen, (Member, IEEE) describes a method of controlling a cycloconverter (Three-pulse cycloconverter, see figure 13), using a microprocessor

(Intel 8080), that will eliminate the use of much of the complex analog control circuitry. The algorithm for this type of control differs fundamentally with the conventional control scheme. When the microprocessor is used, a set of triggering instants are computed several msec's in advance rather than at the triggering instant. The modulation and reference waves can be charecterized by equations;

$$f_m(t) = \sin(w_o \cdot t + \theta_o) \qquad 2.1$$

and

$$f_r(t) = Mag \cdot \sin(w_1 t + \theta_1) \qquad 2.2$$

respectively, where

w_o :modulation frequency in (rad/sec)

θ_o :modulation wave phase angle in (rad)

Mag :normalized magnitude of the reference wave $0.0 < Mag < 1.0$

w_1 :reference frequency in (rad/sec)

θ_1 :reference wave phase angle in (rad)

Clearly when $f_m(t)$ and $f_r(t)$ are equated, the solution for t cannot be determined in closed form. By the method of successive approximations a simple approximate solution $w_o t_{TR}$ is determined, which is expressed by equation below (See figure 2.1),

$$w_o t_{TR} \simeq (n\pi - \theta_o)\ \mathrm{Dir(Sign)}\left|\sin^{-1}(Mag\ \underbrace{\sin((n\pi-\theta_o)\tfrac{w_1}{w_o}+\theta_1-2m\pi)}_{c_1})\right| \qquad 2.3$$

where m=0,1,2,... and is chosen to satisfy $-\pi < c_1 < \pi$

$(n\pi-\Theta_o)$: n^{th} zero crossing of the modulation wave

Dir $\begin{cases} +1 \text{ when the modulation wave slope positive} \\ -1 \text{ when the modulation wave slope negative} \end{cases}$

Sign $\begin{cases} -1 \text{ when } -\pi < c_1 < 0 \text{ i.e. the reference is negative} \\ +1 \text{ when } 0 < c_1 < \pi \text{ i.e. the reference is positive} \end{cases}$

To program equation 2.3 Mag, Θ_1, w_1 & Θ_o have to be initialized. During normal control operations two parameters w_1 and Mag have to be input between calculation periods. The calculation period is chosen to span 12 intersections. During that time, the twelve intersections are computed, four for each modulation phase. This paper deals with developing a program used to quickly execute equation 2.3 for three phase modulation waves and only one reference wave. This case can be thought of as the single phase load case . This is the reason why only 12 intersections are computed insead of 18 (See figure 2.2). At the beginning of a calculation period Θ_1 and Θ_o are internally updated according to equations 1.4 & 1.5 .

$$\Theta_1(\text{new}) = \Theta_1 + w_o t_{TR}(12)\frac{w_1}{w_o} - 2v\pi \quad 2.4$$

$$\Theta_o(\text{new}) = \Theta_o + w_o t_{TR}(12) - 2q\pi \quad 2.5$$

where $w_o t_{TR}(12)$: the 12th intersection angle of a calculation set

$v = 0,1,2,\ldots$ and is determined by the inequality $0 < \Theta_1(\text{new}) < 2\pi$

$q = 0,1,2,\ldots$ and is determined by the inequality $0 < \Theta_o(\text{new}) < 2\pi$

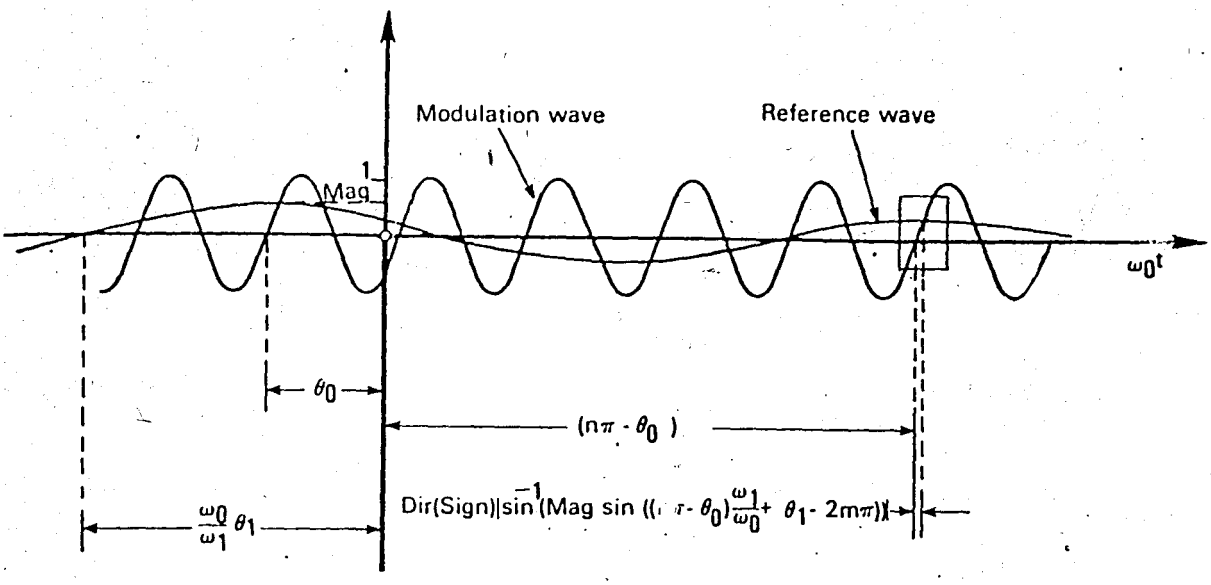
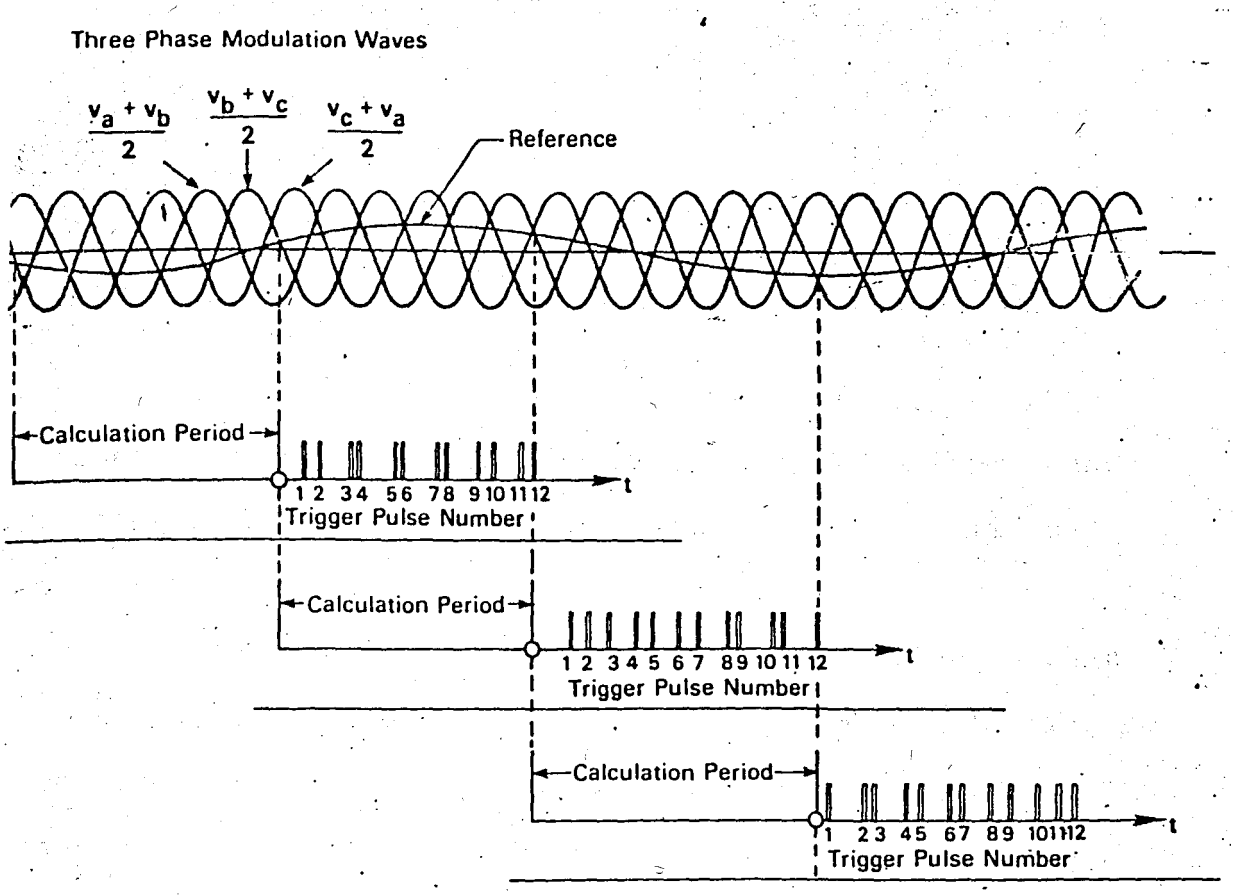


Figure 2.1 Sine modulation with sine reference waveform pair

Since the Intel 8080 does not contain multiplication hardware, a 16-bit multiplier is added as an I/O device using the AMD (Advanced Micro Devices) 25LS14 clocked at 25 MHz. 16 bit product can be performed in less than 3 microseconds. To further enhance the speed of the program, a sine and an arcsine look-up tables are included in memory. The program utilizing all of these aids, is calculated to have a maximum execution time of 7 msec. When more accuracy is desired, the need to use a more sophisticated algorithm arises. Chen gives a more accurate algorithm in the appendix of his paper, the execution of which is expected to be six times as long as the reference time of 7 msec, namely 42 msec.

In short, the main limitation of this type of control is the processing time, which defines the time delay of the control. Depending on the control system requirements, the time delay may or may not be acceptable for control applications.



igure 2.2 Updating scheme: Allocation of time sections for real time calculations of twelve triggering instants

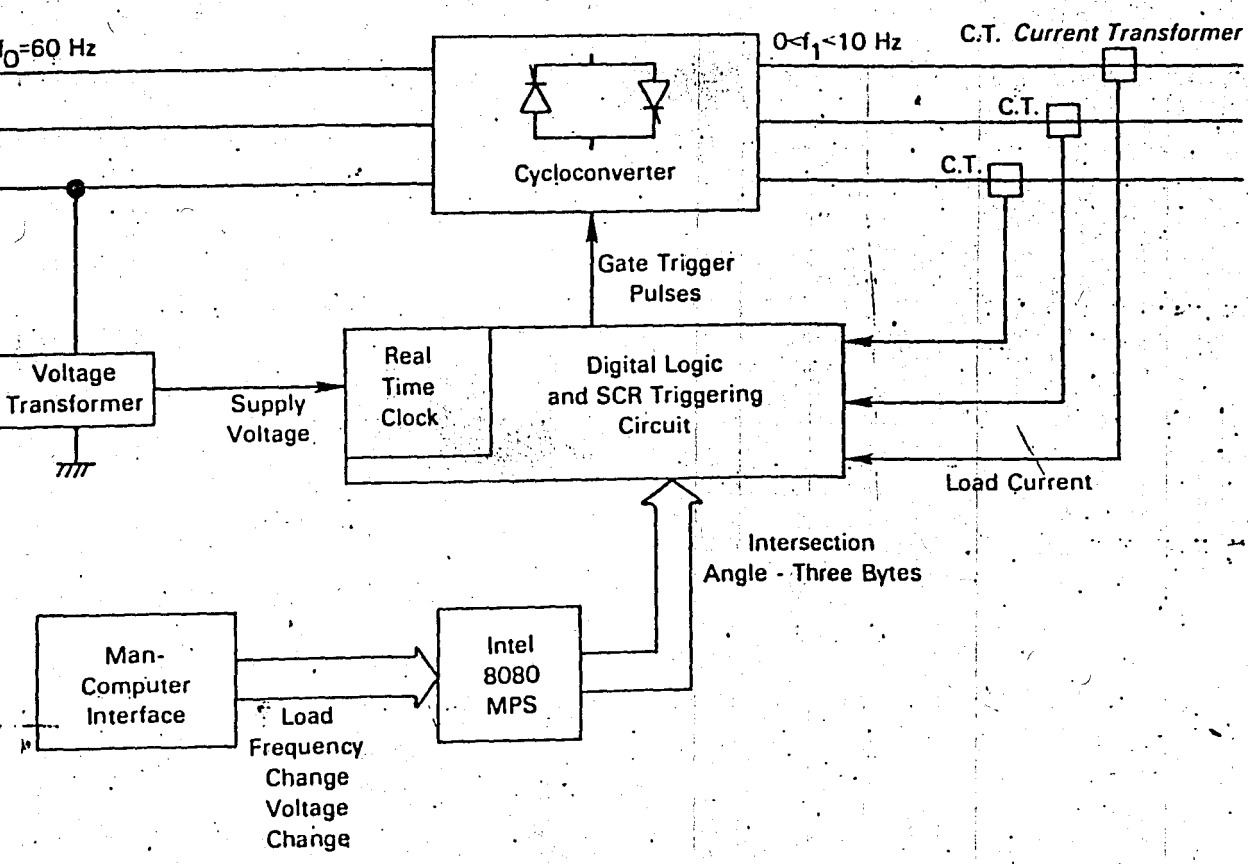


Figure 2.3 Block-diagram of microprocessor-based control system for a cycloconverter

II.2 A DIRECT DIGITAL CONTROL OF A THREE-PHASE SIX-PULSE CYCLOCONVERTER USING A MICROPROCESSOR (R,14)

On the IEEE-IECI-79 Conference a similar work was presented which was again the realization of a three phase to single phase cycloconverter, using Z-80 based microcomputer this time.

Since the concept is as said very similar to that of the work described in section II.1, the details will not be given here. The salient aspect of the work is this that software solutions to problems encountered are obtained, instead of using digital circuits such as counters and the comparators for deciding when to trigger the thyristors. The feature of the control system presented here is that the microprocessor is capable of directly triggering the thyristors without the external wired logic circuits.

Figure 2.4 shows a three-phase six-pulse cycloconverter consisting of two bridge converters connected back to back with one another. One converter which

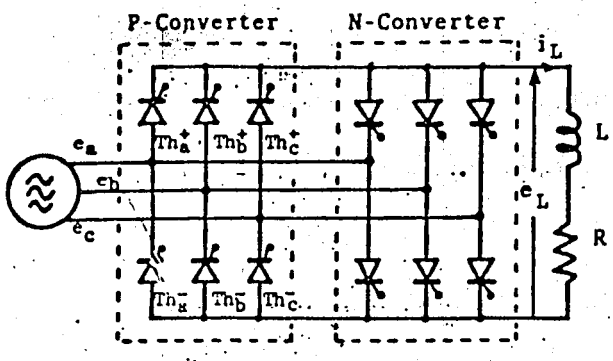


Figure 2.4
Six-pulse cycloconverter

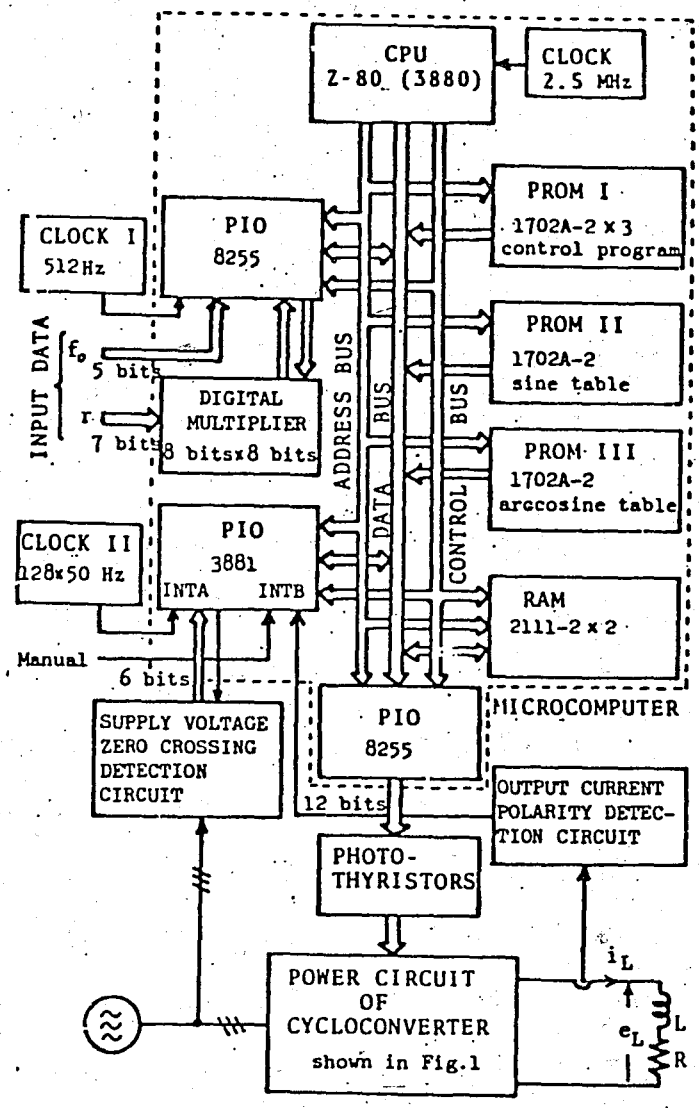


Figure 2.5
Hardware Block Diagram of the 3-phase 6-pulse cycloconverter

can carry the positive current is called the positive converter (P-converter) and another is negative converter (N-converter). Such an arrangement is able to carry current in both directions at its output terminals. By controlling the phase of its firing pulses with respect to the ac supply voltage, it can be made to produce a continuously controllable mean output voltage, of either polarity. Let the firing angle of P-converter be α_p and that of the N-converter be α_n. In order to obtain the sinusoidal output voltage $\bar{e}_L$ expressed by the equation

$$\bar{e}_L = E_o \cdot \sin \omega_o t \qquad 2.6$$

both converters should be controlled as follows:

When the output current i_L is positive, only the P-converter is allowed to conduct and the N-converter is completely blocked. The firing angle of the P-converter is determined by

$$E_{do} = \cos \pounds_p \cdot E_o \sin w_o t \qquad 2.7$$

Then $$\pounds_p = \cos^{-1} (r \sin w_o t) \qquad 2.8$$ where $r = E_o/E_{do}$ is called the output voltage ratio.

When the output current i_L is negative, only the N-converter is allowed to conduct and P-converter is blocked, vise versa. The firing angle of N-converter is

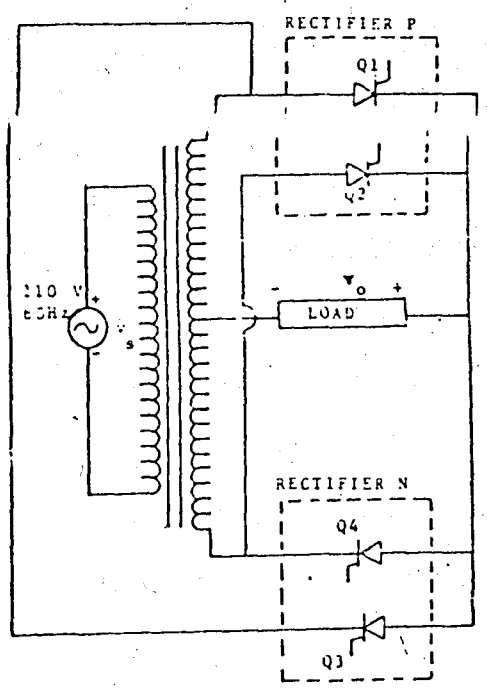
$$\pounds_n = \cos^{-1} (r \sin w_o t) \qquad 2.9$$

It is noted that $\pounds_p$ and $\pounds_n$ have values between 0 and $\pi - \gamma$ and that they are related by $\pounds_n + \pounds_p = \pi$.

Equations 2.8 and 2.9 are most important relationships here, which determine the firing angle of the cycloconverter Figure 2.5 illustrates a diagram of the proposed control system. This system consists of the microcomputer which is enclosed by dashed lines in the figure and a few peripherals. The control program is stored in the three EPROM's the sine and arccosine lookup-tables are stored in the other two EPROM's, respectively. And again the digital multiplier (8bit x 8bit) is present. To realize the quick execution of these programs, the proposed system has two clocks.

II.3 MICROCOMPUTER-CONTROLLED SINGLE-PHASE CYCLOCONVERTER (R,15)

Another similar but much simpler investigation of Singh & Hoft relates to the use of a basically square wave reference signal. The decision was not to modulate the firing angles of the thyristors to obtain a good sine-wave approximation but instead, to use the same firing angle on all thyristors for a required output voltage and frequency. While this no doubt simplifies computation and may be considered acceptable to certain restricted applications, the output voltage of the cycloconverter no longer approximates to a sinusoidal variation, of course (See figures 2.6 and 2.7 below).



re 2.6 Single phase to single phase cycloconverter

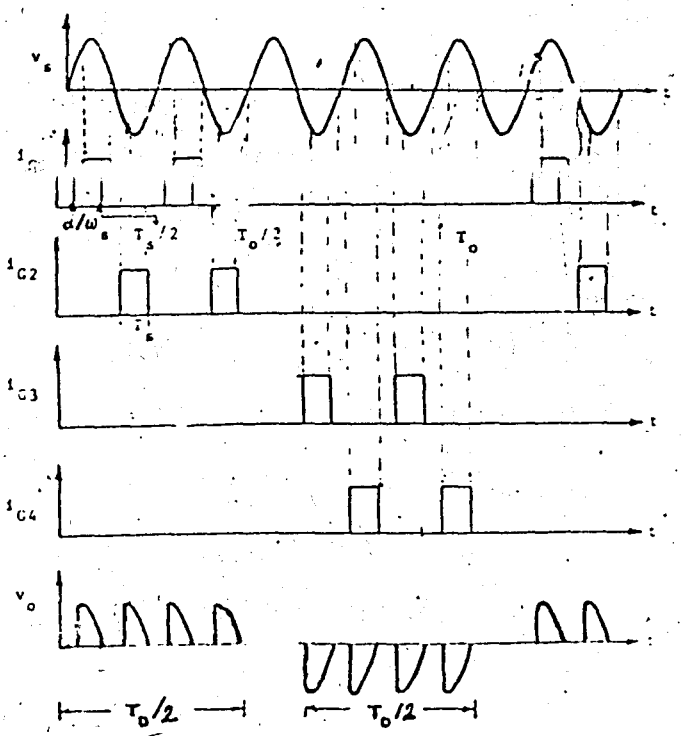


Figure 2.7 Gating Signals

I.4 EFFICIENT MICROPROCESSOR-BASED CYCLOCONVERTER CONTROL (R,16)

Another method is described in IEE proceedings in May 1980.

Digital control of a thyristor cycloconverter using a microprocessor offers the potential advantages of circuit simplification, precision in implementation and high system reliability. A practical constraint has been associated with the limited arithmetic capability of the microprocessor. This paper describes a method of cycloconverter control that expressly departs from the conventional cosine-timing control principle in the search for processing simplification. Equation 2.8 & 2.9 could be generalized as

$$\cos \alpha_{pj} = r \cdot \sin(w_o t_j - \varphi) \qquad 2.10$$

where t_j is the jth firing instant,

α_{pj} the corresponding firing control angle

r the modulation factor, $0 \leq r \leq 1$, and

φ an arbitrary angle.

In fact, the condition as specified in equation 2.10 forms the basis of the conventional cosine timing control method. α_{p1}, α_{p2}, α_{p3},... can be derived from the concecutive points of intersection obtained between a sine wave and a set of phase-displaced cosine waves.

In this paper an alternative scheme is described, which proves far superior for digital implementation as it relies on no numerical iterations or approximations. Equation 2.10 is first rearranged to give

$$\alpha_{pj} = \cos^{-1}\left(r \sin(w_0 t_j - \varphi)\right) \qquad 2.11$$

and $\quad 0 \leq \alpha_{pj} \leq \pi$

With reference to figure 2.8, it is proposed that a series of linear timing waves are conceptually introduced (in place of the conventional cosine waves but likewise synchronised to the supply waves), the jth timing wave e_{tj} being mathematically represented by

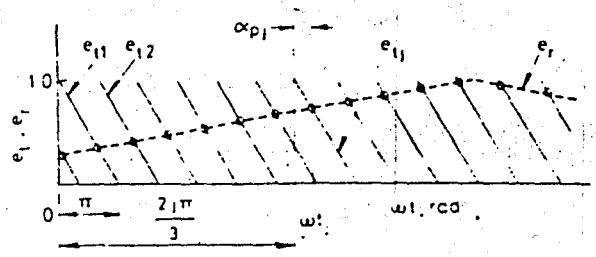


Figure 2.8 Firing control scheme based on linear timing waves.

$$e_{tj}(t) = 1 - \frac{wt}{\pi} + \frac{2}{3}j \qquad 2.12$$

$$j\pi \leq wt \leq (j+1)\pi$$

where it is implicitly assumed that 3-pulse circuits are employed for convenience of the present discussion and w is the angular frequency of the supply.

By choosing the reference signal to be of the particular form $\quad e_r(t) = 1 - \frac{1}{\pi}\cos^{-1}(r \sin(w_0 t - \varphi)) \qquad 2.13$

the condition embodied in equation 2.11 is then exactly satisfied because, at the jth point of intersection

$$wt_j - \frac{2\pi j}{3} = \cos^{-1}(r \sin(w_o t_j - \varphi)) \qquad 2.14$$

and also, from figure 20,

$$\varepsilon_{pj} = wt_j - \frac{2\pi j}{3} \qquad 2.15$$

The firing instant t_j can therefore be determined theoretically by equating equations 1.12 & 1.13 for integral values of j .

At the jth sampling instant, the reference signal is precisely

$$e_r\left(\frac{2\pi j}{3w}\right) = 1 - \frac{1}{\pi}\cos^{-1}\left(r \sin\left(w_o \frac{2j}{3w} - \varphi\right)\right) \qquad 2.16$$

Because e_r is held constant for the timing interval the firing delay can hence be determined explicitly and without recourse to any numerical iteration procedure. This is obtained as

$$\varepsilon_{pj} = \cos^{-1}\left(r \sin\left(\frac{2\pi j}{3w} w_o - \varphi\right)\right) \qquad 2.17$$

$$0 \leq \varepsilon_{pj} \leq \pi$$

The output frequency may in fact be entered as a scaled variable $w_o' = B\, w_o$, where $B = 2\pi/3w$ is predetermined as a constant for the system. In advancing from one firing instant to the next, the argument for the sine function is simply icremented by w_o' each time. A recurrent multiplication step is thus avoided. By providing a sine and arccosine table, only one multiplication step is then required for determined ε_{pj} based on equation 2.17 . The output variables r and w_o' can be independently changed according to control demands. The algorithm for determining ε_{nj} can be similarly obtained :

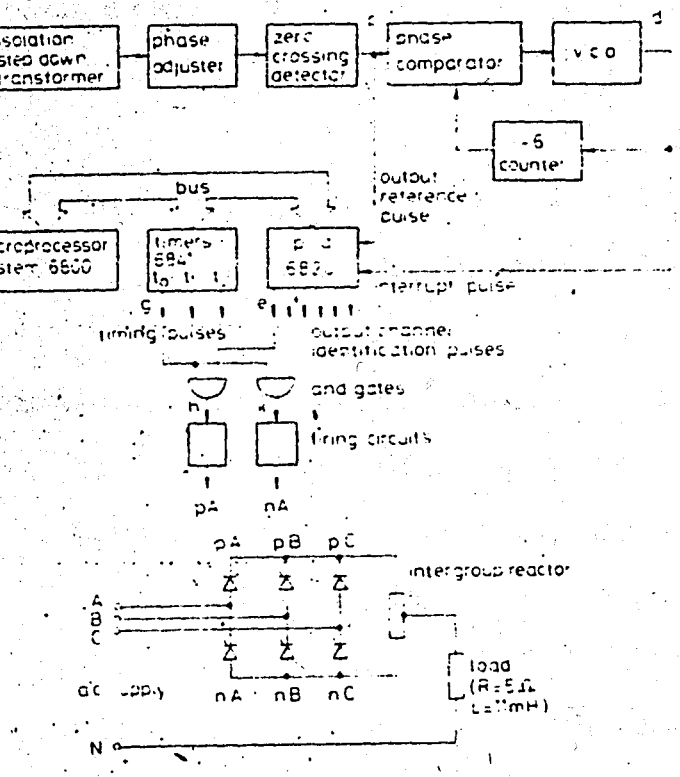
$$\mathcal{E}_{nj} = \cos^{-1}\left(-r \sin(jBw_o - Q)\right) \qquad 2.18$$

$$0 \leq \mathcal{E}_{nj} \leq \pi$$

The significance of the above development is the establishment of the firing delay expressions in closed form, with the minimum of arithmetic processing involved.

It is seen that the present approach offers practical solution to the nontrivial problem of applying effective digital control to the cycloconverter.

Experimental arrangement built around M 6800 components has been tried in the laboratory to verify the new control method developed. This consists of an M 6800 evaluation kit, an MC 6840 timer module and an MC 6820 p.i.a. unit(See figure 23). Based on the hardware shown in figure 29, the computation associated with each firing is completed in some 2.5 msec . Having in mind that 6800's twice as fast as the evaluation kit used are already available this is a real success.



gure 2.9 Schematic diagram of microprocessor controlled cyclo-converter

MICROPROCESSOR-CONTROLLED CYCLOCONVERTER (R,17)

A last paper about the subject is by Sonf B. Park & T.H.Choi . It is published in the proceedings of 1979 ISCAS. The 3-pulse circuit is extended to 6 pulses by using an interface transformer. As a result, it is possible to control the output frequency from 0 close to the line frequency which is not possible in the other arrangements.

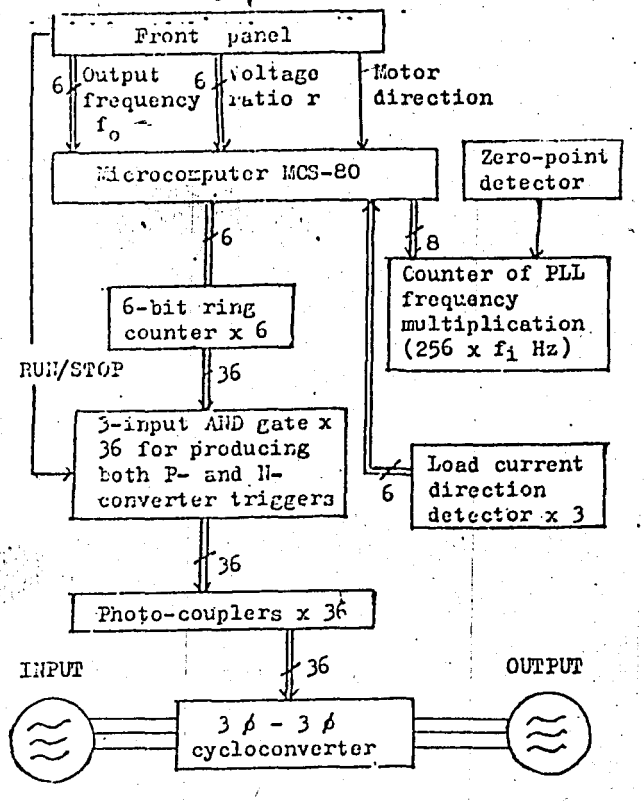


Figure 2.10 System Block Diagram

MCS-80 microcomputer kit is used. The required interface was just six 6-bit ring counters and 36, 3-input AND gates. The auxiliary circuits are also minimal: one crossing point detector for the input line voltages, three load current direction detectors and one PLL frequency multiplier. The firing angles are calculated according to the equation 2.8 again for phase U only. For the output phases V & W, the values of f_p can be used with taking into account the 120° and 240° phase differences.

CHAPTER III

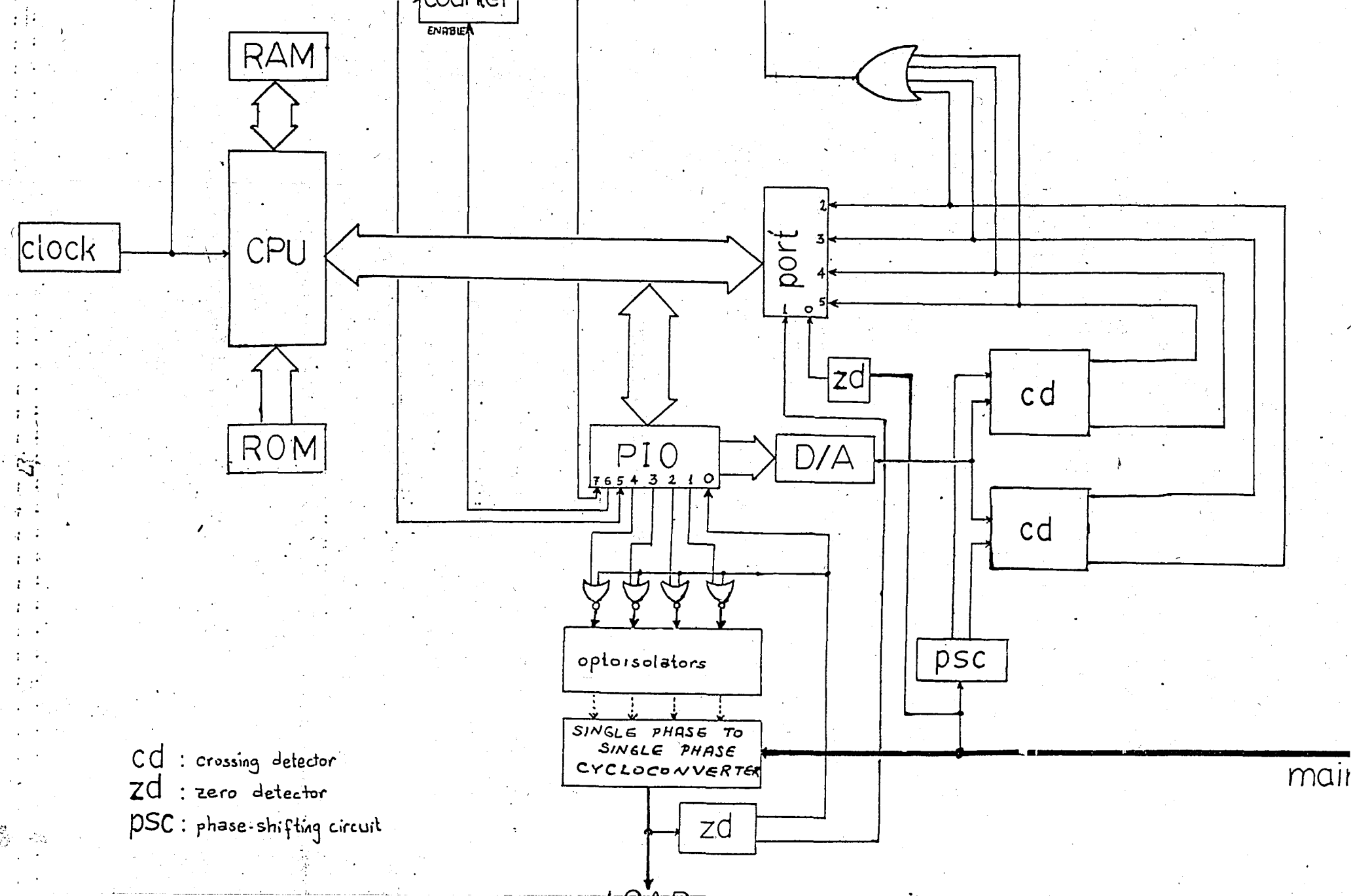
CONTROL METHOD USED IN THIS THESIS

III.1 GENERAL INFORMATION

The survey of the works published on the subject has shown that either a very simple approach is used as that of Ref.15, or with an attempt to eliminate any need for hardwired logic circuitry, a very complex system is arrived at.

In this thesis, a different approach is adopted in the sense that no attempt is made to replace all the functions of the conventional control circuitry by the microprocessor but rather an economical and simple design is tried to be arrived at by combining the advantages of both.

In order to keep the work within manageable limits a single phase to single phase configuration was used. The principle is however easily expandable to 3 phase to single phase or 3 phase to 3 phase cases.


counter
ENABLE
RAM
clock
CPU
ROM
port
2
3
4
5
1
0
zd
cd
cd
PIO
7 6 5 4 3 2 1 0
D/A
psc
optoisolators
SINGLE PHASE TO SINGLE PHASE CYCLOCONVERTER
zd
cd : crossing detector
zd : zero detector
psc : phase-shifting circuit
mai

The firing pulses for the cycloconverter were derived using "optimum firing scheme", for a constant output frequency i.e.5 Hz. Varying the delay angle α throughout each half cycle of the output waveforms the best approximation to a sinusoidal output current, hence the minimum current harmonics is obtained. The microcomputer system as well as the power circuit and the required interface were built, which will be discussed later in this chapter. Also the software was developed and tested. Finally, the output waveforms for various power factor loads are obtained. Figure 3.1 shows the block diagram of the system.

III.2 OPERATIONAL ASPECTS OF THE SYSTEM

1) Rules of control:

With reference to section 1.2.1c and figure 1.12, the control circuitry should be able to perform certain duties which can be summarized as follows:

a. To generate the reference sine wave i.e. 5 Hz

b. To get two modulation signals using the supply voltages having 180° phase difference with one another

c. To determine the crossing instants of the reference signal with the two modulation signals

d. To output the firing pulses depending upon the crossing; that is whether it is an "increasing" or a "decreasing" one with respect to the modulation signal

e. To get feed-back from the output current in order to know its polarity at that instant

f. Using the current feed-back to generate the blocking signal of the thyristors (for P as well as N group converters)

g. To ensure that a period is allowed for the conducting thyristors to fully turn-off

h. Under the light of the above considerations to turn on and off the appropriate thyristors at the right instances

The reference sine wave whose amplitude and the frequency determines the output voltage amplitude and frequency is generated by the processor digitally. This digital sine wave is then converted into an analog signal by means of an eight bit D/A (digital to analog) converter.

2). Interfacing Circuits:

The operations listed above are controlled partly by the microprocessor but also hardwired logic and analog circuits; namely two crossing detectors, a current zero detector, a positive going zero crossing detector, two phase shifting (90°) circuits and an 8-bit D/A converter are employed.

Two crossing detectors are used to detect the crossing points of the reference sine wave with the two modulation signals (these two modulation signals being 180° out of phase). They are simple comparators each one having two monostable multivibrators at their outputs (fig.A.2) the one being positive edge and the other one negative edge triggered respectively. As a result of this, either output 1 or output 2 of the crossing detector goes high depending upon the increasing or the decreasing character of the modulation signal, whenever a crossing exists. The width of the monostable output pulses is adjusted for a minimum width due to considerations explained in section III.3 .

The current zero detector circuit gives two putputs one of which indicates the current polarity and the other output stays high for a short period every time a polarity change takes place. As can be seen from the circuit diagram in A.5, the comparison is not done with 0 V as would be expected, but with a small voltage (50 mV). Assuming that this current feed-back is obtained across a 10 Ohm resistor in series with the load, this voltage corresponds to a current of 5 mA. So, in reality, not the zero crossings are detected, but the points at which the current falls below 5 mA in either direction. The reason for this is that the current will not reverse by

itself, but will reverse only if the other rectifier is turned on, which again can be done after the current has gone to zero. With a signal which does not reverse but goes to zero slowly and stays there, it can become difficult to detect the exact zero crossings. Hence, it was decided to detect crossings of the 5 mA point. It is important to note that the feed-back resistance must be selected in accordance with the load resistance so that it detects these 5 mA points but not a much higher level in magnitude.

The supply voltage zero crossing detector is similar to the crossing detector. In other words, it is a special case of the crossing detector in the sense that it is positive edge sensitive only which means that it has just one monostable multivibrator (therefore only one output) and one of its inputs is at ground level. The circuit thus obtained detects only positive going zero crossings as required.

The modulation signal is obtained from the supply voltage. However, as indicated in section I.2.1c it must be phase shifted by 90° before use. The circuit in A.8 simply does this job. Besides that, it attenuates the voltage waveform by a factor of $2/\pi$ as desired (See figure 1.12).

3) Computer and Memory Organization

The Central Processing Unit (CPU) and its peripherals are shown in figure A.1

The program and the sine table are stored in an EPROM+.

The memory organization is as follows:

EPROM	00 00 - 00 2E	Main Program	
	00 38 - 00 81	Interrupt Service Routine	
	00 90 - 01 57	Sine Table	
	01 58 - 03 FF	FF (empty space)	
RAM	04 00 - 04 08	Stack	

As indicated above a part of the memory is reserved for stack*. This is because the processor is used in interrupt mode and as a result of this the last address pointed by the program counter has to be saved so that the processor can return to the same program step after the interrupt has been serviced. Therefore a RAM (Random Access Memory) is required and the stack pointer has to be loaded appropriately at the beginning of the program to get this stack.

(+) Eraseble programmable read only memory

(*) The stack is an array of registers which allows words or addresses to be accessed from the top of this array on a last-in, first-out (LIFO) basis.

The computer needs input/output (I/O) ports to communicate with the outside world. Here a Z-80 PIO (Parallel I/O circuit) is used. This is a programmable, two port device which provides a TTL compatible interface between peripheral devices and the Z-80 CPU. It was decided to use port B to output the digitally generated sine wave as 8 bits data, and port A is programmed to operate in "Bit Control Mode" that is every bit is defined to be input or output individually, as listed below:

D_6	D_5	D_4	D_3	D_2	D_1	D_0
output counter enable	input crossing interrupt	output thyristor no.4	output thyristor no.3	output thyristor no.2	output thyristor no.1	input current polarity change

Bit 0 is set whenever the current changes polarity. Bits 1,2,3 & 4 are used to fire the thyristors. They are programmed to be active low. These bits are, of course, not directly coupled to the gates of the thyristors but isolation between the power circuit and the computer circuit is achieved using opto-couplers. Bit 5 becomes active whenever a crossing occurs between the reference sine wave and the modulation signals. Bit 6 is used for synchronization purposes, that is when a positive

going zero crossing of the supply voltage is met the processor sets this bit to enable the counter circuit (figure A.7). Synchronization of the digital sine wave to be generated with the supply voltage is thus achieved. Since a full period of the sine wave is approximated using 200 values (See Appendix , B.3), a value needs to be outputted every 1 msec to obtain the digital sine wave of 5 Hz. Two 4518 counter chips shown in figure A.7 achieve this by effectively dividing 2 MHz clock by 2000. The output thus obtained is fed to the last bit of port A, i.e. bit 7.

Besides this PIO, another input port is required, 4 bits of which are reserved for the crossing information (bits 2,3,4 & 5). Bit 1 has the information of the polarity of the output current, that is a low level on this pin means positive whereas a high level means negative. Bit 0 gets information of the supply voltage zero crossing, as indicated above, namely the positive going zero crossing. The organization of this input port made up of two 74125 chips is as follows:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
not used	not used	crossing due to tap 1 up going	crossing due to tap 1 down going	crossing due to tap 2 up going	crossing due to tap 2 down going	current polarity 0, pos. 1, neg.	positive going zero crossing active high

I.3 FLOWCHART & PROGRAM

The flowcharts to meet the gating signal requirements are shown in figures 3.2 & 3.3 . The main program just prepares the conditions required and starts the system at the right instant. But the interrupt service routine is the heart of the program. Mainly the processor has two jobs; either a crossing exists which must be taken care of, or else it is time to put a new sine value out to the port. These are all done in interrupt service routine.

It is very important not to miss any valid interrupt requests. There are three sources of interrupt requests, two of them being due to crossings of the modulation signals with the reference sine wave and the third one being for the generation of the digital sine wave. It is noted from the flowchart that not every crossing will result in a change in thyristor pulses. For instance, if the current is positive decreasing crossings of the modulation wave are used only, and crossings of increasing character are not considered. They are so forth called invalid crossing points. If the current is negative on the other hand, the decreasing crossings are invalid. At the worst case the three interrupt requests might occur at the same time, one of them being invalid crossing interrupt necessarily. The point is that the two valid interrupt requests are not allowed to be missed but the

invalid one.

The program of the interrupt service routine is prepared so that every valid crossing interrupt will be executed in 65 μsec whereas every invalid one in 53 μsec. These time intervals are kept constant by introducing extra instructions -no operation- in the branches where necessary. Sine wave generation on the other hand lasts 40 usec. As a result of this, the best choice of the pulse widths of the interrupt signals seems to be 35 usec and 60 usec, for the reference sine wave and the crossings respectively. This choice gave satisfactory results.

Z-80 CPU can be programmed to respond to the maskable interrupt in three possible modes. In this work it is decided to use mode 1 . When this mode is selected, the CPU will respond to an interrupt by executing a restart to location 0038H.

Z-80 PIO may be operated in any of four distinct modes. Port A of PIO is chosen to operate in Mode 3. When this mode is selected, the next control word sent to the PIO must define which of the port data lines are to be inputs and which are outputs.

Port B of PIO is programmed on the other hand to operate in Mode 0, which is output mode.

These modes are chosen at the beginning of the main program before the system starts to operate (See figure 3.2).

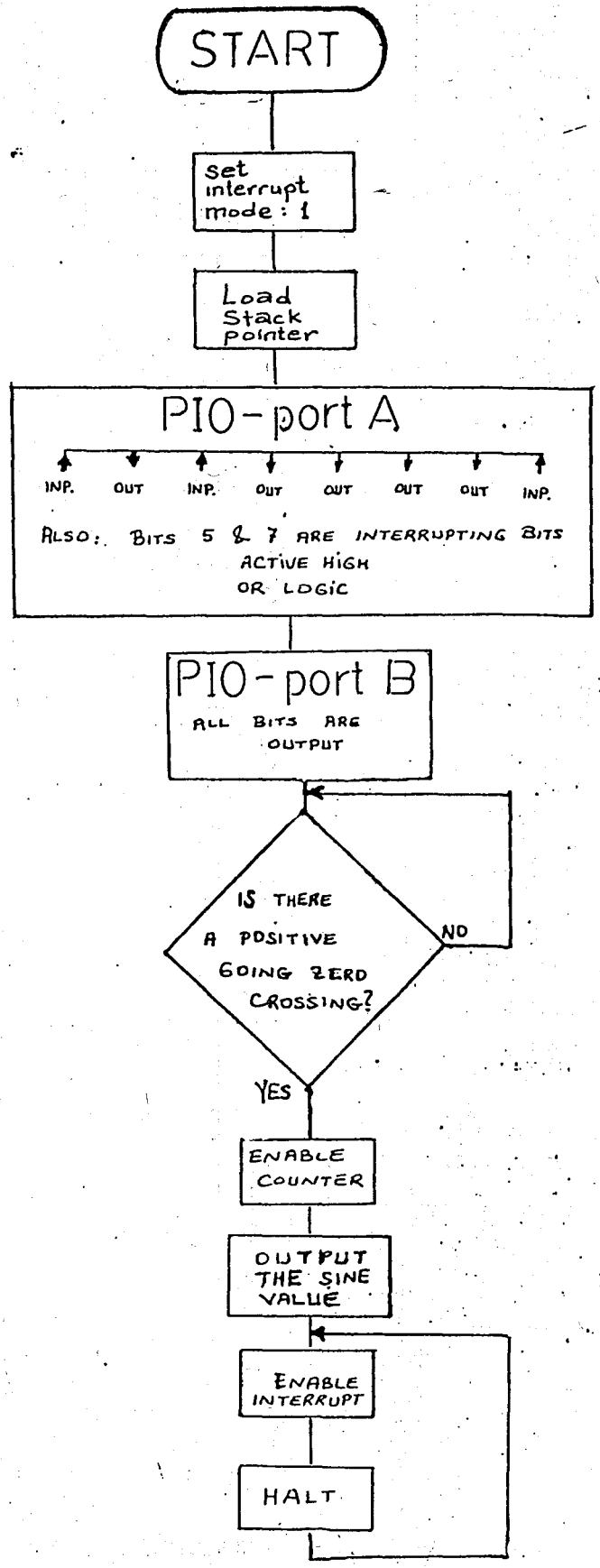


Figure 3.2 The flowchart of the main program

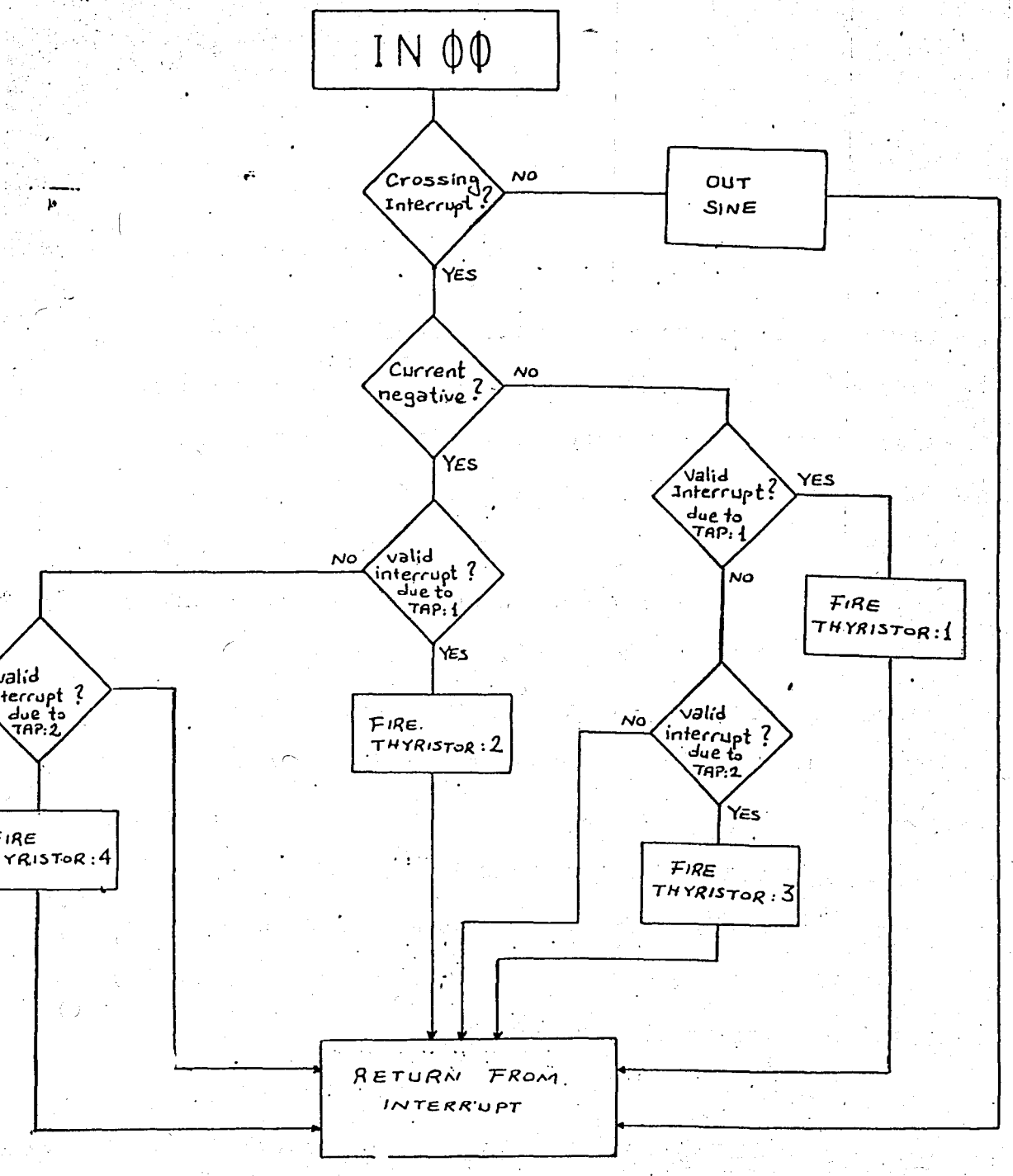


Figure 3.3 The flowchart of the interrupt service routine

CHAPTER IV

CONCLUSION

IV.1 EXPERIMENTAL RESULTS

As explained in the previous chapter the interrupt service routine is the heart of the program. Because of the reason that the two sources of interrupt requests are serviced in the same routine the possibility to miss an interrupt request arises.

The interrupts might be due to:

a) A valid interrupt, requiring 65 μsec

b) An invalid crossing interrupt, requiring 53 μsec

c) A sine-wave clock interrupt, requiring 40 μsec

to be serviced.

If the width of the crossing interrupt signal is adjusted to be 60 usec satisfactory operation is ensured as,

(i) if (a) occurs shortly before (b), (b) will be missed but causes no problem since that is an invalid interrupt request in any case

(ii) if (b) occurs before (a), the signal due to (a) is still there when CPU comes out of interrupt service routine so that (a) is serviced.

(iii) if (c) occurs before (a) or (b), (a) is still serviced.

In this way it is ensured that (a) is never missed.

The width of the sine-wave clock interrupt should not however be greater than 40 μsec since otherwise two sine values will be outputted consequently. The width was therefore adjusted to be 35 μsec. Due to this if (a) occurs at least 30 μsec before (c) or (b) occurs at least 18 μsec before (c), (c) will be missed. This is not very important, since the output waveform will be 5.001 Hz in that cycle instead of 5.00 Hz. This is within the accuracy of the 2 kHz clock in any case.

In section I.2.1b operation with continuous output current was discussed. The condition for this was stated in equation 1.4 as:

$$0 \leq \pounds < \emptyset \quad \text{, where} \quad \emptyset = \tan^{-1}(wL/R)$$

In the single phase to single phase converter this condition is very difficult to be achieved, because referring to figure 1.12, the firing angle of thyristors can be near or even above 90°. Consequently, even with very highly inductive load, continuous current can never be obtained. Such a case would not arise in 3-phase to single phase cycloconverter in which a moderately inductive load would ensure continuous current.

Due to above considerations, the operation of the present system is disrupted when the current feed-back level goes below 50 mV in either direction as this is translated as a current polarity change.

In order to demonsrate the capabilities of the system, continuous current was simulated in three different ways. In the first case positive current was simulated and the oscillogram is shown in figure 4.1 .

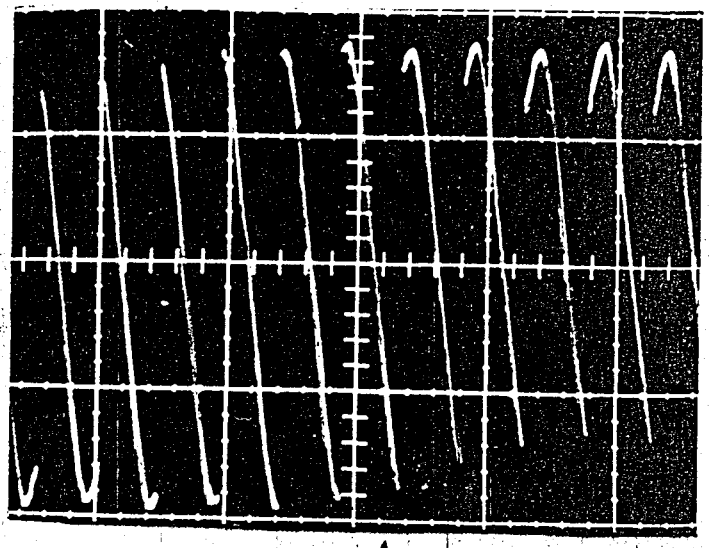


Figure 4.1 Output voltage wave-form for positive current

For a negative current simulation the wave-form is presented in figure 4.2 .

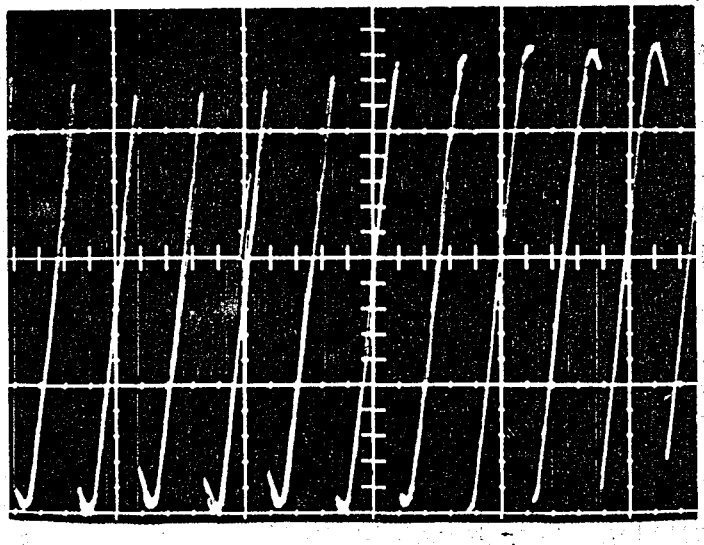


Figure 4.2 Output voltage wave-form for negative current

Finally the oscillograms corresponding to a sine-wave output current are shown in figures 4.3a & 4.3b .

Figure 4.3a

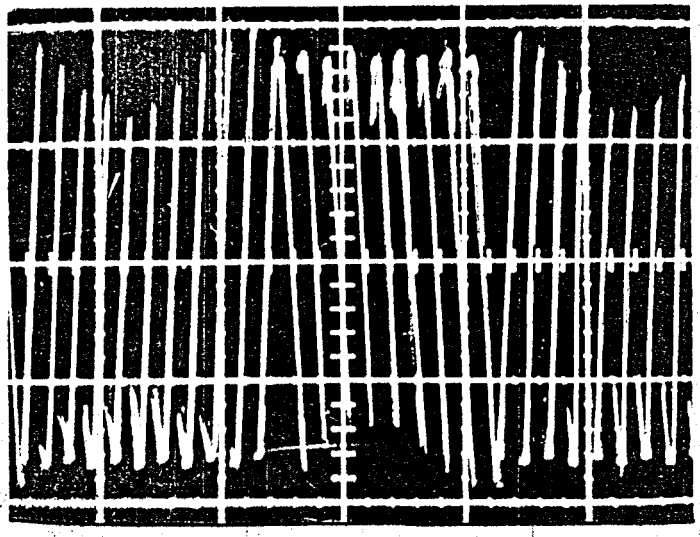
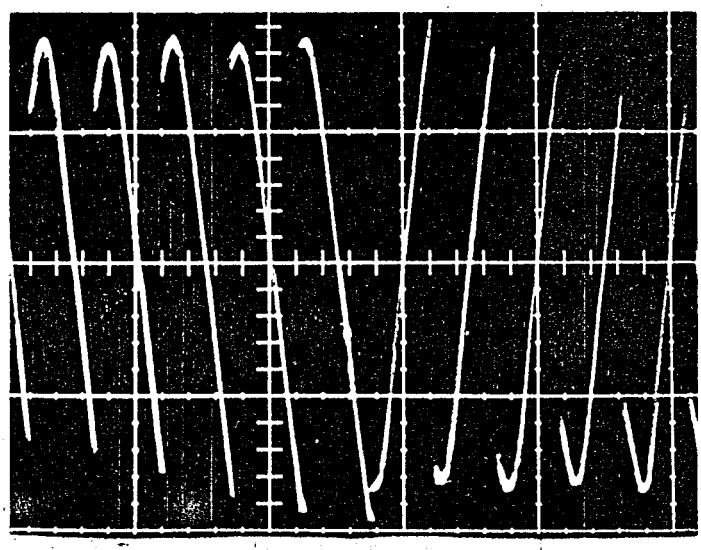


Figure 4.3b



Output voltage wave-forms corresponding to sinusoidal output current

IV.2 CONCLUDING REMARKS

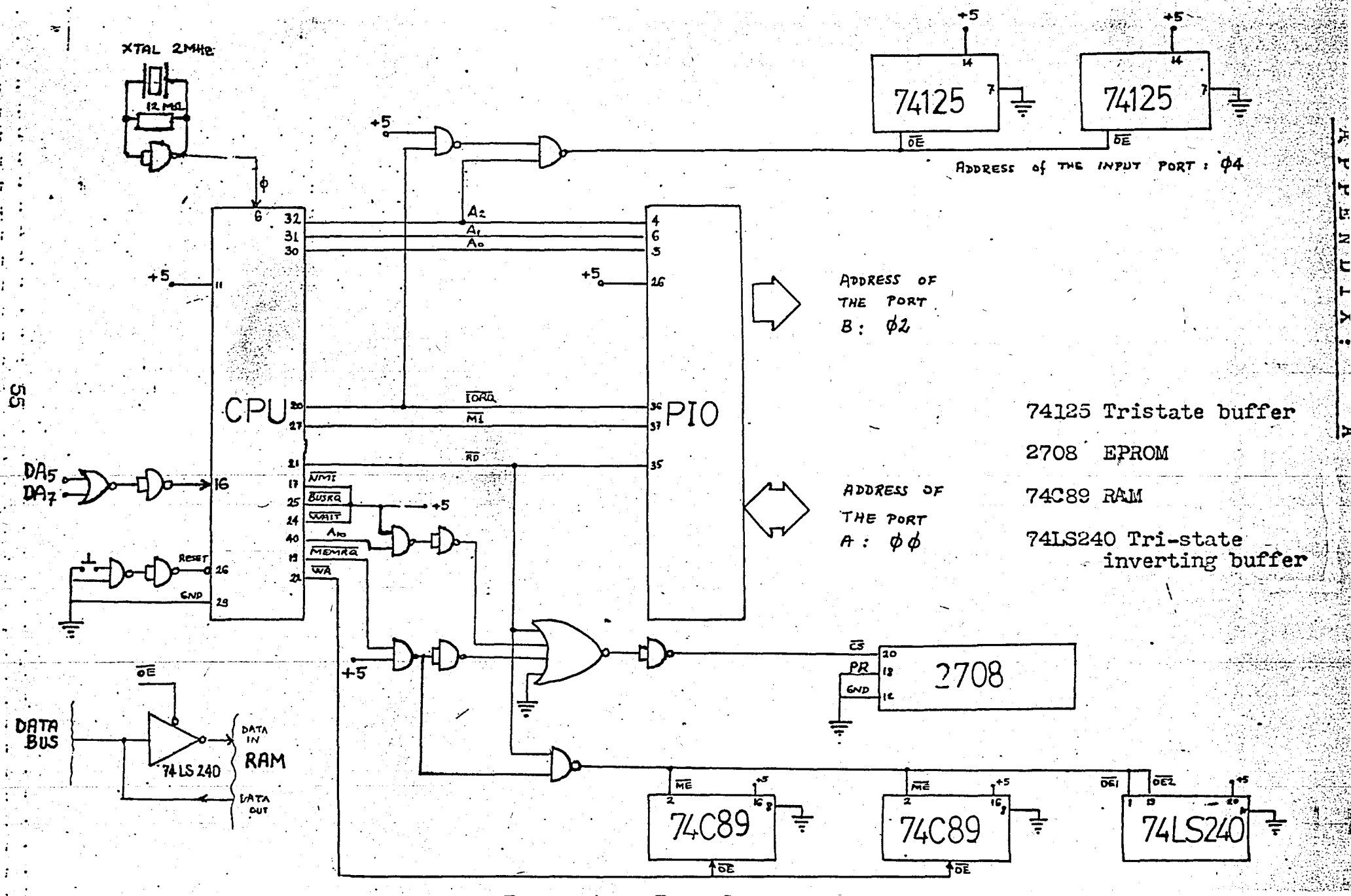
The results showed that this method of control is a practical solution for cycloconverter control. Since the basic aim was to introduce the new technique onsisting of microprocessor and analog circuitry. It is preferred to see the experimental results simply in a single phase to single phase converter. The method however applies easily to the 3 phase to single phase case. Then four extra crossing detectors and also an output port (8 bits) are required if the 12 bits of output are to be directly coupled to the 12 thyristors. Alternatively, without using any new output port, an 4 to 16 decoder could be employed to select 12 thyristors by 4 bits of output only.

The sine wave clock frequency determines the output frequency. If the need arises to change this frequency within the program a digitally programmable counter is required. Zilog has such an integrated circuit Z-80 CTC (Z-80 Counter-Timer Circuit). This is a programmable component with four independent channels that provide counting and timing functions for microcomputer systems based on the Z-80 CPU. In timer mode the CTC generates timing intervals that are an integer value of the system

clock period. Periods of 125 μsec up to 32 msec can be obtained in 256 steps, with the prescaler factor of 256, using the 2 MHz clock.

The system could also be operated without using interrupt mode, then RAM would not be required, therefore the hardware cost would decrease. In this case the program returns to the beginning of the subroutine instead of to the end of the main program, where the processor halts. Of course, a delay up to 53 or 65 μsec is expected whenever the processor is supposed to give a new decision.

In order not to miss the sine-wave interrupt requests the non-maskable interrupt of the processor could be used for digital sine wave generation. In that case there would be two interrupt service routines; one for sine-wave generation (NMI) and the other one for the crossings (MI). As a result the accuracy of the reference sine wave frequency is increased.



74125 Tristate buffer

2708 EPROM

74C89 RAM

74LS240 Tri-state inverting buffer

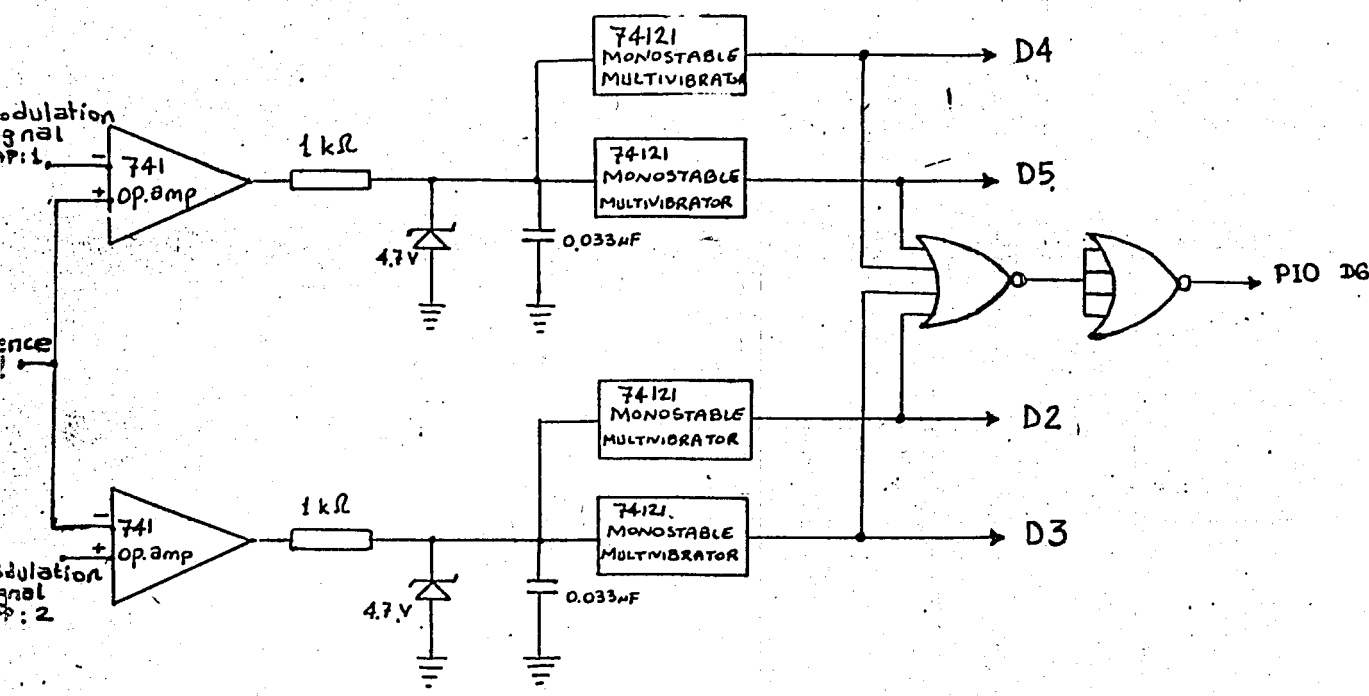


Figure A.2 Crossing Detectors for reference and modulation waves

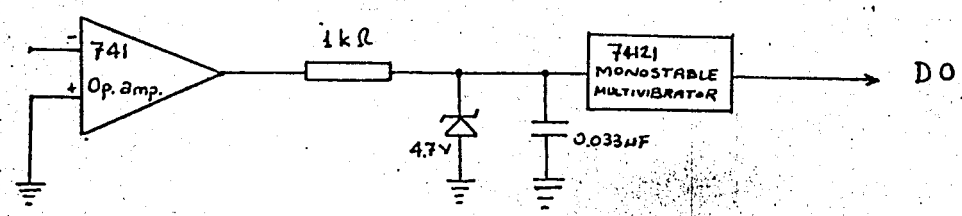


Figure A.3 Supply voltage zero crossing detector

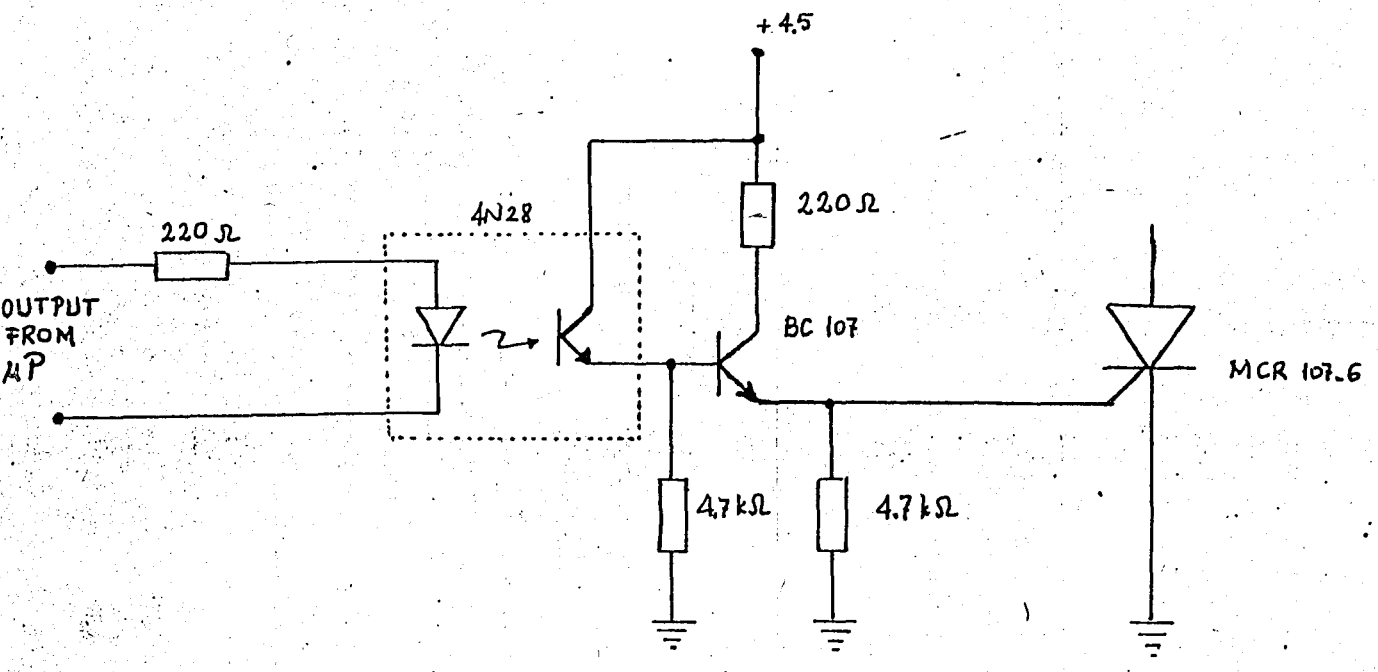


Figure A.4 Opto-isolated driving of thyristors using the processor outputs

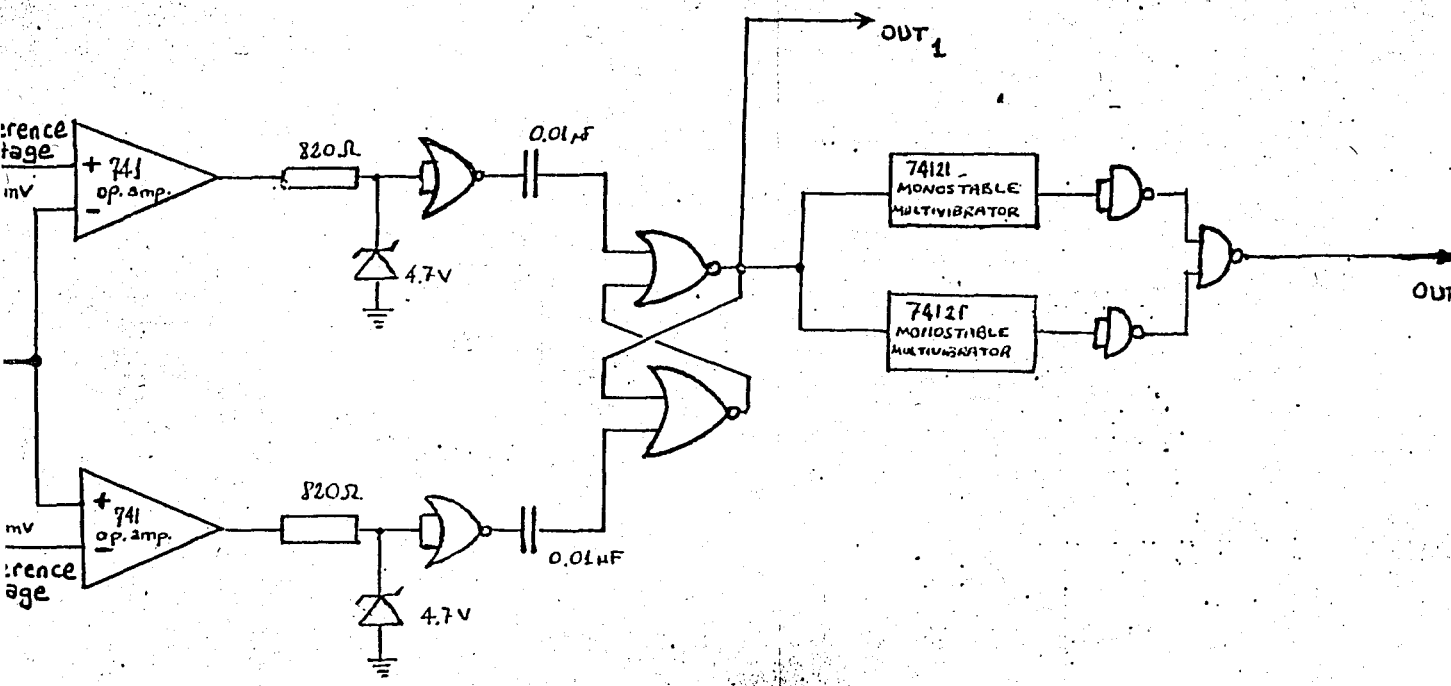


Figure A.5 Output Current Detector

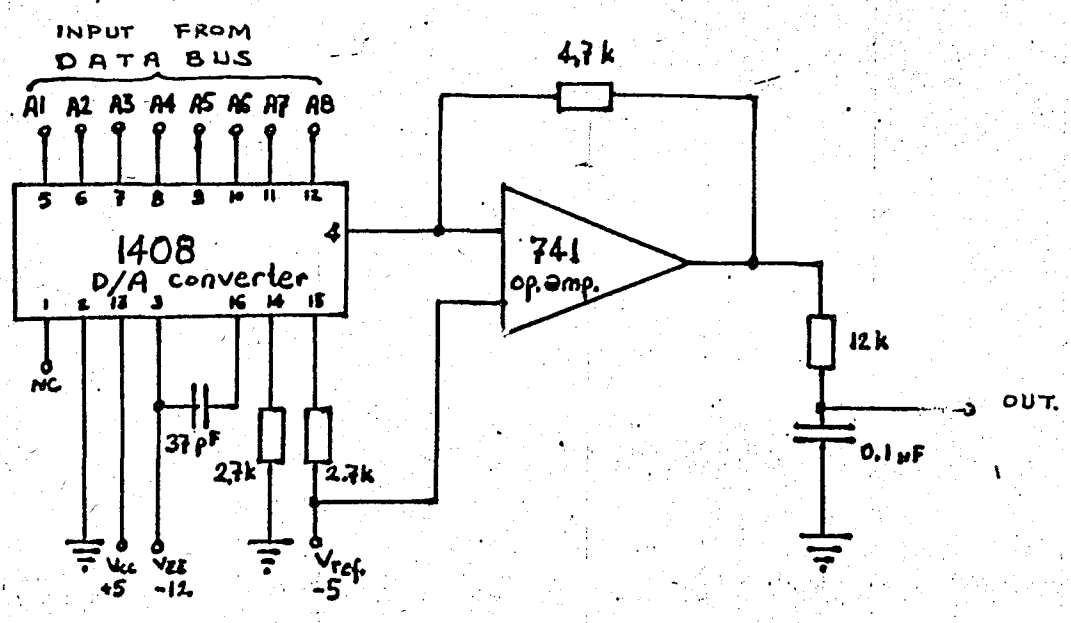


Figure A.6 Bipolar output voltage circuit for D/A converter

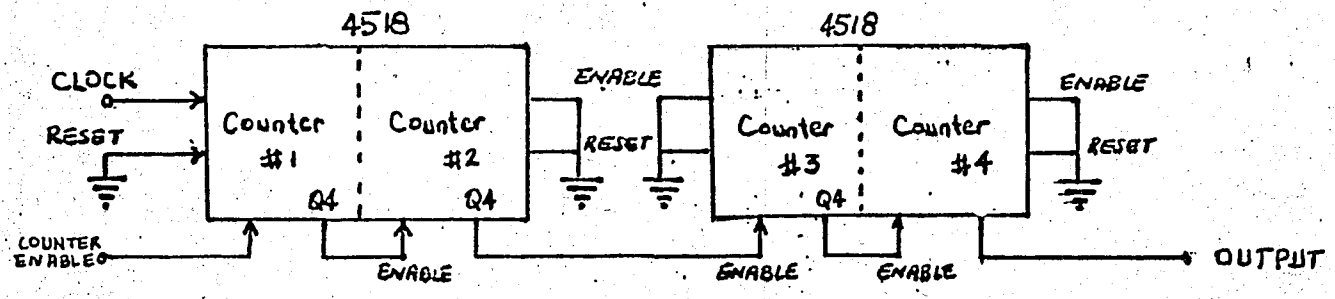


Figure A.7 Counter circuit for sine generation

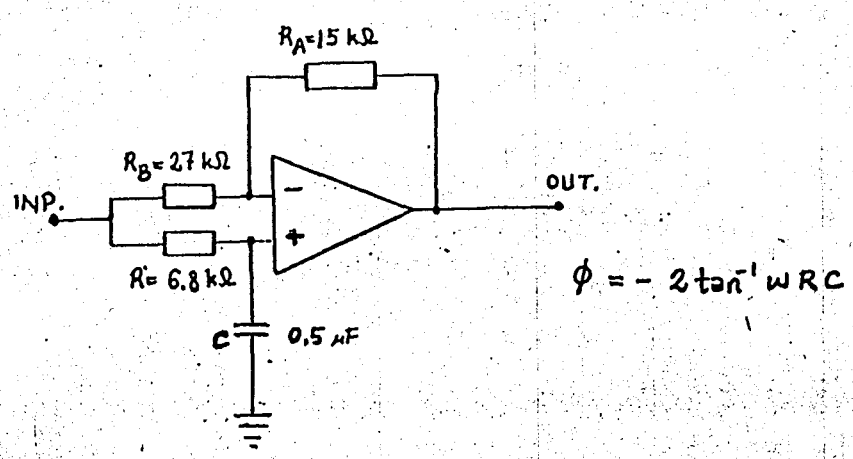


Figure A.8 Phase shifting circuit and attenuator

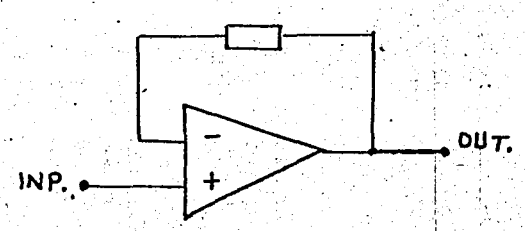


Figure A.9 High impedance buffer
(to use as supply voltage follower)

APPENDIX: B

B.1 MAIN PROGRAM

00 00	ED 56	SET INT MODE 1	setting interrupt mode
00 02	31 08 04	LD SP, 04 08	loading stack-pointer
00 05	3E CF	LD A, CF	programming port A of PIO
00 07	D3 01	OUT 01	
00 09	3E A1	LD A, A1	
00 0B	D3 01	OUT 01	
00 0D	3E B7	LD A, B7	
00 0F	D3 01	OUT 01	
00 11	3E 5F	LD A, 5F	
00 13	D3 01	OUT 01	
00 15	3E 0F	LD A, 0F	programming port B of PIO
00 17	D3 03	OUT 03	
00 19	0E 02	LD C, 02	defining the sine table
00 1B	06 C8	LD B, C8	
00 1D	21 90 00	LD HL, 00 90	
00 20	DB 04	IN 04	positive going zero crossing of the supply voltage
00 22	1F	RRA	
00 23	30 FB	JRNC	
00 25	3E 5E	LD A, 5E	enable counter
00 27	D3 00	OUT 00	
00 29	ED A3	OUTI	utput the firs sine value
00 2B	FB	EI	enable interrup
00 2C	76	HALT	wait for interrupt
00 2D	18 FC	JR	

B.2 INTERRUPT SERVICE ROUTINE

00 38	DB 00	IN 00	sine wave interrupt or crossing interrupt?
00 3A	CB 6F	BIT 5,A	
00 3C	28 34	JRZ	
00 3E	DB 04	IN 04	check for current polarity
00 40	CB 4F	BIT 1,A	
00 42	28 14	JRZ	
00 44	CB 6F	BIT 5,A	
00 46	28 06	JRZ	
00 48	3E 5A	LD A, 5A	
00 4A	D3 00	OUT 00	fire thyristor 2
00 4C	18 32	JR	
00 4E	CB 5F	BIT 3,A	
00 50	28 2E	JRZ	
00 52	3E 4E	LD A, 4E	
00 54	D3 00	OUT 00	fire thyristor 4
00 56	ED 4D	RETI	
00 58	CB 67	BIT 4,A	
00 5A	28 0B	JRZ	
00 5C	3E 5C	LD A, 5C	
00 5E	D3 00	OUT 00	fire thyristor 1
00 60	00	NOP	
00 61	00	NOP	
00 62	00	NOP	

00 63	00	NOP	
00 64	00	NOP	
00 65	ED 4D	RETI	
00 67	CB 57	BIT 2, A	
00 69	28 14	JRZ	
00 6B	3E 56	LD A, 56	
00 6D	D3 00	OUT 00	fire thyristor 3
00 6F	00	NOP	
00 70	ED 4D	RETI	
00 72	ED A3	OUTI	
00 74	20 07	JRNZ	
00 76	06 C8	LD B, C8	redefine the sine table
00 78	21 90 00	LD HL, 00 90	
00 7B	ED 4D	RETI	
00 7D	00	NOP	
00 7E	00	NOP	
00 7F	00	NOP	
00 80	ED 4D	RETI	

B.3 SINE TABLE

00	90	80	83	87	8B	8F	93	97	9B
00	98	9F	A3	A7	AA	AE	B2	B5	B9
00	A0	BD	C0	C4	C7	CA	CD	D1	D4
00	A8	D7	DA	DC	DF	E2	E4	E7	E9
00	B0	EB	ED	EF	F1	F3	F4	F6	F7
00	B8	F9	FA	FB	FC	FD	FD	FE	FE
00	C0	FE	FF	FF	FF	FE	FE	FE	FD
00	C8	FD	FC	FB	FA	F9	F7	F6	F4
00	D0	F3	F1	EF	ED	EB	E9	E7	E4
00	D8	E2	DF	DC	DA	D7	D4	D1	CD
00	E0	CA	C7	C4	C0	BD	B9	B5	B2
00	E8	AE	AA	A7	A3	9F	9B	97	93
00	F0	8F	8B	87	83	80	7C	78	74
00	F8	70	6C	68	64	60	5C	58	55
01	00	51	4D	4A	46	42	3F	3B	39
01	08	35	32	2E	29	28	25	23	20
01	10	1D	1B	18	16	14	12	10	0E
01	18	0C	0B	09	08	06	05	04	03
01	20	02	02	01	01	01	00	00	00
01	28	01	01	01	02	03	03	04	05
01	30	06	08	09	0B	0C	0E	10	12
01	38	14	16	18	1B	1D	20	23	25
01	40	28	29	2E	32	35	39	3B	3F
01	48	42	46	4A	4D	51	55	58	5C
01	50	60	64	68	6C	70	74	78	7C

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